

FEATURES

Current Conditioning
Complete Vector Transformation on Silicon
Three-Phase 120° and Orthogonal 90° Signal Transformation
Three-Phase Balance Diagnostic—Homopolar Output
DQ Manipulation
Real-Time Filtering

APPLICATIONS

AC Induction Motor Control
Spindle Drive Control
Pump Drive Control
Compressor Drive Control and Diagnostics
Harmonic Measurement
Frequency Analysis
Three-Phase Power Measurement

GENERAL DESCRIPTION

The AD2S105 performs the vector rotation of three-phase 120 degree or two-phase 90 degree sine and cosine signals by transferring these inputs into a new reference frame which is controlled by the digital input angle ϕ . Two transforms are included in the AD2S105. The first is the Clarke transform which computes the sine and cosine orthogonal components of a three-phase input. These signals represent real and imaginary components which then form the input to the Park transform. The Park transform relates the angle of the input signals to a reference frame controlled by the digital input port. The digital input port on the AD2S105 is a 12-bit/parallel natural binary port.

If the input signals are represented by V_{ds} and V_{qs} , respectively, where V_{ds} and V_{qs} are the real and imaginary components, then the transformation can be described as follows:

$$\begin{aligned} V_{ds}' &= V_{ds} \cos\phi - V_{qs} \sin\phi \\ V_{qs}' &= V_{ds} \sin\phi + V_{qs} \cos\phi \end{aligned}$$

Where V_{ds}' and V_{qs}' are the output of the Park transform and $\sin\phi$, and $\cos\phi$ are the trigonometric values internally calculated by the AD2S105 from the binary digital data ϕ .

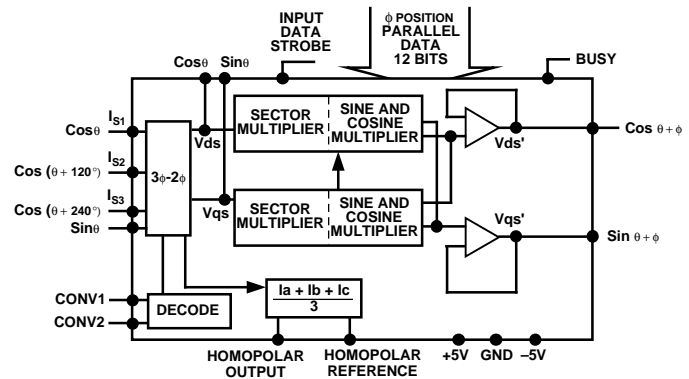
The input section of the device can be configured to accept either three-phase inputs, two-phase inputs of a three-phase system, or two 90 degree input signals. The homopolar output indicates an imbalance of a three-phase input only at a user-specified level.

The digital input section will accept a resolution of up to 12 bits. An input data strobe signal is required to synchronize the position data and load this information into the device counters.

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FUNCTIONAL BLOCK DIAGRAM



A two-phase rotated output facilitates the implementation of multiple rotation blocks.

The AD2S105 is fabricated on LC²MOS and operates on ± 5 volt power supplies.

PRODUCT HIGHLIGHTS

Current Conditioning

The AD2S105 transforms the analog stator current signals (I_{s1} , I_{s2} , I_{s3}) using the digital angular signal (reference frame) into dc values which represent direct current (I_{ds}) and quadrature current (I_{qs}). This transformation of the ac signals into dc values simplifies the design of the analog-to-digital (A/D) conversion scheme. The A/D conversion scheme is simplified as the bandwidth sampling issues inherent in ac signal processing are avoided and in most drive designs, simultaneous sampling of the stator currents may not be necessary.

Hardware Peripheral for Standard Microcontroller and DSP Systems

The AD2S105 off-loads the time consuming Cartesian transformations from digital processors and benchmarks show a significant speed improvement over single processor designs. AD2S105 transformation time = 2 μ s.

Field Oriented Control of AC Motors

The AD2S105 accommodates all the necessary functions to provide a hardware solution for current conditioning in variable speed control of ac synchronous and asynchronous motors.

Three-Phase Imbalance Detection

The AD2S105 can be used to sense imbalances in a three-phase system via the homopolar output.

AD2S105—SPECIFICATIONS ($V_{DD} = +5\text{ V} \pm 5\%$; $V_{SS} = -5\text{ V} \pm 5\%$ AGND = DGND = 0 V; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted)

Parameter	Min	Typ	Max	Units	Conditions
SIGNAL INPUTS					
PH/IP1, 2, 3, 4 Voltage Level		± 2.8	± 3.3	V p-p	DC to 50 kHz
PH/IPH1, 2, 3 Voltage Level			± 4.25	V p-p	DC to 50 kHz
Input Impedance					
PH/IP1, 2, 3	7.5	10		k Ω	
PH/IPH1, 2, 3	13.5	18		k Ω	
PH/IP1, 4		1		M Ω	Mode 1 Only (2 Phase) Sin & Cos
Gain					
PH/IP1, 2, 3, 4	0.95	1	1.05		
PH/IPH1, 2, 3		0.56			
VECTOR PERFORMANCE					
3-Phase Input-Output					
Radius Error (Any Phase)		± 0.4	± 1	%	DC to 600 Hz
Angular Error ^{1,2}					
PH/IP		15	30	arc min	DC to 600 Hz
PH/IPH			30	arc min	DC to 600 Hz
Differential Nonlinearity			± 1	LSB	
Full Power Bandwidth		50		kHz	
Small Signal Bandwidth		200		kHz	
ANALOG SIGNAL OUTPUTS					
PH/OP1, 4					
Output Voltage ³		± 2.8	± 3.3	V p-p	PH/IP, PH/IPH INPUTS DC to 50 kHz
Offset Voltage		2	10	mV	Inputs = 0 V
Slew Rate		2		V/ μ s	
Small Signal Step Response		1		μ s	1° Input to Settle to ± 1 LSB (Input to Output)
Output Impedance		15		Ω	
Output Drive Current	3.0	4.0		mA	Outputs to AGND
Resistive Load	2			k Ω	
Capacitive Load		50		pF	
STROBE					
Write	100			ns	Positive Pulse
Max Update Rate		366		kHz	
BUSY					
Pulse Width		1.7	2.5	μ s	Conversion in Process
V_{OH}	4			V dc	$I_{OH} = 0.5\text{ mA}$
V_{OL}			1	V dc	$I_{OL} = 0.5\text{ mA}$
DIGITAL INPUTS					
DB1–DB12					
V_{IH}	3.5			V dc	
V_{IL}			1.5	V dc	
Input Current, I_{IN}			± 10	μ A	
Input Capacitance, C_{IN}		10		pF	
CONV MODE (CONV1, CONV2)					
V_{IH}	3.5			V dc	
V_{IL}			1.5	V dc	
Input Current			100	μ A	Internal 50 k Ω
Input Capacitance		10		pF	Pull-Up Resistor

Parameter	Min	Typ	Max	Units	Conditions
HOMOPOLAR OUTPUT HPOP-OUTPUT V_{OH} V_{OL} HPREF-REFERENCE	4	0.5	1	V dc V dc V dc	$I_{OH} = 0.5$ mA $I_{OL} = 0.5$ mA Homopolar Output-Internal $I_{SOURCE} = 25$ μ A and 20 k Ω to AGND
POWER SUPPLY V_{DD} V_{SS} I_{DD} I_{SS}	4.75 -5.25	5 -5	5.25 -4.75	V dc V dc mA mA	Quiescent Current Quiescent Current

NOTES

¹Angular accuracy includes offset and gain errors, measured with a stationary digital input and maximum analog frequency inputs.

²The angular error does not include the additional error caused by the phase delay as a function of input frequency. For example, if $f_{INPUT} = 600$ Hz, the contribution to the error due to phase delay is: 650 ns \times $f_{INPUT} \times 60 \times 360 = 8.4$ arc minutes.

³Output subject to input voltage and gain.

Specifications subject to change without notice.

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage (+ V_{DD} , - V_{SS}) ± 5 V dc $\pm 5\%$

Analog Input Voltage (PH/IP1, 2, 3, 4) 2 V rms $\pm 10\%$

Analog Input Voltage (PH/IPH1, 2, 3) 3 V rms $\pm 10\%$

Ambient Operating Temperature Range

Industrial (AP) -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

V_{DD} to AGND -0.3 V to +7 V dc

V_{SS} to AGND +0.3 V to -7 V dc

AGND to DGND ± 0.3 V dc

Analog Input Voltage to AGND V_{SS} to V_{DD}

Digital Input Voltage to DGND -0.3 V to $V_{DD} + 0.3$ V dc

Digital Output Voltage to DGND -0.3 V to $V_{DD} + V$ dc

Analog Output Voltage to AGND

. $V_{SS} - 0.3$ V to $V_{DD} + 0.3$ V dc

Analog Output Load Condition (PH/OP1, 4

Sin θ , Cos θ) 2 k Ω

Power Dissipation 140 mW

Operating Temperature

Industrial (AP) -40°C to +85°C

Storage Temperature -65°C to +150°C

Lead Temperature (Soldering, 10 sec) +300°C

CAUTION

1. Absolute Maximum Ratings are those values beyond which damage to the device will occur.
2. Correct polarity voltages must be maintained on the + V_{DD} and - V_{SS} pins

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD2S105 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Accuracy	Option*
AD2S105AP	-40°C to +85°C	30 arc min	P-44A

*P = Plastic Leaded Chip Carrier.

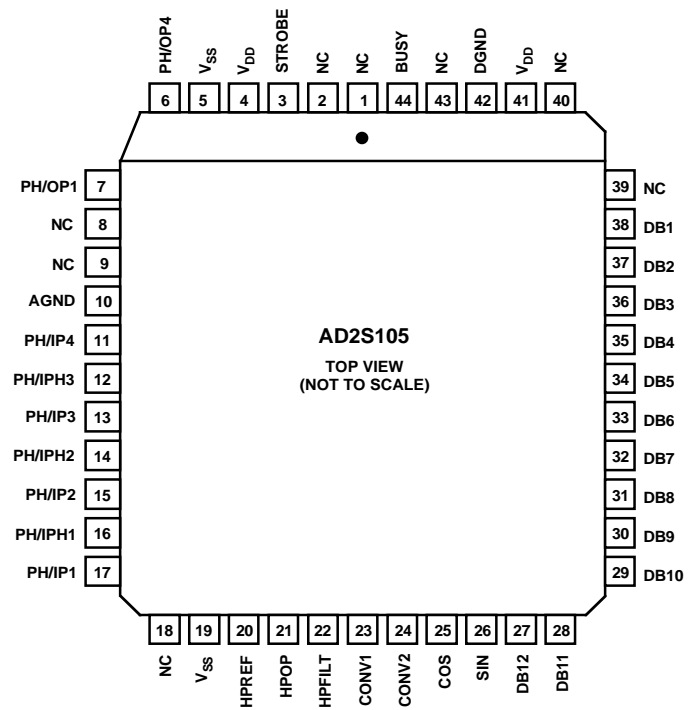


AD2S105

PIN DESIGNATIONS^{1, 2, 3}

Pin	Mnemonic	Description
3	STROBE	Begin Conversion
4	V _{DD}	Positive Power Supply
5	V _{SS}	Negative Power Supply
6	PH/OP4	Sin ($\theta + \phi$)
7	PH/OP1	Cos ($\theta + \phi$)
10	AGND	Analog Ground
11	PH/IP4	Sin θ Input
12	PH/IPH3	High Level Cos ($\theta + 240^\circ$) Input
13	PH/IP3	Cos ($\theta + 240^\circ$) Input
14	PH/IPH2	High Level Cos ($\theta + 120^\circ$) Input
15	PH/IP2	Cos ($\theta + 120^\circ$) Input
16	PH/IPH1	High Level Cos θ Input
17	PH/IP1	Cos (θ) Input
19	V _{SS}	Negative Power Supply
20	HPREF	Homopolar Reference
21	HPOP	Homopolar Output
22	HPFILT	Homopolar Filter
23	CONV1	Select Analog Input Format
24	CONV2	Select Analog Input Format
25	COS	Cos Output
26	SIN	Sin Output
27–38	DB12 to DB1	(DB1 = MSB, DB12 = LSB Parallel Input Data)
41	V _{DD}	Positive Power Supply
42	DGND	Digital Ground
44	BUSY	Internal Logic Setup Time

PIN CONFIGURATION



NC = NO CONNECT.

NOTES

¹90° orthogonal signals = Sin θ , Cos θ (Resolver) = PH/IP4 and PH/IP1.

²Three phase, 120°, three-wire signals = Cos θ , Cos ($\theta + 120^\circ$), Cos ($\theta + 240^\circ$).
= PH/IP1, PH/IP2, PH/IP3

High Level = PH/IPH1, PH/IPH2, PH/IPH3.

³Three Phase, 120°, two-wire signals = Cos ($\theta + 120^\circ$), Cos ($\theta + 240^\circ$) =
PH/IP2, PH/IP3.

In all cases where any of the input Pins 11 through 17 are not used, they must be left unconnected.

THEORY OF OPERATION

A fundamental requirement for high quality induction motor drives is that the magnitude and position of the rotating air-gap rotor flux be known. This is normally carried out by measuring the rotor position via a position sensor and establishing a rotor oriented reference frame.

To generate a flux component in the rotor, stator current is applied. A build-up of rotor flux is concluded which must be maintained by controlling the stator current, i_{ds} , parallel to the rotor flux. The rotor flux current component is the magnetizing current, i_{mr} .

Torque is generated by applying a current component which is perpendicular to the magnetizing current. This current is normally called the torque generating current, i_{qs} .

To orient and control both the torque and flux stator current vectors, a coordinate transformation is carried out to establish a new reference frame related to the rotor. This complex calculation is carried out by the AD2S105.

To expand upon the vector operator a description of a single vector rotation is of assistance. If it is considered that the moduli of a vector is OP and that through the movement of rotor position by ϕ , we require the new position of this vector it can be deduced as follows:

Let original vector $OP = A (\cos \theta + j \sin \theta)$ where A is a constant;

if $OQ = OP e^{j\phi}$ (1)

and: $e^{j\phi} = \cos \phi + j \sin \phi$

$$\begin{aligned}
 OQ &= A (\cos (\theta + \phi) + j \sin (\theta + \phi)) \\
 &= A [\cos \theta \cos \phi - \sin \theta \sin \phi + j \sin \theta \cos \phi + j \cos \theta \sin \phi] \\
 &= A [(\cos \theta + j \sin \theta) (\cos \phi + j \sin \phi)]
 \end{aligned}
 \tag{2}$$

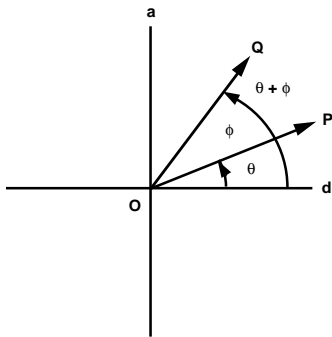


Figure 1. Vector Rotation in Polar Coordinate

The complex stator current vector can be represented as $i_s = i_{as} + ai_{bs} + a^2i_{cs}$ where $a = e^{j\frac{2\pi}{3}}$ and $a^2 = e^{j\frac{4\pi}{3}}$. This can be replaced by rectangular coordinates as

$$i_s = i_{ds} + ji_{qs} \tag{3}$$

In this equation i_{ds} and i_{qs} represent the equivalent of a two-phase stator winding which establishes the same magnitude of MMF in a three-phase system. These inputs can be seen after the three-phase to two-phase transformation in the AD2S105 block diagram. Equation (3) therefore represents a three-phase to two-phase conversion.

To relate these stator current to the reference frame the rotor currents assume the same rectangular coordinates, but are now rotated by the operator $e^{j\phi}$, where $e^{j\phi} = \cos \phi + j \sin \phi$.

Here the term vector rotator comes into play where the stator current vector can be represented in rotor-based coordinates or vice versa.

The AD2S105 uses $e^{j\phi}$ as the core operator. In terms of the mathematical function, it rotates the orthogonal i_{ds} and i_{qs} components as follows:

$$i_{ds}' + ji_{qs}' = (I_{ds} + jI_{qs}) e^{j\phi}$$

where i_{ds}' , i_{qs}' = stator currents in the rotor reference frame. And

$$e^{j\phi} = \cos \phi + j \sin \phi$$

$$= (I_{ds} + jI_{qs})(\cos \phi + j \sin \phi)$$

The output from the AD2S105 takes the form of:

$$i_{ds}' = I_{ds} \cos \phi - I_{qs} \sin \phi$$

$$i_{qs}' = I_{ds} \sin \phi + I_{qs} \cos \phi$$

The matrix equation is:

$$\begin{bmatrix} i_{ds}' \\ i_{qs}' \end{bmatrix} = \begin{bmatrix} \cos \phi & -\sin \phi \\ \sin \phi & \cos \phi \end{bmatrix} \begin{bmatrix} I_{ds} \\ I_{qs} \end{bmatrix}$$

and it is shown in Figure 2.

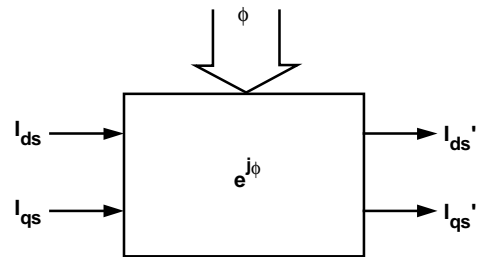


Figure 2. AD2S105 Vector Rotation Operation

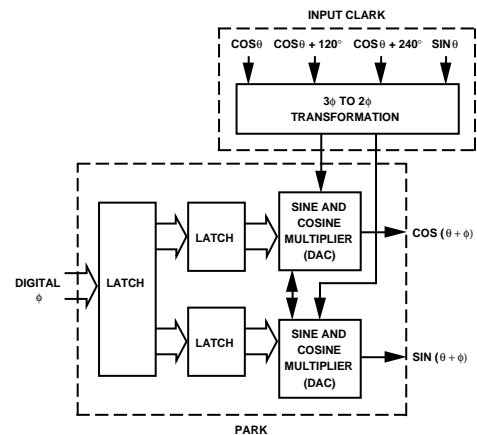


Figure 3. Converter Operation Diagram

AD2S105

CONVERTER OPERATION

The architecture of the AD2S105 is illustrated in Figure 3. The AD2S105 is configured in the forward transformation which rotates the stator coordinates to the rotor reference frame.

Vector Rotation

Position data, ϕ , is loaded into the input latch on the positive edge of the strobe pulse. (For detail on the timing, please refer to the “timing diagram.”) The negative edge of the strobe signifies that conversion has commenced. A busy pulse is subsequently produced as data is passed from the input latches to the Sin and Cos multipliers. During the loading of the multiplier, the busy pulse remains high preventing further updates of ϕ in both the Sin and Cos registers.

The negative edge of the busy pulse signifies that the multipliers are set up and the orthogonal analog inputs are then multiplied real time. The resultant two outputs are accessed via the PH/OP1 (Pin 7) and PH/OP4 (Pin 6).

For other configurations, please refer to “Transformation Configuration.”

CONNECTING THE CONVERTER

Power Supply Connection

The power supply voltages connected to V_{DD} and V_{SS} pins should be +5 V dc and -5 V dc and must not be reversed. Pin 4 (V_{DD}) and Pin 41 (V_{DD}) should both be connected to +5 V; similarly, Pin 5 (V_{SS}) and Pin 19 (V_{SS}) should both be connected to -5 V dc.

It is recommended that decoupling capacitors, 100 nF (ceramic) and 10 μ F (tantalum) or other high quality capacitors, are connected in parallel between the power line V_{DD} , V_{SS} and AGND adjacent to the converter. Separate decoupling capacitors should be used for each converter. The connections are shown in Figure 4.

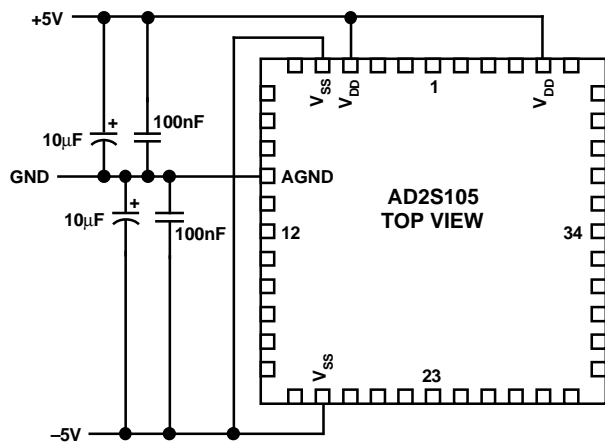


Figure 4. AD2S105 Power Supply Connection

ANALOG SIGNAL INPUT AND OUTPUT CONNECTIONS

Input Analog Signals

All analog signal inputs to AD2S105 are voltages. There are two different voltage levels of three-phase (0° , 120° , 240°) signal inputs. One is the nominal level, which is ± 2.8 V dc or 2 V rms and the corresponding input pins are PH/IP1 (Pin 17), PH/IP2 (Pin 15), PH/IP3 (Pin 13) and PH/IP4 (Pin 11).

The high level inputs can accommodate voltages from nominal up to a maximum of $\pm V_{DD}/V_{SS}$. The corresponding input pins are PH/IPH1 (Pin 16), PH/IPH2 (Pin 14) and PH/IPH3 (Pin 12). The homopolar output can only be used in the three-phase connection mode.

The converter can accept both two-phase format and three-phase format input signals. For the two-phase format input, the two inputs must be orthogonal to each other. For the three-phase format input, there is the choice of using all three inputs or using two of the three inputs. In the latter case, the third input signal will be generated internally by using the information of other two inputs. The high level input mode, however, can only be selected with three-phase/three-input format. All these different conversion modes, including nominal/high input level and two/three-phase input format can be selected using two select pins (Pin 23, Pin 24). The functions are summarized in Table I.

Table I. Conversion Mode Selection

Mode	Description	CONV1 (Pin 23)	CONV2 (Pin 24)
MODE1	2-Phase Orthogonal with 2 Inputs Nominal Input Level	NC	DGND
MODE2	3-Phase (0° , 120° , 240°) with 3 Inputs Nominal/High Input Level*	DGND	V_{DD}
MODE3	3-Phase (0° , 120° , 240°) with 2 Inputs Nominal Input Level	V_{DD}	V_{DD}

*The high level input mode can only be selected with MODE2.

MODE1: 2-Phase/2 Inputs with Nominal Input Level

In this mode, PH/IP1 and PH/IP4 are the inputs and the Pins 12 through 16 must be left unconnected.

MODE2: 3-Phase/3 Inputs with Nominal/High Input Level

In this mode, either nominal or high level inputs can be used. For nominal level input operation, PH/IP1, PH/IP2 and PH/IP3 are the inputs, and there should be no connections to PH/IPH1, PH/IPH2 and PH/IPH3; similarly, for high level input operation, the PH/IPH1, PH/IPH2 and PH/IPH3 are the inputs, and there should be no connections to PH/IP1, PH/IP2 and PH/IP3. In both cases, the PH/IP4 should be left unconnected. For high level signal input operation, select MODE2 only.

MODE3: 3-Phase/2 Inputs with Nominal Input Level

In this mode, PH/IP2 and PH/IP3 are the inputs and the third signal will be generated internally by using the information of other two inputs. It is recommended that PH/IP1, PH/IPH1, PH/IPH2, PH/IP4 and PH/IPH3 should be left unconnected.

Output Analog Signals

There are two sets of analog output from the AD2S105.

Sin/Cos orthogonal output signals are derived from the Clark/ three-to-two-phase conversion before the Park angle rotation. These signals are available on Pin 25 (Cos θ) and Pin 26 (Sin θ), and occur before Park angle rotation.

Two-Phase (Sin (θ + φ), Cos (θ + φ)) Signals

These represent the output of the coordinate transformation. These signals are available on Pin 6 (PH/OP4, Sin (θ + φ)) and Pin 7 (PH/OP1, Cos (θ + φ)).

HOMOPOLAR OUTPUT

HOMOPOLAR Reference

In a three-phase ac system, the sum of the three inputs to the converter can be used to indicate whether or not the phases are balanced.

If $V_{SUM} = PH/IP1 + PH/IP2 + PH/IP3$ (or $PH/IPH1 + PH/IPH2 + PH/IPH3$) this can be rewritten as $V_{SUM} = [Cosθ + Cos(θ + 120°) + Cos(θ + 240°)] = 0$. Any imbalances in the line will cause the sum $V_{SUM} \neq 0$. The AD2S105 homopolar output (HPOP) goes high when $V_{SUM} > 3 \times V_{ts}$. The voltage level at which the HPOP indicates an imbalance is determined by the HPREF threshold, V_{ts} . This is set internally at ± 0.5 V dc (± 0.1 V dc). The HPOP goes high when

$$V_{ts} < \frac{(Cosθ + Cos(θ + 120°) + Cos(θ + 240°))}{3} \times V$$

where V is the nominal input voltage.

With no external components V_{SUM} must exceed ± 1.5 V dc in order for HPOP to indicate an imbalance. The sensitivity of the threshold can be reduced by connecting an external resistor between HPOP and ground in Figure 5 where

$$V_{ts} = \frac{0.5 R_{EXT}}{R_{EXT} + 20,000}$$

R_{EXT} is in Ω.

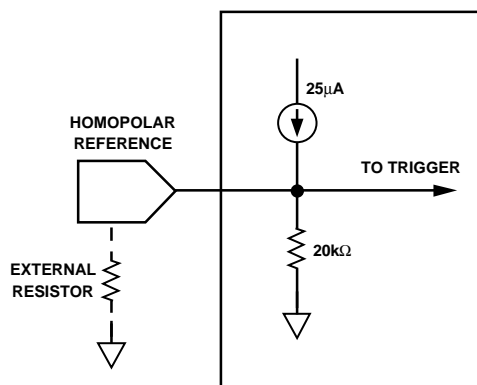


Figure 5. The Equivalent Homopolar Reference Input Circuitry

Example: From the equivalent circuit, it can be seen that the inclusion of a 20 kΩ resistor will reduce V_{ts} to ± 0.25 V dc. This corresponds to an imbalance of ± 0.75 V dc in the inputs.

Homopolar Filtering

The equation $V_{SUM} = Cosθ + Cos(θ + 120°) + Cos(θ + 240°) = 0$ denotes an imbalance when $V_{SUM} \neq 0$. There are conditions, however, when an actual imbalance will occur and the conditions as defined by V_{SUM} will be valid. For example, if the first phase was open circuit when $θ = 90°$ or $270°$, the first phase is valid at 0 V dc. V_{SUM} is valid, therefore, when $Cosθ$ is close to 0. In order to detect an imbalance θ has to move away from $90°$ or $270°$, i.e., when on a balanced line $Cosθ \neq 0$.

Line imbalance is detected as a function of HPREF, either set by the user or internally set at ± 0.5 V dc. This corresponds to a dead zone when $φ = 90°$ or $270° \pm 30°$, i.e., $V_{SUM} = 0$, and, therefore, no indicated imbalance. If an external 20 kΩ resistor is added, this halves V_{ts} and reduces the zone to $\pm 15°$. Note this example only applies if the first phase is detached.

In order to prevent this false triggering an external capacitor needs to be placed from HPFILT to ground, as shown in Figure 5. This averages out the perceived imbalance over a complete cycle and will prevent the HPOP from alternatively indicating balance and imbalance over $θ = 0°$ to $360°$.

For

$$\frac{dθ}{dt} = 1000 \text{ rpm } C_{EXT} = 220 \text{ nF}$$

$$\frac{dθ}{dt} = 100 \text{ rpm } C_{EXT} = 2.2 \text{ µF}$$

Note: The slower the input rotational speed, the larger the time constant required over which to average the HPOP output. Use of the homopolar output at slow rotational speeds becomes impractical with respect to the increased value for C_{EXT} .

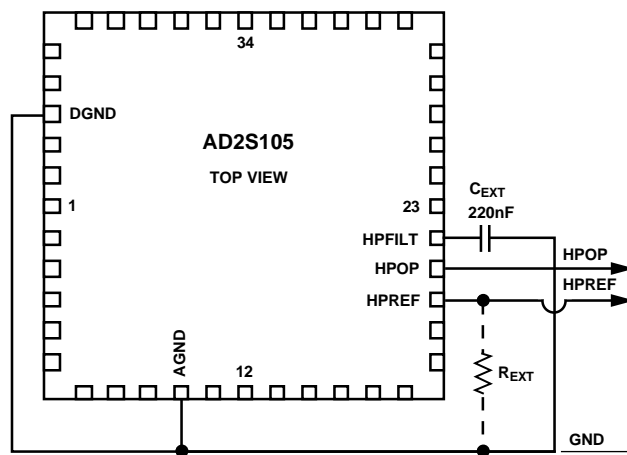


Figure 6. AD2S105 Homopolar Output Connections

AD2S105

TIMING DIAGRAMS

Busy Output

The BUSY output will go HI at the negative edge of the STROBE input. This is used to synchronize digital input data and load the digital angular rotation information into the device counter. The BUSY output will remain HI for 2 μ s, and go LO until the next strobe negative edge occurs.

Strobe Input

The width of the positive STROBE pulse should be at least 100 ns, in order to successfully start the conversion. The maximum frequency of STROBE input is 366 kHz, i.e., there should be at least 2.73 μ s from the negative edge of one STROBE pulse to the next rising edge. This is illustrated by the following timing diagram and table.

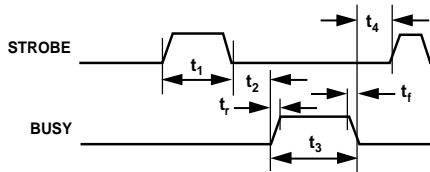


Figure 7. AD2S105 Timing Diagram

Note: Digital data should be stable 25 ns before and after positive strobe edge.

Table II. AD2S105 Timing Table

Parameter	Min	Typ	Max	Condition
t_1	100 ns			STROBE Pulse Width
t_2		30 ns		STROBE \downarrow to BUSY \uparrow
t_3	1.7 μ s		2.5 μ s	BUSY Pulse Width
t_4		100 ns		BUSY \downarrow to STROBE \uparrow
t_r		20 ns		BUSY Pulse Rise Time with No Load
		150 ns		BUSY Pulse Rise Time with 68 pF Load
t_f		10 ns		BUSY Pulse Fall Time with No Load
		120 ns		BUSY Pulse Fall Time with 68 pF Load

TYPICAL CIRCUIT CONFIGURATION

Figure 8 shows a typical circuit configuration for the AD2S105 in a three phase, nominal level input mode (MODE2).

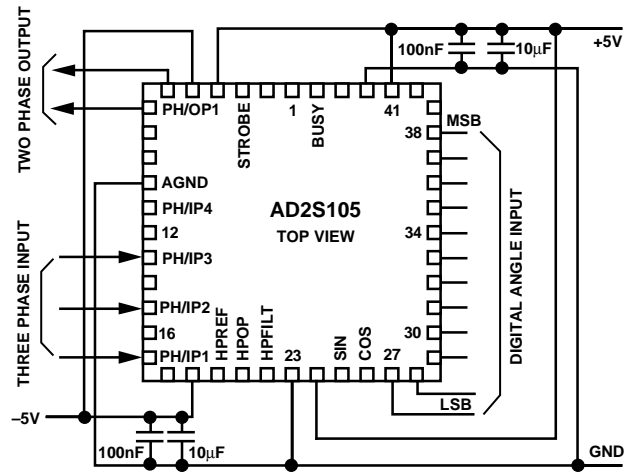


Figure 8. Typical Circuit Configuration

APPLICATIONS

Transformation Configuration

The AD2S105 can perform both forward and reverse transformations. The section "Theory of Operation" explains how the chip operates with the core operator $e^{+j\phi}$, which performs a forward transformation. The reverse transformation, $e^{-j\phi}$, is performed by providing a negative angle ϕ . Figure 9 shows two different phase input/output connections for AD2S105 reverse transformation operation.

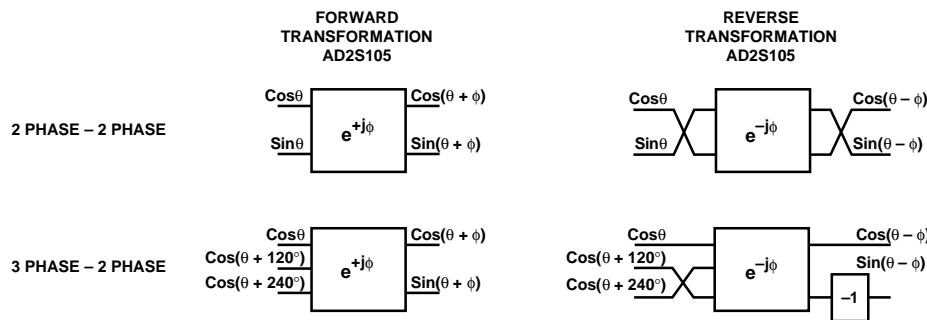


Figure 9. Forward and Reverse Transformation Connections

MEASUREMENT OF HARMONICS

In ac power systems, the quality of the electrical supply can be affected by harmonic voltages injected into the power main by loads, such as variable speed drive systems and computer power supplies. These harmonics are injected into other loads through the point of common coupling of the supply. This produces extra losses in power factor correction capacitors, power supplies and other loads which may result in failure. It also can result in tripping and failure of computer systems and other sensitive equipment. In ac machines the resultant harmonic currents and flux patterns produce extra motor losses and torque pulsations, which can be damaging to the load.

The AD2S105 can be used to monitor and detect the presence and magnitude of a particular harmonic on a three-phase line. Figure 10 shows the implementation of such a scheme using the AD2S105, where V_a, V_b, V_c are the scaled line voltages.

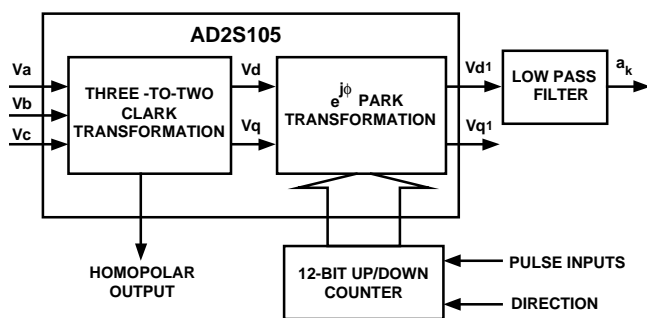


Figure 10. Harmonics Measurement Using AD2S105

Selecting a harmonic is achieved by synchronizing the rotational frequency of the park digital input, ϕ , with the frequency of the fundamental component and the integer harmonic selected. The update rate, r , of the counters is determined by:

$$r = 4096 \times \frac{n \times \omega}{2\pi}$$

Here, r = input clock pulse rate (pulses/second);
 n = the order of harmonics to be measured;
 ω = fundamental angular frequency of the ac signal.

The magnitude of the n -th harmonic as well as the fundamental component in the power line is represented by the output of the low-pass filter, a_k . In concert with magnitude of the harmonic the AD2S105 homopolar output will indicate whether the three

phases are balanced or not. For more details about this application, refer to the related application note listed in the bibliography.

Field Oriented Control of AC Induction Motors

In ac induction motors, torque is produced through interaction between the rotating air gap field and currents induced in the rotor windings. The stator currents consist of two components, the flux component which drives the air gap field, and the torque component which is reflected from the rotor windings. A successful field oriented control strategy must independently control the flux component of current, referred to as direct current (I_{ds}), and the torque producing component of stator current, referred to as quadrature current (I_{qs}).

The control architecture in Figure 11 is referred to as field oriented because the control algorithms performed on the ADSP-2105 processor operate on decoupled flux and torque current components in a reference frame relative to the rotor flux of the motor. The control algorithms provide fast torque response at any speed which results in superior dynamic performance, and consequently, load variations have minimal effect on speed or position control.

The AD2S90 resolver-to-digital converter is used to convert the modulated resolver position signals into a 12-bit digital position value. This value is brought into the ADSP-2105 via the serial port where the control algorithms calculate the rotor flux angle. The rotor flux angle is the sum of the rotor position and the slip angle. The relationship between the stator current frequency and the slip frequency can be summarized by the following formula:

$$f_{stat} = (\omega m \times (p/2)) + f_{slip}$$

where: f_{stat} = Stator Current Frequency (Hz)
 ωm = Mechanical Speed of the Motor (revs/sec)
 p = Number of poles
 f_{slip} = Slip Frequency (Hz)

The rotor flux angle is fed into the 12-bit position input of the AD2S105. The AD2S105 transforms the three ac stator currents using the digital rotor flux angle into dc values representing direct current (I_{ds}) and quadrature current (I_{qs}). The transformation of the ac signals into dc values simplifies the design of the A/D converter as it avoids the bandwidth sampling issues inherent in ac signal processing and in most cases eliminates the need for a simultaneous sampling A/D converter.

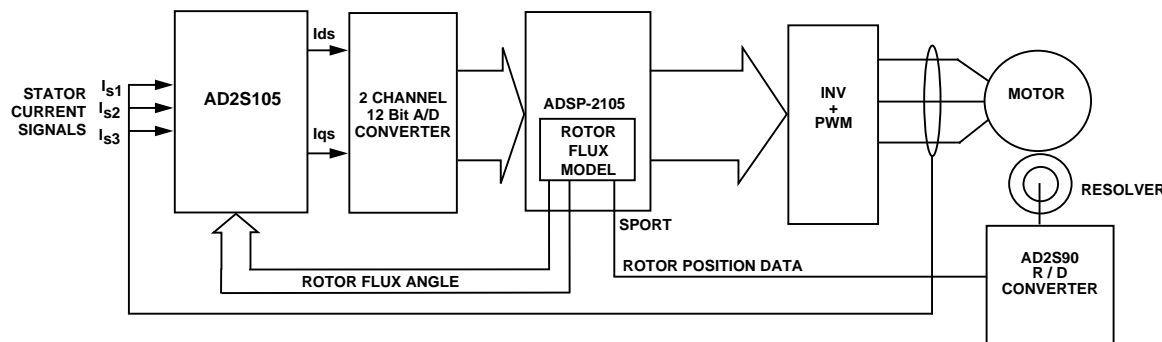


Figure 11. Field Oriented Control of AC Induction Motors

AD2S105

MULTIPLE POLE MOTORS

For multi-pole motor applications where a single speed resolver is used, the AD2S105 input has to be configured to match the electrical cycle of the resolver with the phasing of the motor windings. The input to the AD2S105 is the output of a resolver-to-digital converter, e.g., AD2S80A series. The parallel output of the converter needs to be multiplied by 2^{n-1} , where n = the number of pole pairs of the motor. In practice this is implemented by shifting the parallel output of the converter left relative to the number of pole pairs. This will work for motors with a binary number of pole pairs.

Figure 12 shows the generic configuration of the AD2S80A with the AD2S105 for a motor with n pole pairs. The MSB of the AD2S105 is connected to MSB-($n-1$) bit of the AD2S80A digital output, MSB-1 bit to MSB-($n-2$) bit, etc.

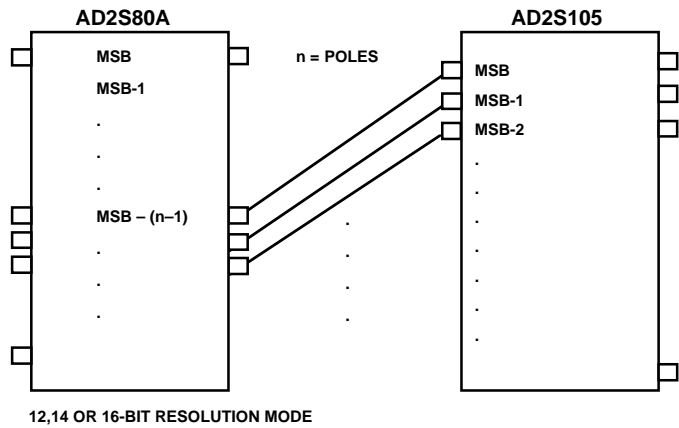


Figure 12. A General Consideration in Connecting R/D Converter and AD2S105 for Multiple Pole Motors

Figure 13 shows the AD2S80A configured for use with a four pole motor, where $n = 2$. Using the formula described the MSB is shifted left once.

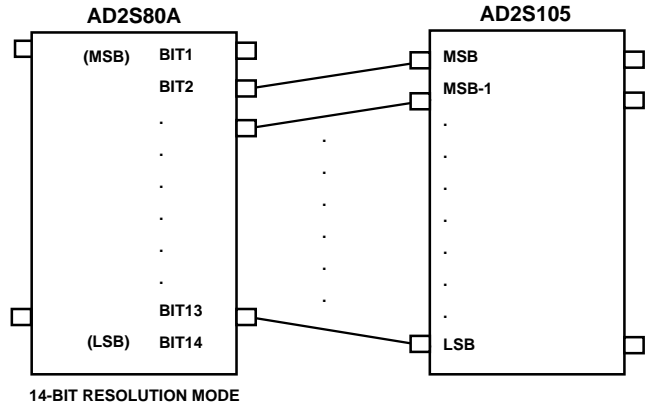


Figure 13. Connecting of R/D Converter AD2S80A and AD2S105 for Four-Pole Motor Application

APPLICATION NOTES LIST

1. "Vector Control Using a Single Vector Rotation Semiconductor for Induction and Permanent Magnet Motors," by F.P. Flett, Analog Devices.
2. "Silicon Control Algorithms for Brushless Permanent Magnet Synchronous Machines," by F.P. Flett.
3. "Single Chip Vector Rotation Blocks and Induction Motor Field Oriented Control," by A.P.M. Van den Bossche and P.J.M. Coussens.
4. "Three Phase Measurements with Vector Rotation Blocks in Mains and Motion Control," P.J.M. Coussens, et al.
5. "A Tutorial in AC Induction and Permanent Magnet Synchronous Motors—Vector-Control with Digital Signal Processors."

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

44-Lead Plastic Leaded Chip Carrier (P-44A)

