ADV601 VideoLAB User's Guide

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Table of Contents

VideoLAB Contents

- ADV601 VideoLAB PCI board
- 4-pin DIN to BNC color coded breakout cable (required for RGB component analog video output only)
- ADV601 VideoLAB CD-ROM with cover and “liner notes”
- ADV601 Low Cost Multi-Format Video CODEC Datasheet
- ADV601 VideoLAB User’s Guide (this document)
- FOR THE BEAUTY VHS cassette

Optional Contents: 10-bit CCIR656 Video I/O

- CCIR656 ECL interface ISA board
- 20 position gray ribbon cable for CCIR656 ECL interface board
- IN and OUT 25-pin D-shell breakout cable for CCIR656 ECL interface board with two removable gender changers

Host System Requirements

- Microsoft Windows 95
- A Pentium 90 MHz processor or better
- Intel Triton motherboard chipset and PCI BIOS
- One short card PCI slot
- 16MB of RAM
- 600 MB of Hard Drive space (for storing compressed video clips)
- Any speed CD-ROM drive
- Optional: One short card ISA slot for optional ECL CCIR656 interface board

  Note: The ECL CCIR656 interface board only uses the ISA slot for power and mechanical connections—there are no signal connections to the ISA bus.

- Preferred: Sound Card with CD-Audio playback
- Preferred: Microsoft Video for Windows 1.1e and Adobe Premier 4.1

Optional Tools Required for Rebuilding Drivers and Applications

- Microsoft Visual C++ Version 2.2
- Microsoft Win32 Software Development kit final release Version 3.1
- Microsoft Windows 95 Device Driver Kit (DDK) October 1995 Version
- VToolsD from Vireo Software
- Microsoft Windows 95
- Optional: AMCC “PCI Matchmaker Developer’s Kit”

Note: AMCC "PCI Matchmaker Developer's Kit" Software from AMCC of San Diego, CA will only be required for those changing the definition of the VideoLAB *PCI configuration space.*

Suggested Video Equipment

- VCR and color video monitor with CCIR624/RS-170 analog composite, analog Y/C video, or analog RGB input (PAL or NTSC)
- LaserDisc, VCR, camcorder, or camera with CCIR624/RS-170 analog composite or analog Y/C video output (PAL or NTSC)
- Optional: professional video equipment with CCIR656/SMPTE125M 10-bit parallel digital video interfaces

VideoLAB Installation

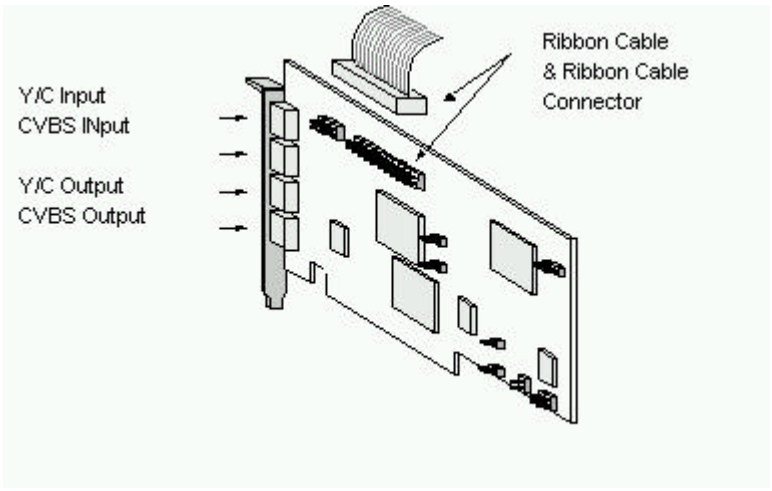
Please follow all installation directions found on CD-ROM Liner notes.

Jumper Settings and Test Points

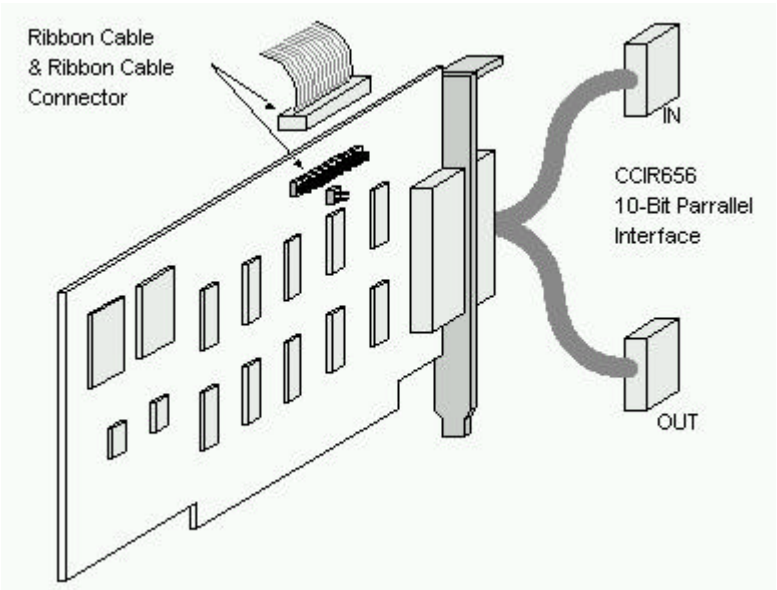
Jumper	Function	Usage	Typical Setting	Alternate Setting
JP3	Video Clock Source	Used to select between SAA7111 line-locked clock source (1-2 short) for ADV601 or CCIR656 digital video clock source (2-3 short) for ADV601.	1-2 short when input video is composite or Y/C.	2-3 short when ECL CCIR656 interface board is used and valid CCIR656 digital input is present.
JP13	75 Ω Video Input terminator	When shorted provides 75 Ω termination to composite and Y/C inputs. Pins 5-6 Composite Pins 1-2 & 3-4 Y/C	Short 1-2, 3-4, 5-6 to terminate composite and Y/C Inputs.	Open when T-tap 75 Ω cable is used for pass-thru connections.
JP14 & JP15	Test Points	JP14 Pin 1 SAA7111 analog video pass-through JP15 Pin 1 SAA7111 Hsync JP15 Pin 2 SAA7111 Vsync	n/a	n/a

Ribbon Cable Installation Diagram

Please see the written comments about ribbon cable installation and orientation in the CD-ROM liner notes.



ADV601 VideoLAB PCI Board

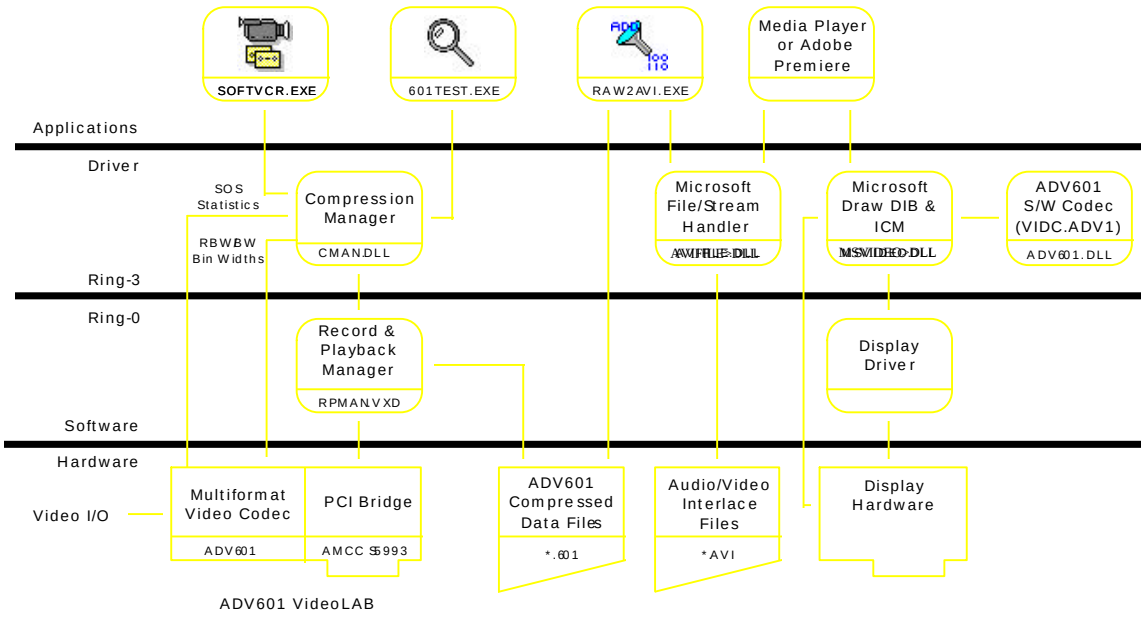


CCIR656 ECL Interface ISA Board w/ D-Shell Breakout Cable

VideoLAB Software

Software Architecture

The software for VideoLAB consists of three applications and three drivers. All of the necessary source code files and make files required for rebuilding these applications and drivers are included in the associated CD-ROM.



Application: (SOFTVCR.EXE) “SoftVCR”

Button	Function
I/O	Clicking on this button results in the input/output configuration dialog box being displayed. From this dialog box Video Input source, RGB Component Analog Video Output (CAV) , NTSC/PAL Video Formats, and Compression ratio options can be selected.
Cassette Door “Push to Load”	Clicking on this button produces a Windows 95 file browser. From this browser *.601 files for playback or record (capture) can be selected. It is analogous to selecting a video cassette to record to or playback from. *Remember: Just as you can record over you favorite video cassette -- you can record over files you intend for playback only. Be careful.*

Play	Clicking here plays the selected *.601 file back. CCIR624 compliant analog video output is simultaneously available on both the lowermost composite BNC and lowermost Y/C 4-pin DIN output connectors of the VideoLAB board. Users can manually select RGB component analog video (CAV) via the I/O then Video Output buttons. A special cable converts the lowermost outputs to 3 BNCs. CCIR656 compliant 4:2:2 10-bit parallel digital video is available on the 25-pin D-shell connector labeled OUT (metallic shroud) when the optional ECL CCIR656 interface board is used. The video output is automatically generated in the same format it was captured in whether PAL or NTSC. Users in Japan will have to manually remove the 7.5 IRE pedestal from analog video via the I/O then Video Format Dialog box by clicking on the “Japan” radio button.
Stop/Eject	Clicking this button during play or record (capture) stops video playback or record (capture). Clicking this button when playback or record is not happening “empties” the selected file -- a new file needs to be selected via the cassette door.
Record	Clicking here starts the recording (capturing) of video from the selected source into the selected *.601 file. CCIR624 compliant analog video can be recorded from the uppermost composite BNC input or the uppermost Y/C 4-pin DIN input of the VideoLAB board. Or, CCIR656 compliant 4:2:2 10-bit parallel digital video is available from the 25-pin D-shell connector labeled IN (black plastic shroud) when the optional ECL CCIR656 interface board is used. A VideoLAB jumper must be set properly to select this input. Users can manually select which input is selected via the I/O then Video Input dialog. Selected source video is instantly passed through to all of the video outputs for monitoring.
Pause	Clicking here pauses playback of a *.601 file only.
Power	Clicking here forces an exit from SoftVCR.
Clock	During playback and record (capture) this display shows the VITC time code down to field resolution..

I/O >> Video In	clicking on this results in a dialog allowing the selection of the video source for recording (capturing) or monitoring. Sources include: • CCIR624 compliant analog video from the uppermost composite BNC input of the VideoLAB board via the Philips SAA7111. • Analog Y/C video from the uppermost Y/C 4-pin DIN input of the VideoLAB board via the Philips SAA7111. • CCIR656 compliant 4:2:2 10-bit parallel digital video from the 25-pin D-shell connector labeled IN (black plastic shroud) when the optional ECL CCIR656 interface board is used. A VideoLAB jumper must also be set properly to select this input. The LineLocked check box should be checked when Analog video is being sourced from an unreliable source like a VCR or camcorder. Checking this box directs the SAA7111 to perform its most robust Line-Locking.
I/O >> Video Out	Clicking on this allows the user to select between: Three simultaneous video outputs: 1. CCIR624 compliant analog composite video on the lowermost BNC connector processed by the ADV7175; 2. analog Y/C video on the lowermost 4-pin DIN connector processed by the ADV7175; 3. CCIR656 complaint parallel 10-bit digital component video (D1) on the 25-pin D-shell connector labeled OUT (metallic shroud). Or two simultaneous video outputs: 1. RGB component analog video (CAV) with embedded Sync on the lowermost BNC connector (Blue) and the lowermost 4-pin DIN connector (Red/Green) processed by the ADV7175. A special cable adapter converts the 4-pin DIN to two BNCs (these are color coded Red and Green); 2. CCIR656 complaint parallel 10-bit digital component video (D1) on the 25-pin D-shell connector labeled OUT (metallic shroud). Please note that D1 4:2:2 10-bit digital component video is only accessible when the CCIR656 ECL interface board is used.
I/O >> Video Format	Clicking on this allows the user to manually select between PAL and NTSC video format. Please note that D1 4:2:2 10-bit digital component video is only accessible when the CCIR656 ECL interface board is used. When Composite or Y/C video is selected as input, NTSC/PAL format determination occurs automatically through support of the SAA7111.

I/O >> Compression	Clicking on this allows the user to manually select the compression ratio of recorded (captured) video. This data rate can be specified as compression ratio or bits per pixel (bpp). Each pixel of uncompressed 4:2:2 10-bit digital component video is 20 bits in size (i.e. 20 bits per pixel or 20 bpp). For the VideoLAB board this is the standard reference used even when Y/C or composite video is digitized by the 8-bit SAA7111. For reference, the data rate for the active portion of uncompressed 10-bit CCIR601 video is: 26.2 Mbytes/second for NTSC 25.9 Mbytes/second for PAL For example, if an NTSC video source was compressed with a compression ratio of 20 down to 1 bpp the resulting compressed video data rate would be 1.31 Mbytes/second.

Application: (RAW2AVI.EXE) "RAW2AVI"

The SoftVCR will only capture and playback `*.601` compressed video files. In order to use Video-for-Windows compliant software tools from other vendors (like Adobe Premiere and Media Player) `*.601` files must be translated to `*.avi` files. The `raw2avi` utility will perform this function.

Application: (601TEST.EXE) 601TEST Diagnostics

The 601TEST application is a "no frills" DOS BOX application only. It is intended to offer the user of the ADV601 VideoLAB low level test and diagnostic support for the four main chips found on the VideoLAB board. These chips are ADV601, AMCC PCI interface chip, Philips SAA7111 video decoder, and ADV7175.

Driver: (601CMAN.DLL) ADV601 Compression Manager and Bin Width Calculator

This is a 32-bit Windows 95 ring 3 dynamic linked library. The primary purpose of this driver is to provide Bin Width and bit rate control calculation support for the ADV601. It also provides a thin wrapper to the supporting 601RPMAN.VXD ring 0 driver.

Driver: (601RPMAN.VXD) ADV601 Record and Playback Manager

This is a 32-bit Windows 95 ring 0 VxD. The primary purpose of this driver is to control hardware and provide high rate disk access for compressed video data.

Driver: (ADV601.DLL) ADV601 Software CODEC

As part of the normal software installation procedure, an ADV601 compatible software CODEC is automatically installed. Since this software CODEC is Video-for-Windows compliant, any Video for Windows compliant application can use this CODEC. Please note that `*.601` files must first be translated to `*.avi` files using RAW2AVI.EXE.

The Four Character Code identifying the ADV601 software CODEC to Video for Windows is "ADV1". The system.ini will include **`VIDC.ADV1=ADV601.DLL`** *to show proper installation of software CODEC.*

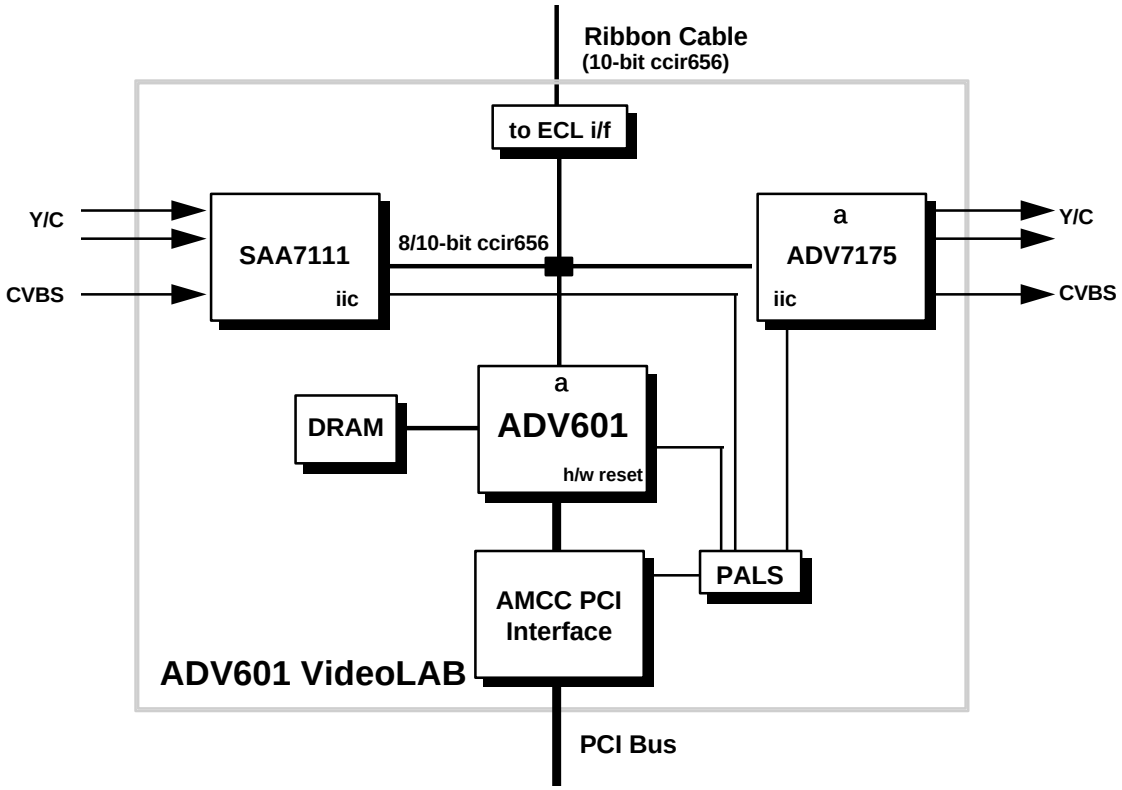
ADV601 Presets for Adobe Premiere

20 Premiere preset files are automatically copied into the `premiere/plugins` sub-directory on install from the CD-ROM.

These files give the user of Adobe Premiere convenient working image sizes and compression presets to work with when using the ADV601 software CODEC. Selection between PAL and NTSC resolutions and field rates is also provided. Please note, even when non-full resolution image sizes are selected as presets, all compressed data files will be compatible with the full image sizes of the ADV601 hardware. That is, any compressed file read or produced by the ADV601 software CODEC can be streamed to the ADV601 (after translation back to `*.601` format) and produce a full resolution image.

This seeming inconsistency can exist because of the scaleable nature of the ADV601 compression algorithm. In fact, within one compressed data stream, multiple nested resolutions exist. So, even though the ADV601 compressed data stream is always a full resolution data stream, embedded within that data stream is a complete set of resolutions. These supported resolutions are FULL, CIF, QCIF, QQCIF, and QQQCIF.

ADV601 VideoLAB Block Diagram



PCI Configuration Space for ADV601 VideoLAB

Access to PCI configuration space for ADV601 VideoLAB is performed through PCI BIOS functions and Microsoft Plug and Play extensions.

PCI Device Identification can be made through the use of five hard-coded values in the configuration space. For the ADV601 VideoLAB, these are the following:

- Vendor ID: 0x11D4 (for all Analog Devices PCI Components)
- Device ID: 0x0601 (for ADV601 VideoLAB)
- Revision ID: 0x13 (for this rev—may change in the future)
- Header Type: 0x00 (typical for PCI agents)
- Class Code: 0x040000 (Multi-Media base class, Video Subclass, 0x00 for programming interface)

With this information, the ADV601 VideoLAB board can be found, configured and subsequently accessed.

offset address	byte 3	byte 2	byte 1	byte 0	
0x0	**Device 0x06**	**ID 0x01**	**Vendor 0x11**	**ID 0xD4**	
0x4	Status		Command		
0x8	**class 0x04**	**code 0x00**	**0x00**	**Rev ID 0x13**	
0xc	BIST	**Header Type 0x00**	Latency Timer	Cache Line Sz	
0x10	Base	Address	0		*AMCC Operation Registers*
0x14	Base	Address	1		ADV601 Indirect Address (Mem)
0x18	Base	Address	2		ADV601 Indirect Data (Mem)
0x1c	Base	Address	3		ADV601 Compressed Data (Mem)
0c20	Base	Address	4		ADV601 Interrupt Mask/Status & ADV7175/SAA7111 via IIC & ADV601 h/w reset (Mem)
0x24	not	used			
0x28	not	used			
0x2c	not	used			
0x30	Expansion	ROM	Base	Address	not used
0x34	not	used			
0x38	not	used			
0x3c	max lat	min gnt	**interrupt pin 0x01**	**interrupt line (0xFF)**	Interrupt pin INTA~ Interrupt line selected by Plugn'Play

PCI Configuration Space for ADV601 VideoLAB

The configuration space Base Address Registers have been partially set up by Analog Devices to allow memory-mapped access to all ADV601 registers.

Microsoft Windows Plug and Play will complete the setup of configuration space by assigning the actual physical base address values to the Base Address Registers upon system power-up.

> *Plug and Play is responsible for assuring that the assigned address values will not interfere with other devices in the system.*

ADV601 driver software (601cman.dll and 601rpman.vxd) will read the base address values from the configuration space to determine which physical memory spaces are used for ADV601 register access.

AMCC Operational Registers

BaseAddressRegister0 is reserved for the AMCC interface chip for accesses of its own operational registers. The reader is directed to the relevant AMCC documentation for information about these registers. A programmer interested in controlling ADV601 functionality should only need access to the AMCC Interrupt Control/Status register and the Bus Master Control and Status registers.

Byte Address	byte 3	byte 2	byte 1	byte 0
Base Address Register0+0x38	**AMCC**	**Interrupt**	**Control/Status**	**Register**

PCI Memory Space: ADV601 Registers

All ADV601 operations are controlled though the ADV601 registers. All of these registers are memory-mapped onto the PCI bus through the AMCC S5933 interface chip. There are no I/O mapped ADV601 operations.

BaseAddressRegister1 is used to access the ADV601 Indirect Address Register.

Memory Byte Address	byte 3	byte 2	byte 1	byte 0
Base Address Register1 + 0x0 *through* Base Address Register1 + 0x3ff			**Indirect**	**Address**

BaseAddressRegister2 is used to access ADV601 Indirect Data Registers. Please note that since successive reads/writes to the Indirect Data Registers results in auto-incrementing of the Indirect Address Register, successive reads to any part of the memory-mapped space defined below results in auto-incrementing of the indirect address. The result is that entire vectors of indirect register data (like BWs) can be read/written to the indirect data memory space via burst writes and reads.

Memory Byte Address	byte 3	byte 2	byte 1	byte 0
Base Address Register2 + 0x0 *through* Base Address Register2 + 0x3FF			**Indirect**	**Data** ***(as indexed by Indirect Address)***

BaseAddressRegister3 is used to access the ADV601 Compressed Data Register. Please note that since successive reads/writes to the Compressed Data Register results in auto-advancing of compressed data through the 512x32 on-chip FIFO, successive reads to any part of the memory-mapped space defined below results in accesses of the FIFO. The net result is that entire vectors of compressed data can be read/written to the indirect data memory space via burst writes and reads.

Memory Byte Address	byte 3	byte 2	byte 1	byte 0
Base Address Register3 + 0x0 *through* Base Address Register3 + 0x3FFFF	**Compressed**	**Data**	**Register**	

BaseAddressRegister4 is used to access ADV601 Interrupt Mask/Status Register. Please note that only the lower 16 bits of this address space should be used for Interrupt Mask/Status Register. The upper 8 bits of this space is reserved for IIC bus access and ADV601 h/w resets (described below).

Programmers should be careful in accessing the Interrupt Mask/Status register since it is easy to disturbed the IIC bus and the h/w reset pin of the ADV601.

Memory Byte Address	byte 3	byte 2	byte 1	byte 0
Base Address Register4 + 0x0 *through* Base Address Register4 + 0x3FF	**IIC access to ADV7175 and SAA7111**		**Interrupt**	**Mask/Status**

PCI Memory Space: ADV7175/SAA7111 Access & ADV601 h/w Reset

In addition to ADV601 interrupt Mask / Status access, **BaseAddressRegister3** is used to access the ADV7175 video encoder IIC port, SAA7111 video decoder IIC port and ADV601 h/w reset pin. Please note that only the upper 8 bits of this address space should be used for IIC and h/w reset The lower 16 bits of this space reserved for Interrupt Mask/Status register.

Programmers should be careful not to inadvertently change Interrupt Mask/Status register.

Memory Byte Address	byte 3	byte 2	byte 1	byte 0
Base Address Register3 + 0x0 *through* Base Address Register3 + 0x3FF	**IIC access to ADV7175 and SAA7111** (see below)		**Interrupt**	**Mask/Status**

On writes, byte 3 is defined as follows:

bit 0	**SDA data output value**
bit 1	**SDA output enable (set high to drive)**
bit 2	**SCL output value**
bit 3	**SCL output enable (set high to drive)**
bit 4	**ADV601 reset (0 -- reset; 1 -- run)**
bit 5	undf
bit 6	undf
bit 7	**Bus Master Mode enable**

On reads, byte 3 is defined as follows:

bit 0	**SDA data input value**
bit 1	undf
bit 2	**SCL input value**
bit 3	undf
bit 4	undf
bit 5	undf
bit 6	undf
bit 7	undf

PCI Interrupts: Interrupt Pin & Interrupt Line

The ADV601 generates one physical interrupt from multiple logical sources (see the ADV601 Datasheet). PALs on the ADV601 VideoLAB board translates this ADV601 physical interrupt into a PCI INTA~ interrupt by producing a phantom Mailbox write to AMCC PCI incoming mailbox location 4 byte 3.

The Interrupt Pin Configuration space register is set to 0x01 by Analog Devices indicating that INTA~ is used and Interrupt Line Register is set to 0xFF indicating that the routing of this interrupt to the host's 8259 interrupt controller is unknown prior to powerup.

Microsoft Windows Plug and Play will complete the set up of configuration space by assigning the actual interrupt line (0-15) to the interrupt line register upon system powerup.

Plug and Play is responsible for assuring that the assigned interrupt line will not interfere with other devices in the system. Given the small number of interrupts supported by the standard PC conflicts are not rare.

ADV601 driver software (601cman.dll and 601rpman.vxd) will read the interrupt line from the configuration space to determine which physical 8259 interrupt is used by the ADV601.