# Video Decoder with 9-Bit ADC, 3-Line Adaptive Comb Filter & Scaler

**Preliminary Technical Data** — **ADV7183**

**FEATURES**

- Analog Video to Digital YUV Video Decoder
  - NTSC-(M/N), PAL-(B/D/G/H/I/M/N)
- Integrates Two 9-Bit Accurate ADCs
- Clocked from a Single 27 MHz Crystal
- Dual Video Clocking Schemes
  - Line Locked Clock Compatible (LLC)
  - Fixed Frequency Oversamping 10-Bit Operation
- Adaptive-Digital-Line-Length-Tracking (ADLLT™)
- Real Time Clock & Status Information Output
- Integrated AGC (Automatic Gain Control) & Clamping
- Simplified Digital Interface
- On-Board Digital FIFO
- Optimised Programmable Video Source Modes
  - Broadcast TV
  - VCR/Camcorder
  - Security/Surveillance
- Multiple, Programmable Analog Input Formats:
  - CVBS (Composite Video)
  - SVHS (Y/C
- 4 Analog Input Video Channels
- Real Time Horizontal and Vertical Scaling
- Adaptive 3-Line Luma and Chroma Comb Filter
- Automatic NTSC/PAL Identification
- VMI & VIP compliant video pixel port
- Digital Output Formats (16-Bit Wide Bus):
  - YCrCb (4:2:2 or 4:1:1)
  - CCIR601/CCIR656 8-Bit
- 0.5V to 2.0V pk-pk i/p range
- Differential Gain < 1%
- Differential Phase < 1°
- Programmable Video Controls
  - Pk-White/Hue/Brightness/Saturation/Contrast
- CCIR/Square Pixel Operation
- Integrated On-Chip Video Timing Generator
- Synchronous or Asynchronous Output Timing
- Line Locked Clock Output
- Close Captioning Passthrough Operation
- Vertical Blanking Interval Support
- Power Down Mode
- 2-Wire Serial MPU Interface ($I^2C$ Compatible)
- +5V/+3V CMOS Supply Operation
- 80-Pin LQFP Package

**APPLICATIONS**

- Video Conferencing
- Hybrid Analog/Digital Set Top Boxes
- PC Video/Multimedia
- Camcorders
- Security Systems/Surveillance



**GENERAL DESCRIPTION**

The ADV7183 is an integrated video decoder that automatically recognises and converts a standard analog baseband television signal compatible with world wide standards NTSC or PAL into 4:2:2 or 4:1:1 component video data compatible with 16-bit/8-Bit CCIR601/CCIR656 8-Bit standards.

The advanced and highly flexible digital output interface enables perfomance video decoding and conversion in both frame-buffer based and line locked clock based systems. This makes the device ideally suited for a broad range of applications with diverse analog video characteristics including tape based sources, broadcast sources, secruity/surveillance cameras and professional systems.

Fully integrated line stores enable 3-line comb filtering in both luminance and chrominance data paths, plus real time horizontal and vertical scaling of captured video down to icon size. The 9-bit accurate A/D conversion provides professional quality SNR performance. This allows true 8-bit resolution in the 8-bit output mode.

The 4 analog inputs channel accept standard composite or S-Video video signals in an extensive number of combinations. AGC and Clamp Restore circuitry allow an input video signal peak to peak range of 0.5V up to 2V. Alternatively these can be bypassed for manual settings.

The fixed 27 MHz clocking of the ADCs and datapath for all modes allows very precise and accurate sampling and digital filtering. The Line Locked Clock output allows the output data rate, timing signals and output clock signals to be synchronous, asynchronous or line locked even with +/-5% line length variation. The output control signals allow glueless interface connection in almost any application.

The ADV7183 modes are set up over a two wire serial bidirectional port ($I^2C$ compatible).

The ADV7183 is fabricated in a +5V CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation.

The ADV7183 is packaged in a small 80 pin LQFP package.

Rev . PrA 05/99



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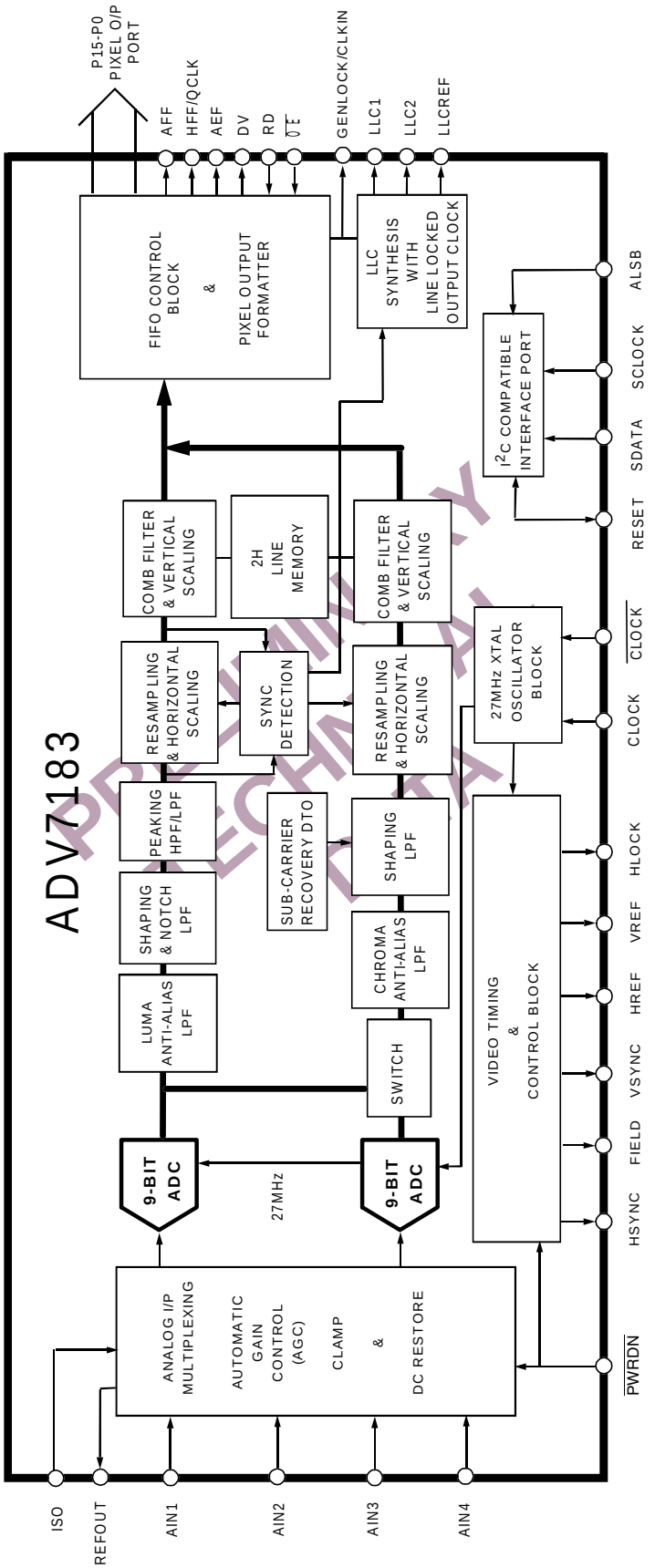



**FUNCTIONAL BLOCK DIAGRAM**

**PIN DESCRIPTION**

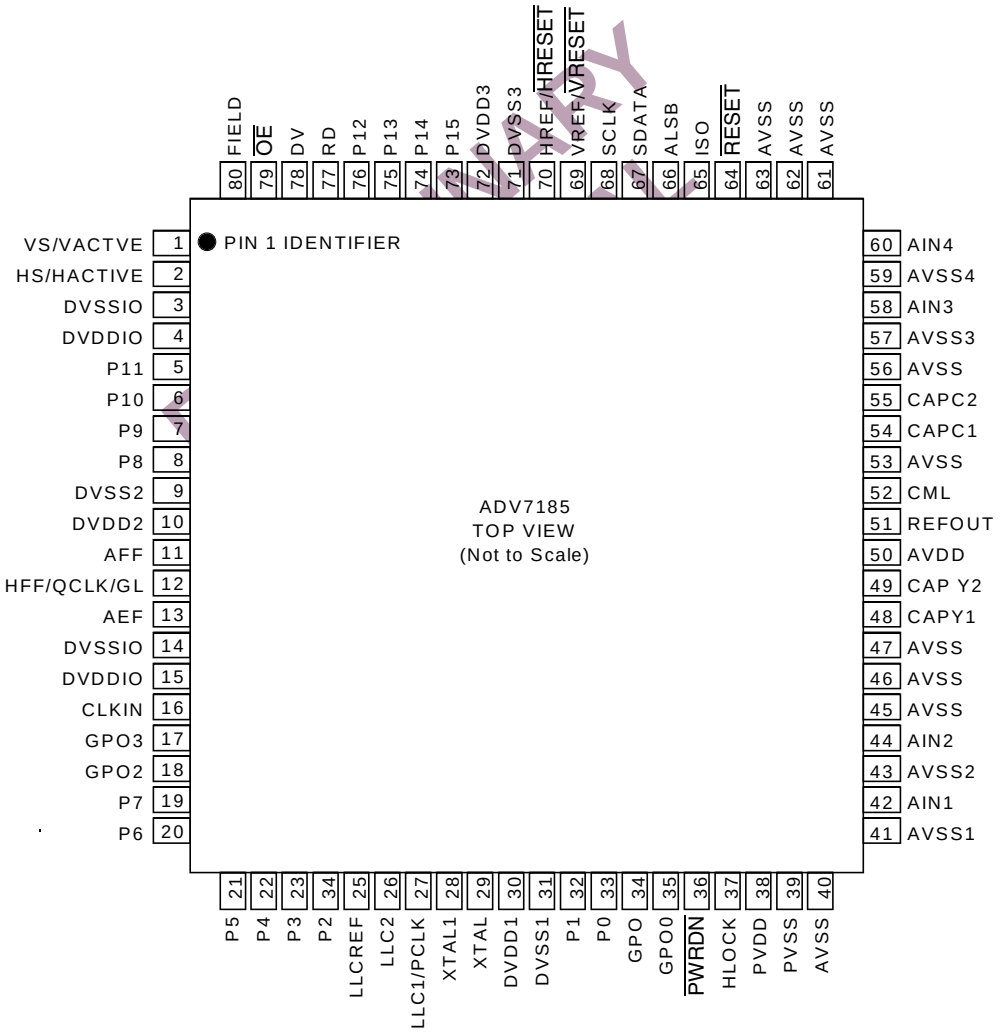
| Mnemonic | Input/Output | Function |
|---|---|---|
| P15-P0 | O | 8-Bit Multiplexed YCrCb Pixel Port (P7-P0), 16-Bit YCrCb Pixel Port (P15-P0). |
| GPO0-3 | O | GP0[0:3] general purpose output pins. |
| XTAL | I | Input terminal for 27MHz crystal oscillator or connection for external oscillator with CMOS compatible square wave clock signal |
| XTAL1 | 0 | Second terminal for crystal oscillator; not connected if external clock source is used |
| DVSS1-3 | G | Ground for Digital supply |
| DVDD1-3 | P | Digital Supply Voltage (+5V) |
| DVDDIO | P | Digital I/O supply Voltage (+5V/+3.3V) |
| DVSSIO | G | Digital I/O ground |
| AVSS | G | Ground for Analog Supply |
| AVDD | P | Analog Supply Voltage (+5V) |
| AVSS1-4 | G | Analog Input Channels ground |
| PVSS | G | PLL Supply Ground |
| PVDD | P | PLL Supply Voltage (+5V) |
| AIN1-4 | I | Video Analog Input Channels |
| SCLOCK | I | MPU Port Serial Interface Clock Input. |
| SDATA | I/O | MPU Port Serial Data Input/Output. |
| ALSB | I | TTL Address Input, it selects the MPU address;<br>MPU address = 88H ALSB = 0<br>MPU address = 8AH ALSB = 1 |
| RD | I | Asynchronous FIFO Read Enable signal. A logical high on this pin enables a read from the output of the FIFO. |
| DV | O | DV or Data Valid output signal.<br>In SCAPI/CAPI mode: DV performs a two functions depending on whether SCAPI or CAPI is selected. It toggles high when the FIFO has reached the AFF margin set by the user, and remains high until the FIFo is empty. The alternative mode is where it can be used to control FIFO reads for bursting information out of the FIFO. In API mode DV indicates valid data in the FIFO, which includes both pixel information and control codes. The polarity of this pin is controlled via PDV. |
| $\overline{OE}$ | I | Output Enable controls pixel port outputs. A logical low will tri-state P19-P0. |
| HREF/$\overline{HRESET}$ | O | Dual function pin, HREF or Horizontal Reference output signal (enabled when Line Locked Interface is selected , OM_SEL[1:0] = 0,0); this signal is used to indicate data on the YUV output. The positive slope indicates the begining of a new active line, HREF is always 720 Y samples long. $\overline{HRESET}$ or Horizontal Reset Output (enabled when SCAPI or CAPI is selected, OM_SEL[1:0] = 0,1 or 1,0) is a signal the indicates the begining of a new line of video. In SCAPI/CAPI this signal is one clock cycle wide and is output relative to CLKIN. It immedi ately follows the last active pixel of a line. The polarity of this pin is controlled via PHVR. |

**PIN DESCRIPTION**

| Mnemonic | Input/Output | Function |
|---|---|---|
| VREF/$\overline{\text{VRESET}}$ | O | VREF or Vertical Reference output signal, indicates start of next field). $\overline{\text{VRESET}}$ or Vertical Reset Output is a signal that indicates the begining of a new field. In SCAPI/CAPI mode this signal is one clock wide and active low relative to CLKIN. It immediately follows $\overline{\text{HRESET}}$ pixel, and it indicates that the next active pixel is the first active pixel of the next field. |
| LLCREF | O | Clock reference ouput; this is a clock qualifier distributed by the internal CGC for a data rate of LLC2. The polarity of LLCREF is controlled by PLLCREF bit. |
| LLC1/PCLK | O | Dual function pin, Line Locked Clock system output clock (27MHz ±5%) or a FIFO output clock ranging from 20-35MHZ. |
| LLC2 | O | Line locked clock system output clock/2 (13.5MHz). |
| HLOCK | O | Horizontal locked: output signal indicating horizontal locking status, a logical high indicates the ADV7183 is locked horizontaly to the input video source. |
| $\overline{\text{RESET}}$ | I/O | System Reset, can be configured as an Input or Output signal (the RES bit can be used to control this pin). |
| $\overline{\text{PWRDN}}$ | I | Power Down enable, a logical low will place part in a power down status. |
| REFOUT | O | Internal Voltage Reference Output. |
| CML | O | Common Mode Level for ADC. |
| AEF | O | Almost Empty Flag is a FIFO control signal. It indicates when the FIFO has reached the almost empty margin set by the user (use FFM[4:0]). The ploarity of this signal is controled by PFF bit. |
| HFF/QCLK/GL | I/O | Multi function pin, Half Full Flag (OM_SEL[1:0] = 1,0) is a FIFO control signal which indicates when the FIFO is half full. The QCLK (OM_SEL[1:0] = 0,1) pin function is a qualified pixel output clcok when using FIFO SCAPI mode. The GL (OM_SEL[1:0] = 0,0) function (Genlock output) is a signal that contains a serial stream of data which contains information for locking the subcarrier frequency. The ploarity of HFF signal is controled by PFF bit. |
| AFF | O | Almost Full Flag is a FIFO control signal. It indicates when the FIFO has reached the almost full margin set by the user (use FFM[4:0]). The ploarity of this signal is controled by PFF bit. |
| CLKIN | I | FIFO is an asynchronous FIFO clock. This asynchronous clock is used to output data onto the P19-P0 bus and other control signals. The LLC1 clock can be tied to this pin and the frequency programmed by CLKVAL[13:0]. |
| FIELD | O | ODD/EVEN field output signal. A active state indicates that an even field is being digitized. The polarity of this signal is controlled by PF bit. |
| HS/HACTIVE | O | Dual function pin, HS or Horizontal Sync (OM_SEL[1:0] = 0,0) is a programmable horizontal sync output signal. The rising and falling edges can be controlled by HSB[9:0] and HSE[9:0] in steps of 2 LLC1. The ploarity of HS signal is controled by PHS bit. HACTIVE (OM_SEL[1:0] = 1,0 or 0,1) is an output signal that is active during the active/viewable period of a video line. The active portion of a video line is programmable on the ADV7183. The polarity of HACTIVE is controlled by PHS bit. |
| VS/VACTIVE | O | Dual function pin, VS or Vertical Sync (OM_SEL[1:0] = 0,0) is an output signal that indicates a vertical sync with respect to the YUV pixel data. The active period of this signal is six lines of video long. The ploarity of VS signal is controled by PVS bit. VACTIVE (OM_SEL[1:0] = 1,0 or 0,1) is an output signal that is active during the active/viewable period of a video field. The polarity of VACTIVE is controlled by PVS bit. |

**PIN DESCRIPTION**

| Mnemonic | Input/Output | Function |
|---|---|---|
| ISO | I | ISO or Input Switch Over is an input that indicates to the decoder core that the input video source has been changed externally and configures the deocder to reacquire the new timing infromation of the new source. This is useful in applications where external video muxs are used. This input gives the advantage of faster locking to the external muxed video sources. |
| CAPY1-2 | I | ADC Capacitor network |
| CAPC1-2 | I | ADC Capacitor network |




**ADV7183 PIN FUNCTIONALITY**

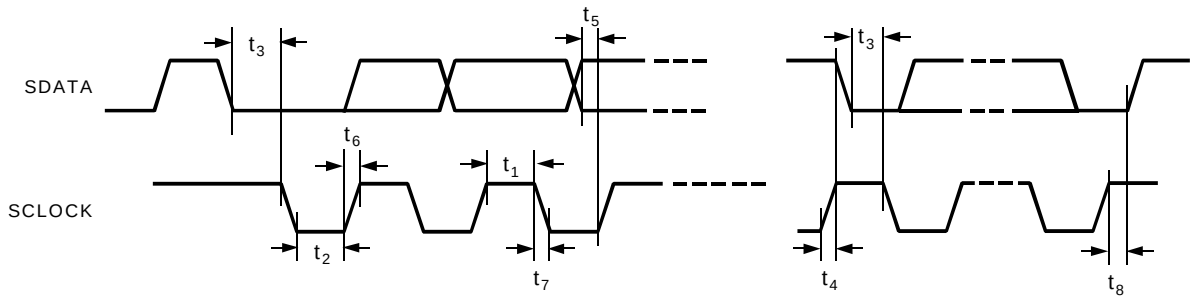



*Figure 2. MPU Port Timing Diagram*

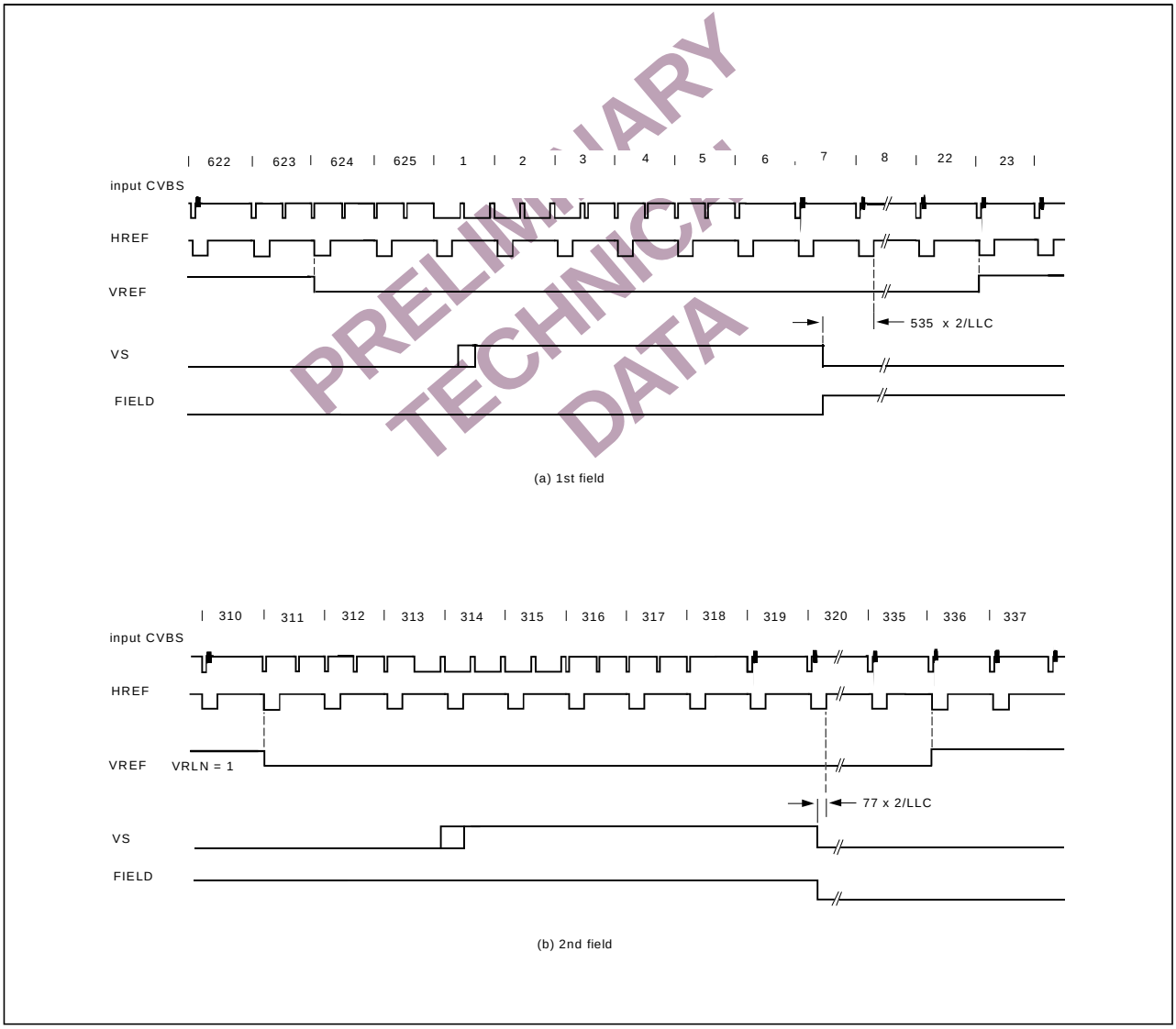





*Figure 3. Vertical Timing Diagram 50Hz system*

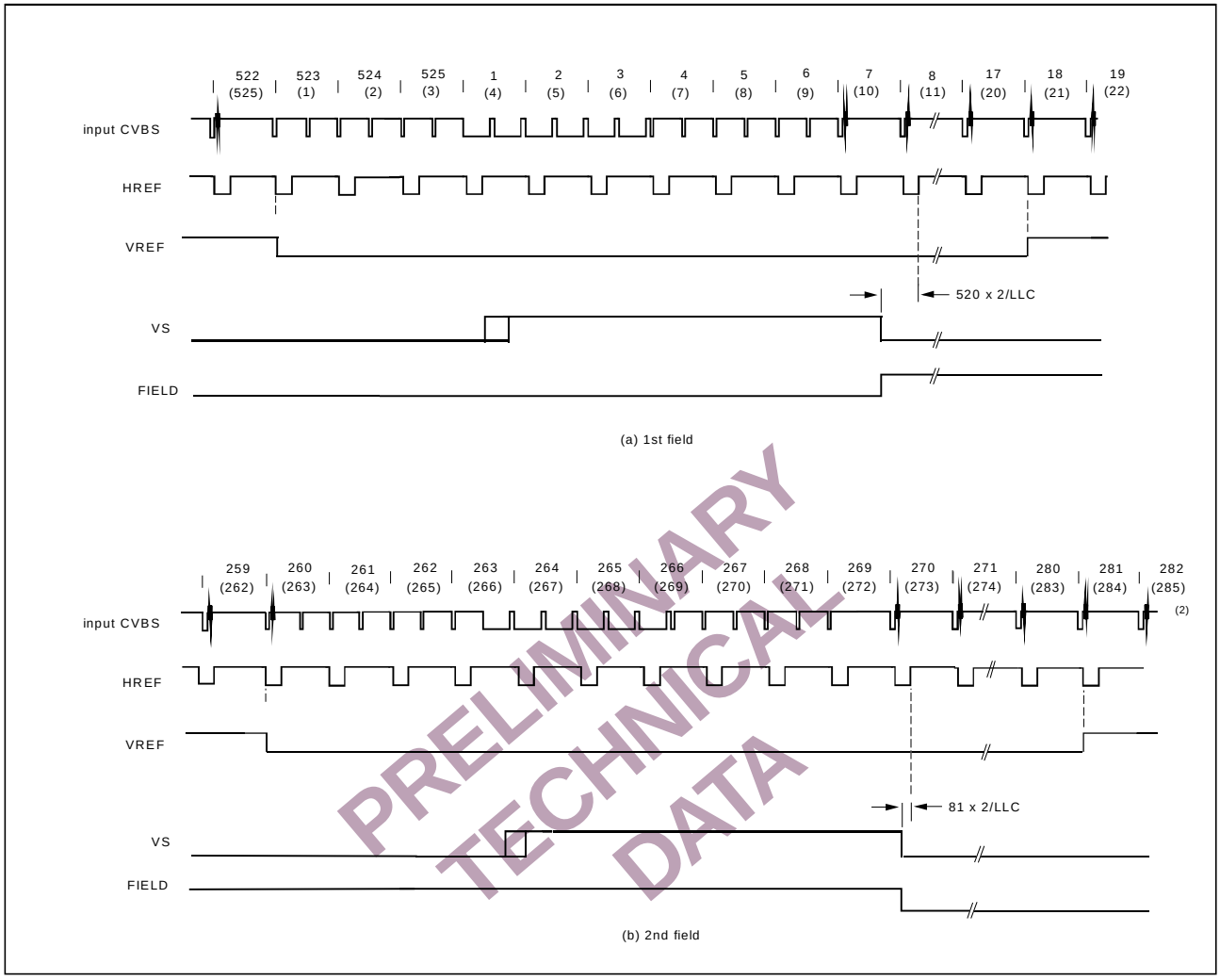



*Figure 13. Vertical Timing Diagram 60Hz system*

## LUMINANCE SHAPING FILTER L PLOTS

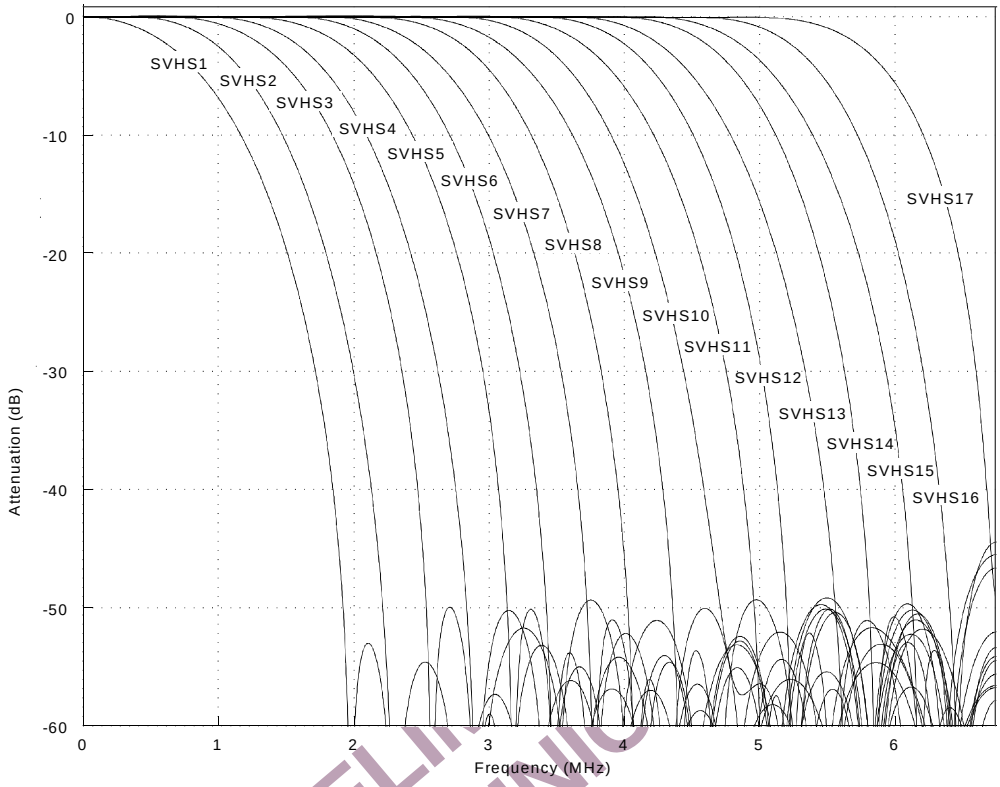



*Figure xx. Luminance SVHS1-17 shaping filter responses*

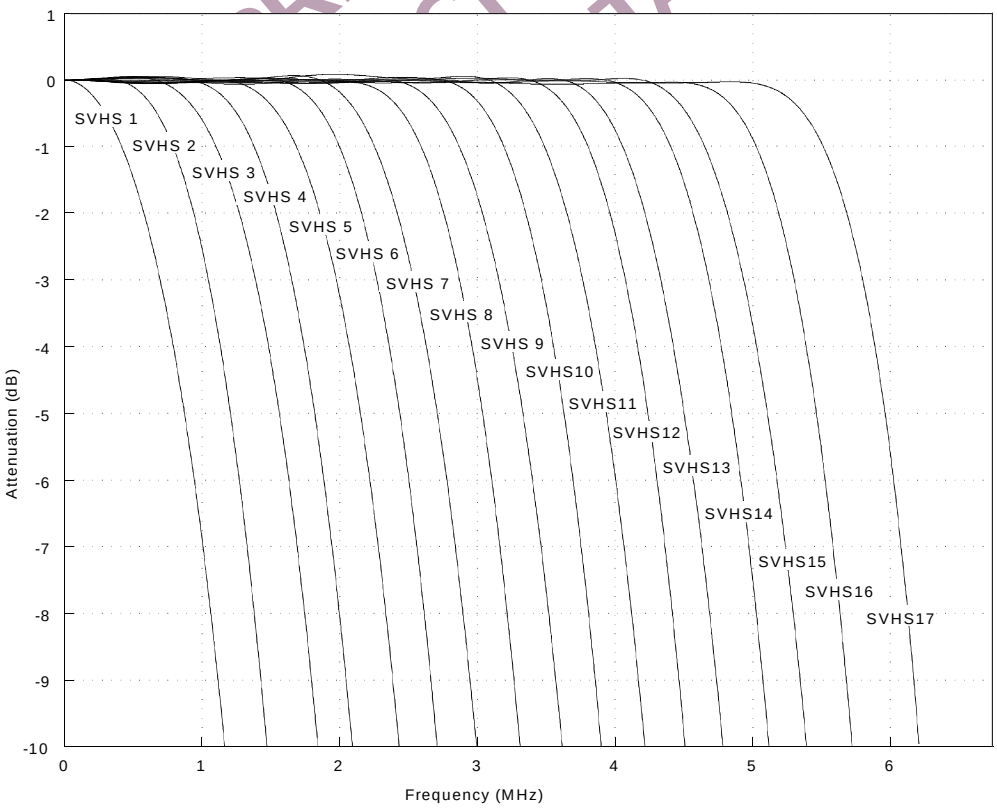



*Figure xx. Luminance SVHS1-17 shaping filter responses (closeup)*

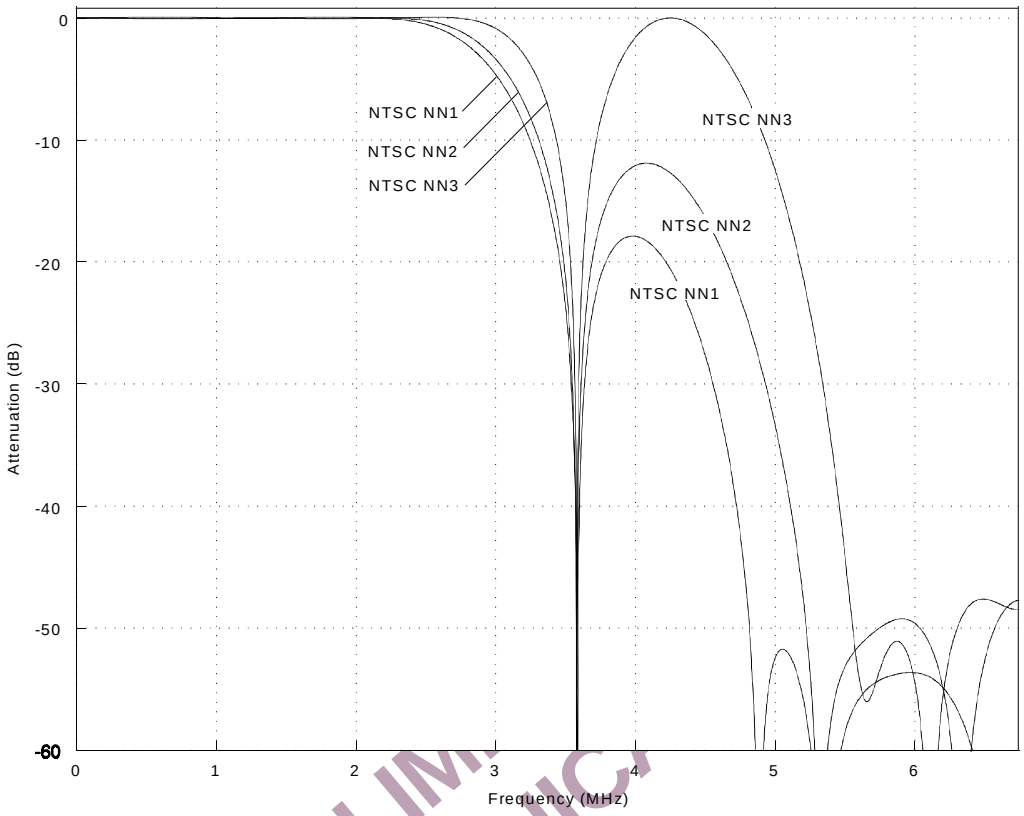



*Figure xx. Luminance NTSC Narrow Notch shaping filter responses*

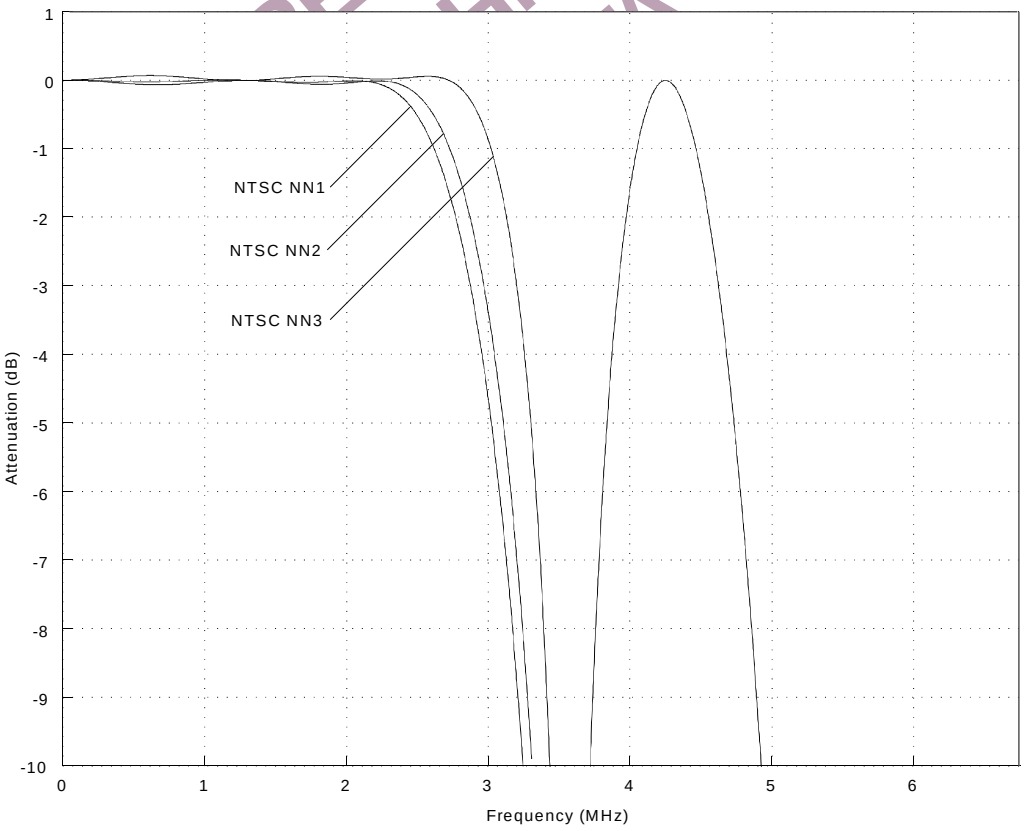



*Figure xx. Luminance NTSC Narrow Notch shaping filter responses (closeup)*

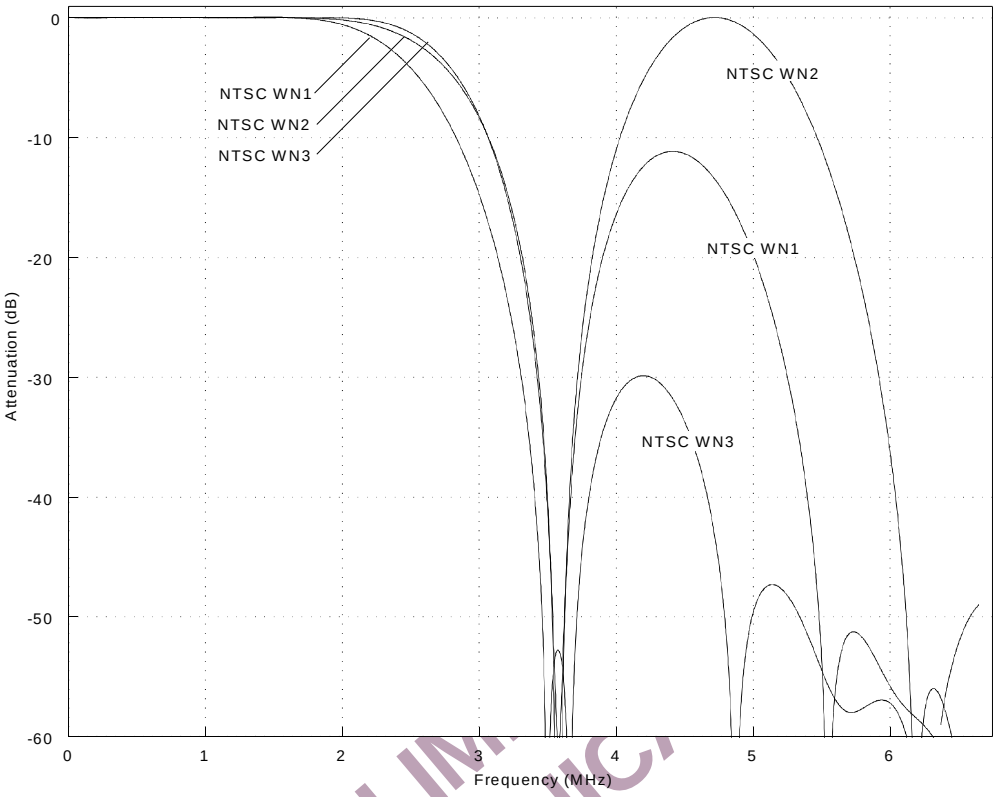



*Figure xx. Luminance NTSC Wide Notch shaping filter responses*

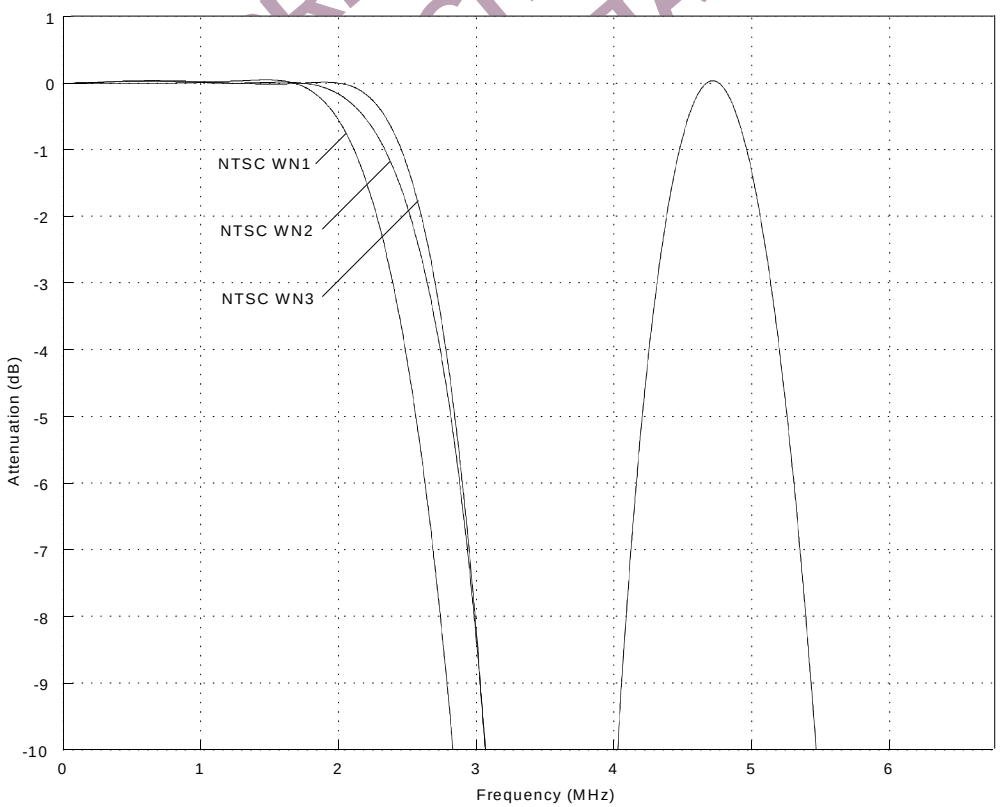



*Figure xx. Luminance NTSC Wide Notch shaping filter responses (closeup)*

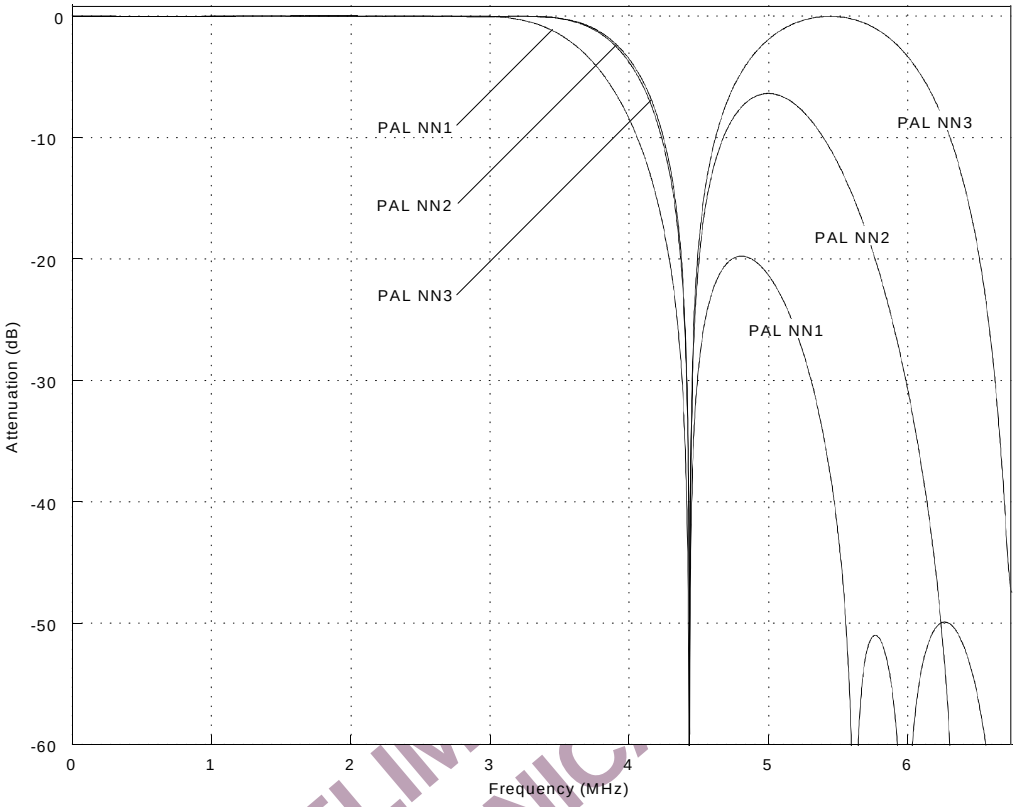



*Figure xx. Luminance PAL Narrow Notch shaping filter responses*

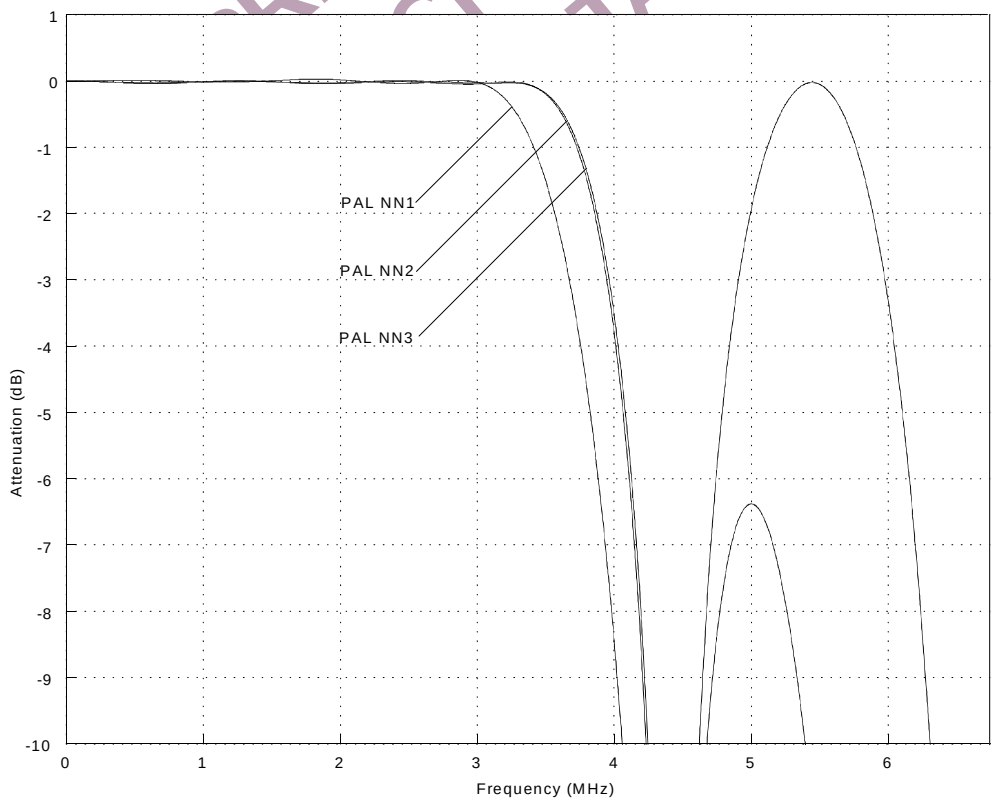



*Figure xx. Luminance PAL Narrow Notch shaping filter responses (closeup)*

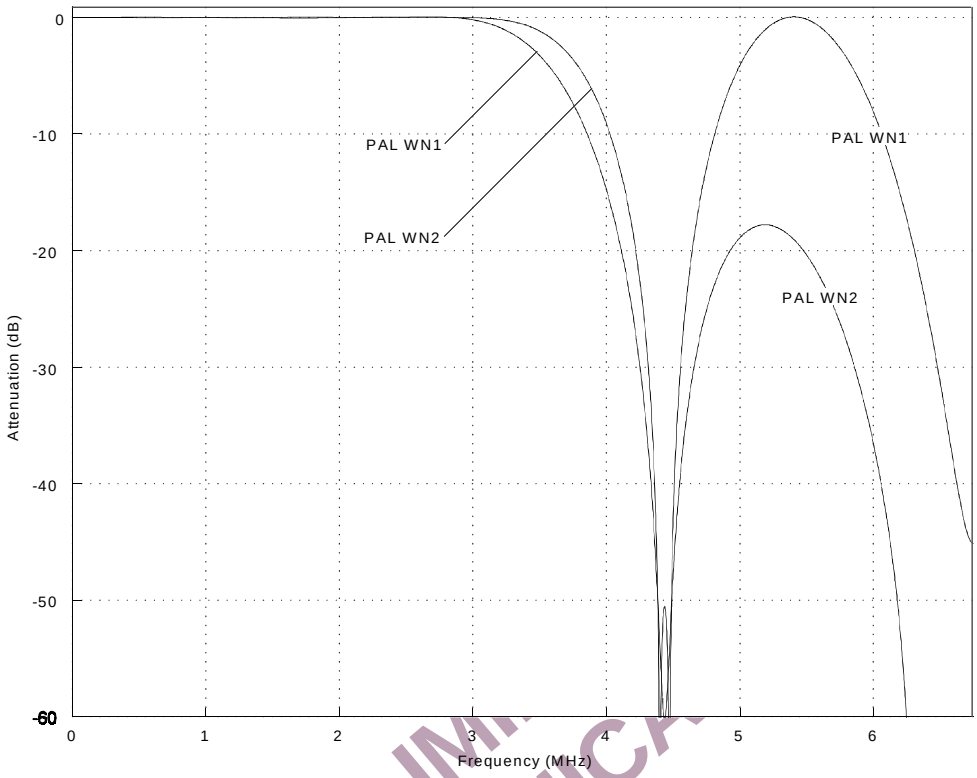



*Figure xx. Luminance PAL Wide Notch shaping filter responses*

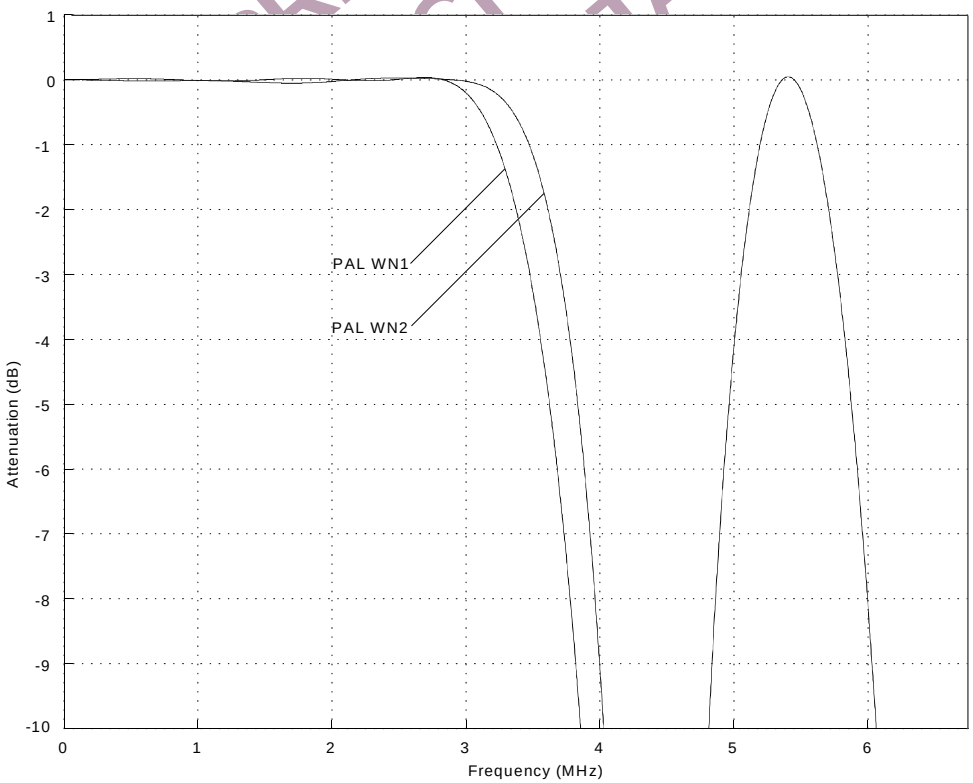



*Figure xx. Luminance PAL Wide Notch shaping filter responses (closeup)*

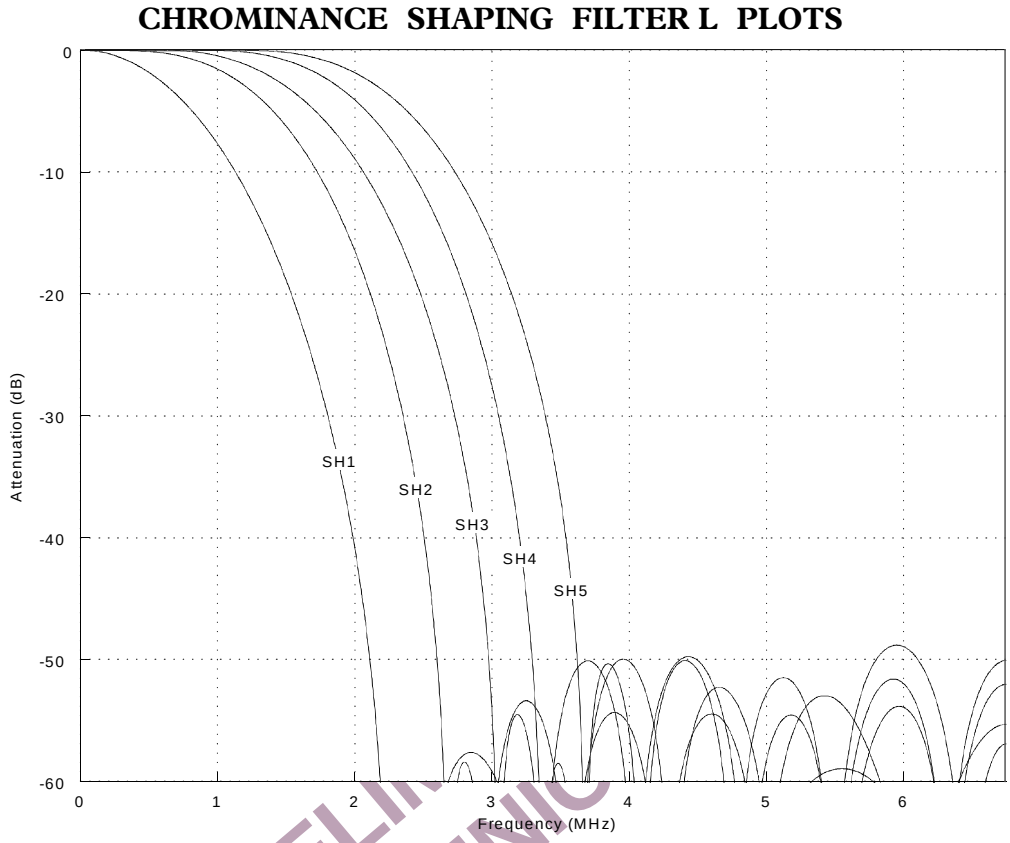



*Figure xx. Chrominance shaping filter responses*

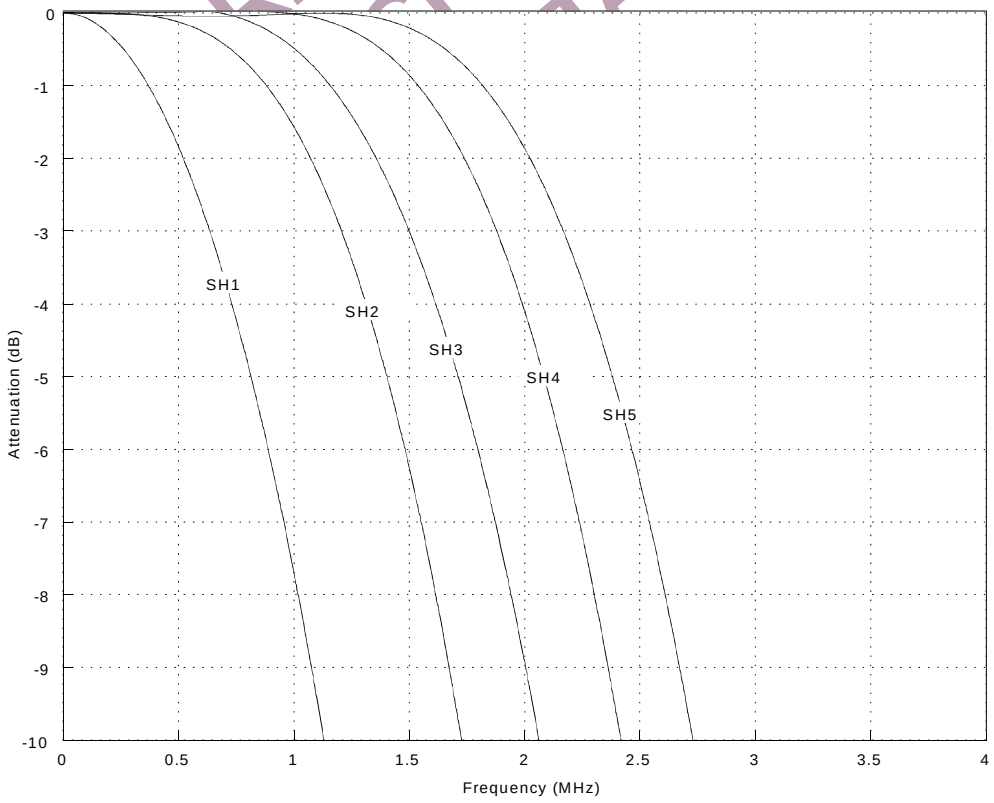



*Figure xx. Chrominance shaping filter responses (closeup)*

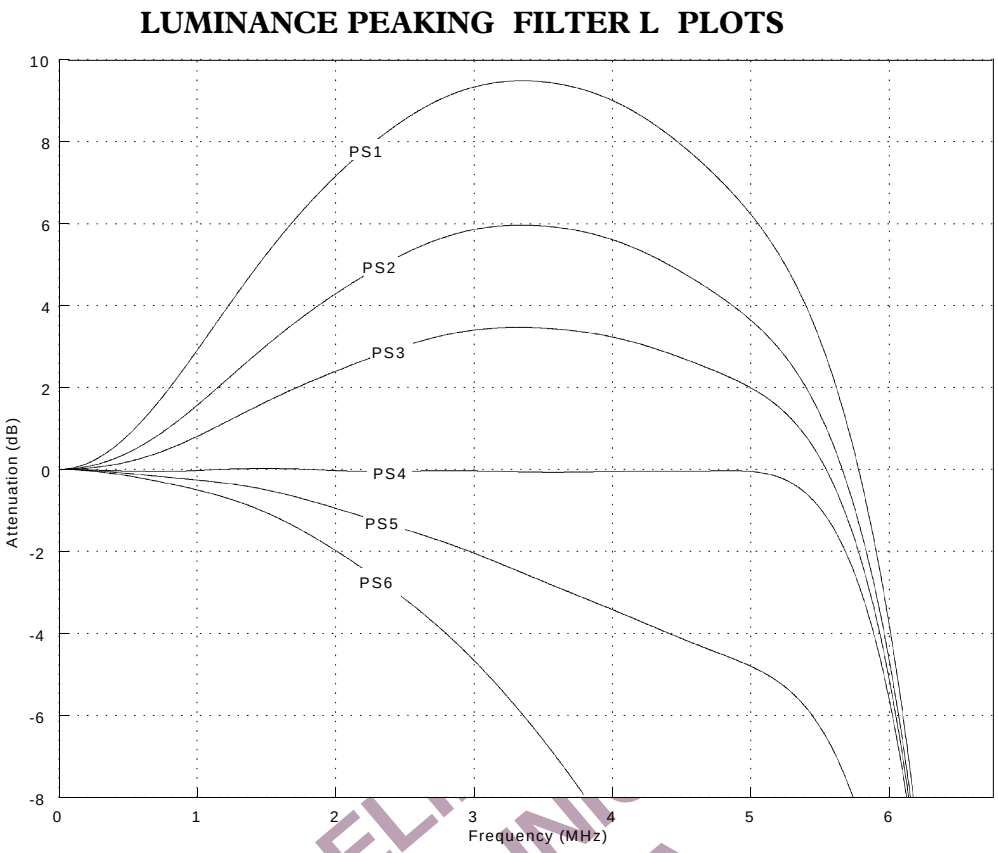



*Figure xx. Luminance Peaking filter responses in S-Video (SVHS17 selected)*

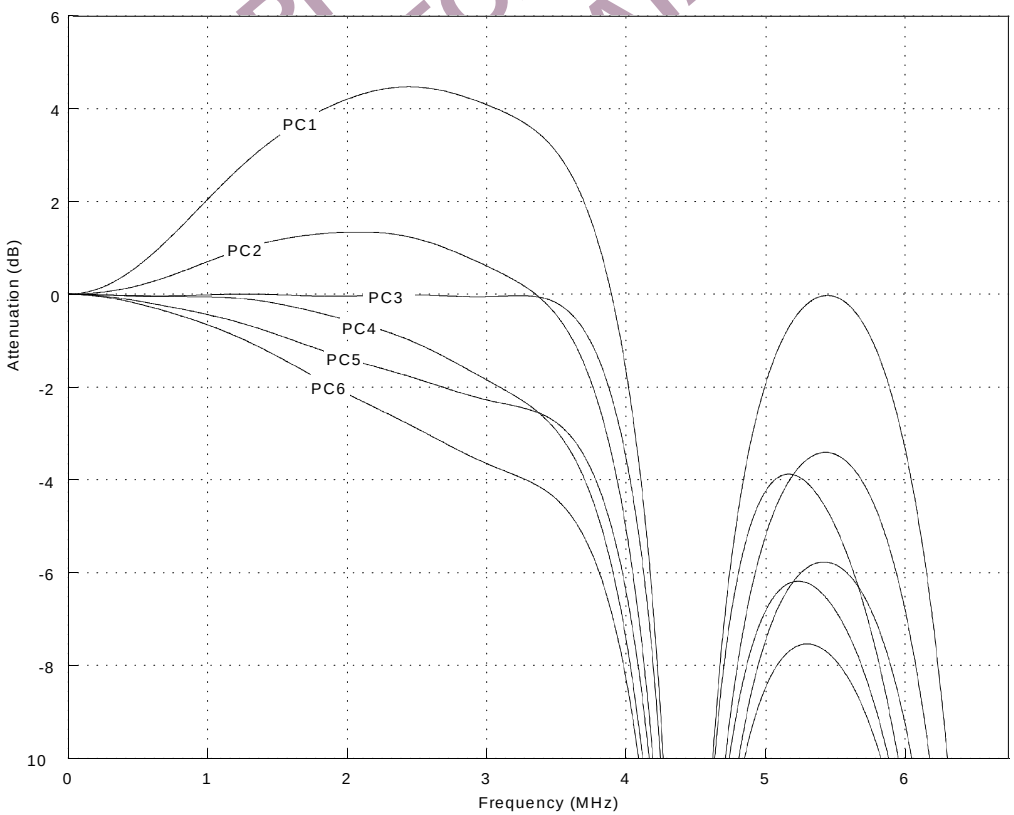



*Figure xx. Luminance Peaking filter responses in CVBS (PAL NN3 selected)*

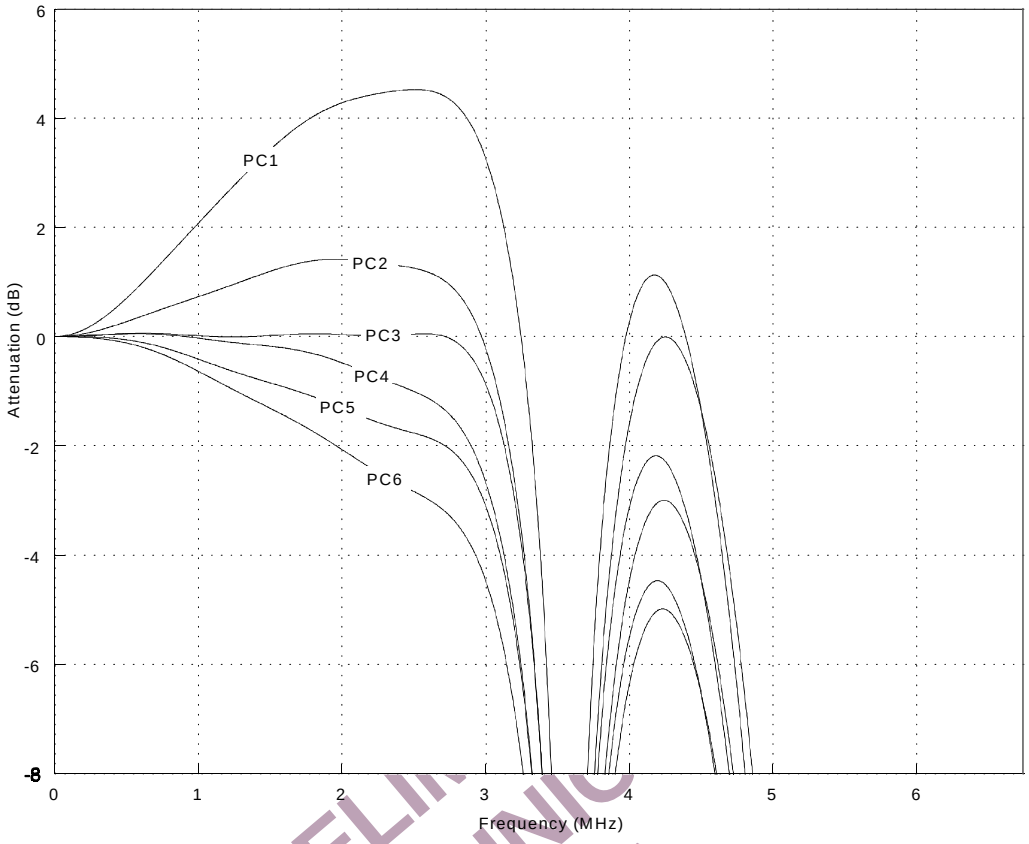



*Figure xx. Luminance Peaking filter responses in CVBS (NTSC NN3 selected)*

## IMPORTANT EQUATIONS

The following is a list of important equations:

$$CSFM[27:0] = \frac{F_{sc} \times 2^{28}}{XTAL\ Frequency}$$

$$Chroma\_Gain = \frac{(0 < CG \le 4095)}{1024} = 0...4$$

$$Luma\_Gain = \frac{(0 < LG \le 4095)}{2048} = 0...4$$

$$End\ Input\ Horiz\ Window = AVHB + \frac{(N_{NOM} \times HSCV)}{2^{21}} \times AVDP$$

$$End\ Input\ Vertical\ Window = AVHB + \left(\frac{VSCV}{2^{8}} \times LCD\right) \times AVDL$$

$$Horizontal\ Scaling = \left(\frac{N_{NOM} \times HSCV}{2^{21}}\right) \times AVDL$$

$$Y_{OUT} = \left(\frac{CONTRAST}{128} \times (Y - 128)\right) + (BRIGHTNESS \times 8)$$

$$UV_{OUT} = \left(\frac{SATURATION}{128} \times (Cr, Cb - 128)\right) + 128$$

$$CLKVAL = \frac{f_{LLC}}{27 \times 10^{6}} \times \frac{2^{24}}{1728}$$

**MPU PORT DESCRIPTION.**

The ADV7183 support a two wire serial ($I^2C$ Compatible) microprocessor bus driving multiple peripherals. Two inputs Serial Data (SDATA) and Serial Clock (SCLOCK) carry information between any device connected to the bus. Each slave device is recognised by a unique address. The ADV7183 has two possible slave addresses for both read and write operations. These are unique addresses for the device and are illustrated in Figure xx. The LSB sets either a read or write operation. Logic level "1" corresponds to a read operation while logic level "0" corresponds to a write operation. A1 is set by setting the ALSB pin of the ADV7183 to logic level "0" or logic level "1".

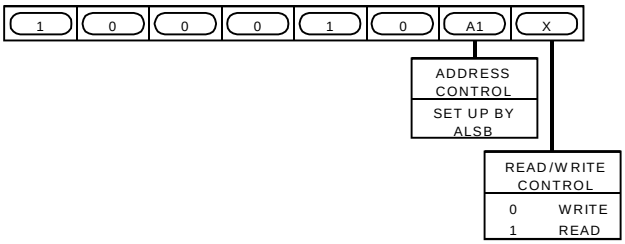



*Fig xx. ADV7183 Slave Address*

To control the device on the bus the following protocol must be followed. First the master initiates a data transfer by establishing a Start condition, defined by a high to low transistion on SDATA whilst SCLOCK remains high. This indicates that an address/data stream will follow. All peripherals respond to the Start condition and shift the next eight bits (7-Bit address + R/$\overline{W}$ bit). The bits tranferred from MSB down to LSB. The peripheral that recognises the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDATA and SCLOCK lines waiting for the Start condition and the correct transmitted address. The R/$\overline{W}$ bit determines the direction of the data. A logic "0" on the LSB of the first byte means that the master will write information to the peripheral. A logic "1" on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7183 acts as a standard slave device on the bus. The data on the SDATA pin is 8 bits long supporting the 7-Bit addresses plus the R/$\overline{W}$ bit. The ADV7183 has 71 subaddresses to enable access to the internal registers. It therefore interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto increment allowing data to be written to or read from from the starting subaddress. A data transfer is always terminated by a Stop condition. The user can also access any unique subaddress register on a one by one basis without having to update all the registers.

Stop and Start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, then these cause an immediate jump to the idle condition. During a given SCLOCK high period the user should only issue one Start condition, one Stop condition or a single Stop condition followed by a single Start condition. If an invalid subaddress is issued by the user, the ADV7183 will not issue an acknowledge and will return to the idle condition. If in auto-increment mode, the user exceeds the highest subaddress then the following action will be taken:

1. In Read Mode the highest subaddress register contents will continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no-acknowledge condition is where the SDATA line is not pulled low on the ninth pulse.

2. In Write Mode, the data for the invalid byte will be not be loaded into any subaddress register, a no-acknowledge will be issued by the ADV7183 and the part will return to the idle condition.

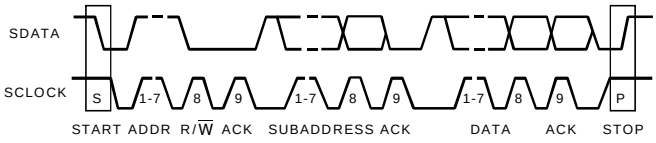



*Figure yy. Bus Data Transfer*

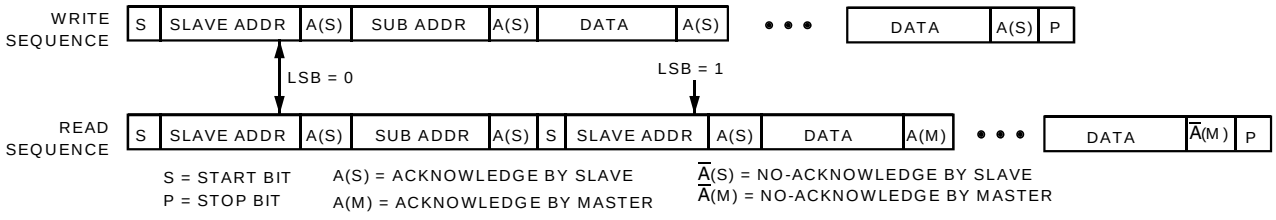



Figure 35 Illustrates an example of data transfer for a read sequence and the Start and Stop conditions.

*Figure 36. Write and Read Sequences*

## REGISTER ACCESSES

The MPU can write to or read from all of the registers of the ADV7183 except the Subaddress Register which is a write only register. The Subaddress Register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the Subaddress Register. Then a read/write operation is performed from/to the target address which then increments to the next address until a Stop command on the bus is performed.

## REGISTER PROGRAMMING

The following section describes each register in terms of its configuration.

**Subaddress Register (SR7-SR0)**

The Communications Register is an eight bit write-only register. After the part has been accessed over the bus and a read/write operation is selected, the subaddress is set up. The Subaddress Register determines to/from which register the operation takes place.

Figure 37 shows the various operations under the control of the Subaddress Register. Zero should always be written to SR7-SR6.

**Register Select (SR5-SR0):**

These bits are set up to point to the required starting address.

| Register Name | Subaddress(Hex) |
|---|---|
| **BASIC BLOCK** | |
| Input Control | 00 |
| Video Selection | 01 |
| Video Enhancement Control | 02 |
| Output Control | 03 |
| Extended Output Control | 04 |
| General Purpose Output | 05 |
| Reserved | 06 |
| FIFO Control | 07 |
| Contrast Control | 08 |
| Saturation Control | 09 |
| Brightness Control | 0A |
| Hue Control | 0B |
| Default Value Y | 0C |
| Default Value C | 0D |
| Temporal Decimation | 0E |
| Power Management | 0F |
| Status Register | 10 |
| Info Register | 11 |
| | |
| **ADVANCED BLOCK** | |
| Reserved | 12 |
| Reserved | 13 |
| Analog Clamp Control | 14 |
| Digital Clamp Control 1 | 15 |
| Digital Clamp Control 2 | 16 |
| Shaping Filter Control | 17 |
| Reserved | 18 |
| Comb Filter Control | 19 |
| Scaling/Cropping MSB | 1A |
| Active Video Desired Lines | 1B |
| Active Video Vertical Begin | 1C |

| Register Name | Subaddress(Hex) |
|---|---|
| **ADVANCED BLOCK** | |
| Vertical Scale Value 1 | 1D |
| Vertical Scale Value 2 | 1E |
| Active Video Horiz Begin | 1F |
| Active Video desired Pixel | 20 |
| Horizontal Scale Value1 | 21 |
| Horizontal Scale Value2 | 22 |
| Reserved | 23 |
| Color Subcarrier Control 1 | 24 |
| Color Subcarrier Control 2 | 25 |
| Color Subcarrier Control 3 | 26 |
| Color Subcarrier Control 4 | 27 |
| Pixel Delay Control | 28 |
| Manual Clock Control 1 | 29 |
| Manual Clock Control 2 | 2A |
| Auto Clock Control | 2B |
| AGC Mode Control | 2C |
| Chroma Gain Control 1 | 2D |
| Chroma Gain Control 2 | 2E |
| Luma Gain Control 1 | 2F |
| Luma Gain Control 2 | 30 |
| Manual Gain Shadow Control 1 | 31 |
| Manual Gain Shadow Control 2 | 32 |
| Misc Gain Control | 33 |
| Hsync Position Control 1 | 34 |
| Hsync Position Control 2 | 35 |
| Hsync Position Control 3 | 36 |
| Polarity Control | 37 |
| Reserved | 38 |
| Reserved | 39 |
| Reserved | 3A |
| Reserved | |



*Figure 37. Subaddress Register*

*Table 1.0 Basic Registers*

| Register Name | addr (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| **Input Control** | 00 | VID SEL.3 | VID SEL.2 | VID SEL.1 | VID SEL.0 | INSEL.3 | INSEL.2 | INSEL.1 | INSEL.0 |
| **Video Selection** | 01 | ASE | - | - | - | - | SQPE | VID QUAL.1 | VID QUAL.0 |
| **Video Enhancement Control** | 02 | - | - | - | COR.1 | COR.0 | YPM.2 | YPM.1 | YPM.0 |
| **Output Control** | 03 | VBI EN | TOD | OF SEL.3 | OF SEL.2 | OF SEL.1 | OF SEL.O | OM SEL.1 | OMEL.O |
| **Extended Output Control** | 04 | - | - | - | - | - | - | - | RANGE |
| **General Purpose Output** | 05 | - | - | GPEH | GPEL | GP0.3 | GP0.2 | GP0.1 | GP0.0 |
| **Reserved** | 06 | - | - | - | - | - | - | - | - |
| **FIFO Control** | 07 | FFST | AFR | FR | FFM.4 | FFM.3 | FFM.2 | FFM.1 | FFM.0 |
| **Contrast Control** | 08 | CON.7 | CON.6 | CON.5 | CON.4 | CON.3 | CON.2 | CON.1 | CON.0 |
| **Saturation Control** | 09 | SAT.7 | SAT.6 | SAT.5 | SAT.4 | SAT.3 | SAT.2 | SAT.1 | SAT.0 |
| **Brightness Control** | 0A | BRI.7 | BRI.6 | BRI.5 | BRI.4 | BRI.3 | BRI.2 | BRI.1 | BRI.0 |
| **Hue Control** | 0B | HUE.7 | HUE.6 | HUE.5 | HUE.4 | HUE.3 | HUE.2 | HUE.1 | HUE.0 |
| **Default Value Y** | 0C | DEF Y.5 | DEF Y.4 | DEF Y.3 | DEF Y.2 | DEF Y.1 | DEF Y.0 | DEF_AUTO_EN | DEF_VAL_EN |
| **Default Value C** | 0D | DEF C.7 | DEF C.6 | DEF C.5 | DEF C.4 | DEF C.3 | DEF C.2 | DEF C.1 | DEF C.0 |
| **Temporal Decimation** | 0E | - | TDR.3 | TDR.2 | TDR.1 | TDR.0 | TDC.1 | TDC.0 | TDE |
| **Power Management** | 0F | RES | TRAQ | PWRDN | PS CG | PS REF | PDBP | PSC.1 | PSC.0 |
| **Status Register** | 10 | STATUS.7 | STATUS.6 | STATUS.5 | STATUS.4 | STATUS.3 | STATUS.2 | STATUS.1 | STATUS.0 |
| **Info Register** | 11 | - | - | - | - | - | IDENT.2 | IDENT.1 | IDENT.0 |

*Table 2.0 Advanced Registers*

| Register Name | addr (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Reserved | 12 | - | - | - | - | - | - | - | - |
| Reserved | 13 | - | - | - | - | - | - | - | - |
| Analog Clamp Control | 14 | - | - | VCLEN | CCLEN | FACL.1 | FACL.0 | FICL.1 | FICL.0 |
| Digital Clamp Control 1 | 15 | DCCM | DCT.1 | DCT.0 | DCFE | DCC0.11 | DCC0.10 | DCC0.9 | DCC0.8 |
| Digital Clamp Control 2 | 16 | DCC0.7 | DCC0.6 | DCC0.5 | DCC0.4 | DCC0.3 | DCC0.2 | DCC0.1 | DCC0.0 |
| Shaping Filter Control | 17 | CSFM.2 | CSFM.1 | CSFM.0 | YSFM.4 | YSFM.3 | YSFM.2 | YSFM.1 | YSFM.0 |
| Reserved | 18 | - | - | - | - | - | - | - | - |
| Comb Filter Control | 19 | - | - | - | CCMB_AD | CCM.1 | CCM.0 | LCM.1 | LCM.0 |
| Scaling/Cropping MSB | 1A | AVDL.8 | AVVB.8 | AVHB.9 | AVDP.9 | AVDP.8 | - | - | SCE |
| Active Video Desired Lines | 1B | AVDL.7 | AVDL.6 | AVDL.5 | AVDL.4 | AVDL3 | AVDL.2 | AVDL.1 | AVDL.0 |
| Active Video Vertical Begin | 1C | AVVB.8 | AVVB.7 | AVVB.6 | AVVB.5 | AVVB.4 | AVVB.3 | AVVB.2 | AVVB.1 |
| Vertical Scale Value 1 | 1D | - | - | - | - | - | VSCV.10 | VSCV.9 | VSCV.8 |
| Vertical Scale Value 2 | 1E | VSCV.7 | VSCV.6 | VSCV.5 | VSCV.4 | VSCV.3 | VSCV.2 | VSCV.1 | VSCV.0 |
| Active Video Horiz Begin | 1F | AVHB.7 | AVHB.6 | AVHB.5 | AVHB.4 | AVHB.3 | AVHB.2 | AVHB.1 | AVHB.0 |
| Active Video desired Pixel | 20 | AVDP.7 | AVDP.6 | AVDP.5 | AVDP.4 | AVDP.3 | AVDP.2 | AVDP.1 | AVDP.0 |
| Horizontal Scale Value1 | 21 | HSCV.15 | HSCV.14 | HSCV.13 | HSCV.12 | HSCV.11 | HSCV.10 | HSCV.9 | HSCV.8 |
| Horizontal Scale Value2 | 22 | HSCV.7 | HSCV.6 | HSCV.5 | HSCV.4 | HSCV.3 | HSCV.2 | HSCV.1 | HSCV.0 |
| Reserved | 23 | - | - | - | - | - | - | - | - |
| Color Subcarrier Control 1 | 24 | - | - | - | CSM | CSMF.27 | CSMF.26 | CSMF.25 | CSMF.24 |
| Color Subcarrier Control 2 | 25 | CSMF.23 | CSMF.22 | CSMF.21 | CSMF.20 | CSMF.19 | CSMF.18 | CSMF.17 | CSMF.16 |
| Color Subcarrier Control 3 | 26 | CSMF.15 | CSMF.14 | CSMF.13 | CSMF.12 | CSMF.11 | CSMF.10 | CSMF.9 | CSMF.8 |
| Color Subcarrier Control 4 | 27 | CSMF.7 | CSMF.6 | CSMF.5 | CSMF.4 | CSMF.3 | CSMF.2 | CSMF.1 | CSMF.0 |

*Table 2.1 Advanced Registers Continued*

| Register Name | addr (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Pixel Delay Control | 28 | SWPC | - | CTA.2 | CTA.1 | CTA.0 | - | - | - |
| Manual Clock Control 1 | 29 | FIX27E | CLKMANE | CLKVAL.13 | CLKVAL.12 | CLKVAL.11 | CLKVAL.10 | CLKVAL.9 | CLKVAL.8 |
| Manual Clock Control 2 | 2A | CLKVAL.7 | CLKVAL.6 | CLKVA5L.13 | CLKVAL.4 | CLKVAL.3 | CLKVAL.2 | CLKVAL.1 | CLKVAL.0 |
| Reserved | 2B | - | - | - | - | - | - | - | - |
| AGC Mode Control | 2C | - | LAGC.2 | LAGC.1 | LAGC.0 | - | - | CAGC.1 | CAGC.0 |
| Chroma Gain Control 1 | 2D | CAGT.1 | CAGT.0 | - | - | CMG.11 | CMG.10 | CMG.9 | CMG.8 |
| Chroma Gain Control 2 | 2E | CMG.7 | CMG.6 | CMG.5 | CMG.4 | CMG.3 | CMG.2 | CMG.1 | CMG.0 |
| Luma Gain Control 1 | 2F | LAGT.1 | LAGT.0 | - | - | LMG.11 | LMG.10 | LMG.9 | LMG.8 |
| Luma Gain Control 2 | 30 | LMG.7 | LMG.6 | LMG.5 | LMG.4 | LMG.3 | LMG.2 | LMG.1 | LMG.0 |
| Manual Gain Shadow Control 1 | 31 | SGUE | - | - | - | LMGS.11 | LMGS.10 | LMGS.9 | LMGS.8 |
| Manual Gain Shadow Control 2 | 32 | LMGS.7 | LMGS.6 | LMGS.5 | LMGS.4 | LMGS.3 | LMGS.2 | LMGS.1 | LMGS.10 |
| Misc Gain Control | 33 | - | CKE | - | MIRE.2 | MIRE.1 | MIRE.0 | AV_AL | PW_UPD |
| Hsync Position Control 1 | 34 | HSB.9 | HSB.8 | HSE.9 | HSE.8 | - | - | - | - |
| Hsync Position Control 2 | 35 | HSB.7 | HSB.6 | HSB.5 | HSB.4 | HSB.3 | HSB.2 | HSB.1 | HSB.0 |
| Hsync Position Control 3 | 36 | HSE.7 | HSE.6 | HSE.5 | HSE.4 | HSE.3 | HSE.2 | HSE.1 | HSE.0 |
| Reserved | 37 | - | - | - | - | - | - | - | - |
| Reserved | 38 | - | - | - | - | - | - | - | - |
| Reserved | 39 | - | - | - | - | - | - | - | - |
| Reserved | 3A | - | - | - | - | - | - | - | - |

# BASIC USER REGISTER MAP

## INPUT CONTROL (SUBADDRESS 00H)

### INSEL[3:0] VIDEO INPUT CHANNEL SELECTION (D3-D0)

The INSEL bits allow the user to select an input channel as well as the input format for that channel. The ADV7183 can be configured as having 4 CVBS inputs , 2 S-Video inputs or any combination of CVBS, S-vVideo when combined give a total to four channels (e.g. 2 CVBS[2 channel], 1 S-Video [2 channel]).

| INSEL 3 | INSEL 2 | INSEL 1 | INSEL 0 | I/P Pins selected | Video Format |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | A1 | CVBS |
| 0 | 0 | 0 | 1 | A2 | CVBS |
| 0 | 0 | 1 | 0 | - | - |
| 0 | 0 | 1 | 1 | A3 | CVBS |
| 0 | 1 | 0 | 0 | A4 | CVBS |
| 0 | 1 | 0 | 1 | - | - |
| 0 | 1 | 1 | 0 | Y1 = A1<br>C1 = A4 | S-Video |
| 0 | 1 | 1 | 1 | Y2 = A2<br>C2 = A5 | S-Video |
| 1 | 0 | 0 | 0 | - | - |
| 1 | 0 | 0 | 1 | - | - |
| 1 | 0 | 1 | 0 | - | - |
| 1 | 0 | 1 | 1 | No I/P | Free Run |
| 1 | 1 | 0 | 0 | - | - |
| 1 | 1 | 0 | 1 | - | - |
| 1 | 1 | 1 | 0 | - | - |
| 1 | 1 | 1 | 1 | - | - |



*Table xx. Input Selection Table*

**VID_SEL[3:0] VIDEO INPUT STANDARD SELECTION (D7-D4)**

The VID_SEL bits allow the user to select the decode standard for the selected input channel.The ADV7183 is configured to decode the input video as per the standard seleceted. There are also 4 autodetect modes which will automatically switch between one of the two possible standards for the selected mode. For example if VID_SEL[3:0] = 0010 and a PAL N source is connected , and the user switches the source to a PAL M (without pedestal) the ADV7183 will automatically detect this change without any input from the user and decode the video acordingly. The non-autodetect modes simply decode the selected standard only, the mode will have to be changed by the user if a different standard source is connected to the deocder.

| VID_SEL.3 | VID_SEL.2 | VID_SEL.1 | VID_SEL.0 | Video Format |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Autodetect (PAL BGHID) - NTSC M (without pedestal) |
| 0 | 0 | 0 | 1 | Autodetect (PAL BGHID) - NTSC M (with pedestal) |
| 0 | 0 | 1 | 0 | Autodetect (PAL N) - NTSC M (without pedestal) |
| 0 | 0 | 1 | 1 | Autodetect (PAL N) - NTSC M (with pedestal) |
| 0 | 1 | 0 | 0 | NTSC M (without pedestal) |
| 0 | 1 | 0 | 1 | NTSC M (with pedestal) |
| 0 | 1 | 1 | 0 | NTSC 4.43 (without pedestal) |
| 0 | 1 | 1 | 1 | NTSC 4.43 (with pedestal) |
| 1 | 0 | 0 | 0 | PAL BGHID (without pedestal) |
| 1 | 0 | 0 | 1 | PAL N (= PAL BGHID (without pedestal)) |
| 1 | 0 | 1 | 0 | PAL M (without pedestal) |
| 1 | 0 | 1 | 1 | PAL M (with pedestal) |
| 1 | 1 | 0 | 0 | PAL combination N |
| 1 | 1 | 0 | 1 | PAL combination N (with pedestal) |
| 1 | 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | 1 | Reserved |



*Table xx. Input Video Standard Selection Table*

## VIDEO SELECTION (SUBADDRESS 01H)

### ASE AUTOMATIC STARTUP ENABLE (D7)

This ASE bit is used to trigger a re-aquire in the ADV7183, this will result in the decoder relocking to a new video source and extracting the new timing information from this source. If this bit is set to 1 then on a change in INSEL the decoder will automatically start a re-aquire of the new video source. This enables faster locking to the new video source. Note this bit should be set to 0 when using Genlock mode.

| ASE | Function |
|---|---|
| 0 | If INSEL changes it will not cause a re-acquire by the decoder |
| 1 | If INSEL changes it will trigger a re-acquire by the decoder |

*Table xx. Automatic Startup Enable*



### SQPE SQUARE PIXEL ENABLE (D2)

This SQPE bit when set to a logic 1 enables SQUARE PIXEL mode. This mode outputs the Video data (P19 : P0)at a clock rates of 24.5454MHz for NTSC and 29.5MHz for PAL. When SQPE is set to a logic 0 the decoder outputs the video data (P19 : 0) at the CCIR656 Clock rate of 27MHz for both PAL and NTSC.

| SQPE | Function |
|---|---|
| 0 | Select standard 27MHz CCIR656 mode |
| 1 | Select Square Pixel mode (24.5454Mhz NTSC 29.5MHz PAL) |

*Table xx. Square Pixel Enable*

**VID_QUAL VIDEO QUALITY SELECTION (D1-D0)**

The VID_QUAL bits are used to select the type of video source being decoded by the ADV7183. The ADV7183 can decode the video more effectively when the user programs the desired video input type being decoded. For whichever video source is selected the decoder will adapt according and deliver the maximum perfromance for the selected video source. Table xx shows the four possilbe modes the ADV7183 can be configured to.

| VID_QUAL.1 | VID_QUAL.0 | Function |
|---|---|---|
| 0 | 0 | Configures decoder to decode Broadcast quality video stable signal amplitudes and timing |
| 0 | 1 | Configures decoder to decode TV quality video variable signal amplitudes and stable timing |
| 1 | 0 | Configures decoder to decode VCRt quality video variable signal amplitudes and instable timing |
| 1 | 1 | Configures decoder to decode Broadcast quality video variable signal amplitudes, stable timing and fast acquire |

*Table xx. Automatic Startup Enable*



## VIDEO ENHANCEMENT CONTROL (SUBADDRESS 02H)

**COR[1 : 0] CORING SELECTION (D4-D3)**

This COR[1 : 0] bits are used to control optional Coring of the Lumainance output signal depending on its level, see Table xx below for options. Coring is used to reduce visual artefacts within black areas of the screen by clipping values to 0 if they are below a certain threshold.

| COR1 | COR0 | Function |
|---|---|---|
| 0 | 0 | No coring |
| 0 | 1 | Truncate if Y value is less than black +8 |
| 1 | 0 | Truncate if Y vlaue is less than black +16 |
| 1 | 1 | Truncate if Y value is less than black +32 |

*Table xx. Coring Selection*

**YPM[2 : 0] LUMINANCE PEAKING FILTER MODES (D2-D0)**

The YPM[2 : 0] bits are used to select the Luminance Peaking filter response, Table xx shows the available response selections. These filters enables luma boost / attenuation of the signal centred around the color subcarrier frequency of both PAL and NTSC frequencies. These filters have the effect of enhancing the picture and improving thepicture contrast.

| YPM2 | YPM1 | YPM0 | Filter Responses | |
|---|---|---|---|---|
| | | | CVBS mode | S-Video Mode |
| 0 | 0 | 0 | PC1 | PS1 |
| 0 | 0 | 1 | PC1 | PS1 |
| 0 | 1 | 0 | PC1 | PS2 |
| 0 | 1 | 1 | PC2 | PS3 |
| 1 | 0 | 0 | PC3 | PS4 |
| 1 | 0 | 1 | PC4 | PS5 |
| 1 | 1 | 0 | PC5 | PS6 |
| 1 | 1 | 1 | PC6 | PS6 |

*Table xx. Luminance Paeking Filter Modes*



## OUTPUT CONTROL (SUBADDRESS 03H)

**VBI VERTICAL BLANKING INTERVAL DATA ENABLE ( D7 )**

This VBI enable bit allows data such as Closed Captioning and Intercast data to be passed through the Video Decoder with no filtering performed on the data. This data is often referred to as "RAW ADC Data". All data from lines 1 to 21 are passed through and available at the output port (P19 : P0). These VBI lines are marked as being invalid by the DVALIVD signal.

| VBI_EN | Function |
|---|---|
| 0 | All video lines including those in the VBI are filtered and sclaeable |
| 1 | No scaling/filtering is allowed on VBI lines 1to 21, VBI data is RAW ADC samples |

*Table xx. Vertical Blanking Interval Data Enable*

**TOD TRI-STATE OUTPUT DRIVERS (D6)**

The tod bit allows the user to Tri-state the output drivers of the ADV7815 regardless of the $\overline{OE}$ pin status.

| TOD | Function |
|---|---|
| 0 | Output drivers working according to $\overline{OE}$ pin polarity |
| 1 | Output drivers tri-state regardless of $\overline{OE}$ pin |

*Table xx. Tri-state Output Enable*

**OF_SEL[3 : 0] OUTPUT FORMAT SELECTION (D5-D2)**

The OF_SEL[3 : 0] bits are used to select the different pixel output formats for the decoder. Table xx shows all the possible pixel output configurations for the ADV7183.

| OF_SEL3 | OF_SEL2 | OF_SEL1 | OF_SEL0 | Output Format | P[15 : 8] | P[7 : 0] |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | - | - | - |
| 0 | 0 | 0 | 1 | - | - | - |
| 0 | 0 | 1 | 0 | 16bit @LLC2<br>4:2:2 CCIR656 | Y[7 : 0] | C[7 : 0] |
| 0 | 0 | 1 | 1 | 8bit @LLC1<br>4:2:2 CCIR656 | Y[7 : 0]<br>C[7 : 0] | tri-state |
| 0 | 1 | 0 | 0 | 12bit @LLC2<br>4:1:1 | Y0[7 : 0]<br>Y1[7 : 0]<br>Y2[7 : 0]<br>Y3[7 : 0] | Cb[ 7 : 6], Cr[ 7 : 6]<br>Cb[ 5 : 4], Cr[ 5 : 4]<br>Cb[ 3 : 2], Cr[ 3 :2]<br>Cb[ 1 : 0], Cr[ 1: 0] |
| 0 | 1 | 0 | 1 | - | - | - |
| 0 | 1 | 1 | 0 | - | - | - |
| 0 | 1 | 1 | 1 | - | - | - |
| 1 | 1 | 1 | 1 | - | - | - |



*Table xx. Output Format Selection*

**OM_SEL[1 : 0] OUTPUT FORMAT SELECTION (D1-D0)**

The OM_SEL[1 : 0] bits are used to select the output mode in terms of the timing and the interface type. Table xx shows the three possible output modes and the mulit-function pin assignments.

| OM_SEL1 | OM_SEL0 | FUNCTION | PIN FUNCTION AS RESULT OF MODE SELECTION | | | | |
|---|---|---|---|---|---|---|---|
| | | | H, V, FIELD | HREF, VREF | RD | DV | HFF / QCLK / GL |
| 0 | 0 | Line Locked Clock Interface | H = HS<br>V = VS<br>FILED= FIELD | HREF = HREF<br>VREF = VFREF | n.c. | DV | GL |
| 0 | 1 | SCAPI<br>Self Clocking<br>Asynchronous<br>Pixel Interface | H = HACTIVE<br>V = VACTIVE<br>FIELD = FIELD | HREF = $\overline{\text{HRESET}}$<br>VREF= $\overline{\text{VRESET}}$ | n.c. | DVALID | QCLK |
| 1 | 0 | CAPI<br>Clocked<br>Asynchronous<br>Pixel Interface | H = HACTIVE<br>V = VACTIVE<br>FIELD = FIELD | HREF = $\overline{\text{HRESET}}$<br>VREF= $\overline{\text{VRESET}}$ | RD | DVALID | HFF |
| 1 | 1 | Not used | - | - | - | - | - |

*Table xx. Output Mode Selection*

## EXTENDED OUTPUT CONTROL (SUBADDRESS 04H)

### RANGE DATA RANGE SELECTION ( D0 )

The RANGE bit control the Luminance and Chrominance data ranges and activates a limiter. Table xx shows thye two available ranges which can be used for the ADV7183.

| RANGE | Function |
|---|---|
| 0 | Luminance Data range is code 16 - 235<br>Chrominance Data range is code 16 - 240 |
| 1 | Luminance Data range is code 1 - 254<br>Chrominance Data range is code 1 - 254 |

*Table xx. Data Range Selection*

## GENERAL PURPOSE OUTPUT (SUBADDRESS 05H)



### GPEH GENERAL PURPOSE ENABLE HIGH ( D5 )

The GPEH is used to control the output drivers on the GPO[3 : 2], table xx shows the bit assignment.

| GPEH | Function |
|---|---|
| 0 | GP[3 : 2] outputs tri-state |
| 1 | GP[3 : 2] outputs enabled |

*Table xx. General Purpose Enable high*

### GPEL GENERAL PURPOSE ENABLE LOW ( D4 )

The GPEL is used to control the output drivers on the GPO[1 : 0], table xx shows the bit assignment.

| GPEL | Function |
|---|---|
| 0 | GP[1 : 0] outputs tri-state |
| 1 | GP[1 : 0] outputs enabled |

*Table xx. General Purpose Enable low*

### GP0[3 : 0] GENERAL PURPOSE OUTPUT ( D3-D0)

The GPO[3 : 0]bits are used to control the GPO[3 : 0] output pins, table xx shows the bit assignments. A logic high or low can be driven on each of the four general purpose outputs.

| GPO3 | GPO2 | GPO1 | GPO0 | Function |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | GPO[3 : 0] drivers output logic 0 |
| - | - | - | - | |
| 1 | 1 | 1 | 1 | GPO[3 : 0] drivers output logic 1 |

*Table xx. General Purpose Enable low*

## FIFO CONTROL (SUBADDRESS 07H)

### FFST FIFO FLAG SELF TIME ( D7 )

This FFST bit selects whether the FIFO flags AEF, AFF and HFF are output synchronous to the clock provided by the user via CLKIN pir or whether they are sel-timed using the internal 27MHz system clock within the ADV7183. If timed from the CLKIN pin then the FIFO flages will change sychronously with the rising edge of the clock. This however means that the user must provide a continuously running clock to the ADV7183 otherwise the flags will never change state. In the self-timed mode the flags are clocked from the internal 27MHz clock and are thus toggling if the user does not provide a continuous clock. This could be used to interrupt a statemachine or CPU which will handle reading the data from the FIFO.

| FFST | Function |
|---|---|
| 0 | FIFO Flags are timed of CLKIN (not self-timed) |
| 1 | FIFO Flags are timed of 27MHz (self-timed) |

*Table xx. FIFO Flag Self Time*



### AFR AUTOMATIC FIFO RESET (D6)

The AFR bit controls a function by which the FIFO is automatically reset at the end of a field of video. Any remaining pixel data in the FIFO will be cleared so that it is empty at the start of the next filed. Table xx shows the polarity assignment of this bit. Please note that this bit is not active in OM_SEL[1 : 0] is configured for Line Locked Clock Interface ( OM_SEL[1 : 0] = 0,0).

| AFR | Function |
|---|---|
| 0 | No automatic reset of the output FIFO |
| 1 | FIFO automatically reset at end of every field |

*Table xx. Automatic FIFO Reset*

### FR FIFO RESET (D5)

If the FR bit is set to 1 this will cause the FIFO to reset. After the reset is executed this bit will be cleared itself. The FIFO reset is executed immediately, a reset to the FIFO means that all read pointers are set to location zero. Note this bit is not active in OM_SEL[1 : 0] is configured for Line Locked Clock Interface ( OM_SEL[1 : 0] = 0,0).

| FR | Function |
|---|---|
| 0 | Normal FIFO operation |
| 1 | Reset FIFO output immediately, this bit is cleared automatically after the reset is applied. The reset FIFO resets the internal pointer to start location |

*Table xx. FIFO Reset*

**FFM[4 : 0] FIFO FLAG MARGIN (D4-D0)**

The FFM[2 : 0] bits are used to program at which physical location within the FIFO the FIFO flags AEF and AFF become active. The margin is symmetrical for both the empty and full flag. Table xx shows the range of progammability for these flags.
Example: with the FIFO total size of 256 and FFM[4 : 0]= 5'd23, the AEF will signal that less or equal to 23 locations within the FIFO are filled. The AFF will become active when 256-23 = 233 locations within the FIFO are filled.

| FFM[4 : 0] | Function |
|---|---|
| 0 | Forbidden value, latency in generating FIFO flags(AFF/AEF) will result in FIFO overflowning before user has time to empty the FIFO |
| 8 | FIFO Flags AFF/AEF are generated when the FIFO is 8 words from being full. This is the minimum allowable FIFO Flag Margin, user will have time to empty FIFO as FLAG is generated a few clock cycles before FIFO is full/empty |
| 32 | FIFO Flags AFF/AEF are generated when the FIFO is 32words from being full. |

*Table xx. FIFO Flag Margin*

## CONTRAST CONTROL (SUBADDRESS 08H)



**CON[7 : 0] CONTRAST CONTROL (D7-D0)**

The CON[7 : 0]bits are used to control the contrast of the video signal, Table xx shows the range of control.

| CON[7 : 0] | GAIN |
|---|---|
| 0 | 0 (Luminance off) |
| 128 | 1 (Luminance gain = 1) |
| 255 | 1.992 (maximum Luminance gain) |

*Table xx. Contrast Control*

## SATURATION CONTROL (SUBADDRESS 09H)

**SAT[7 : 0] SATURATION CONTROL (D7-D0)**

The SAT[7 : 0]bits are used to control the saturation of the video signal, Table xx shows the range of control.

| SAT[7 :0] | GAIN |
|---|---|
| 0 | 0 (color off) |
| 128 | 1 (color gain =1) |
| 255 | 1.992 (maximum color gain) |

*Table xx. Saturation Control*

## BRIGHTNESS CONTROL (SUBADDRESS 0AH)

**BRI[7 : 0] BRIGHTNESS CONTROL ( D7-D0 )**

The BRI[7 : 0]bits are used to control brightness of the video signal, Table xx shows the range of control.

| BRI[7 : 0] | OFFSET |
|---|---|
| 0 | 0 (no brightness added) |
| 1 | 8 |
| 127 | 1016 (mamimum brightness setting) |
| 128 | -1024 |
| 255 | -8 (maximum darkness setting) |

*Table xx. Brightness Control*

## HUE CONTROL (SUBADDRESS 0BH)

**HUE[7 : 0] HUE CONTROL ( D7-D0 )**

The HUE[7 : 0]bits are used to control brightness of the video signal, Table xx shows the range of control.



| HUE{7 : 0] | HUE PHASE (DEG) |
|---|---|
| 0 | 0.0° |
| 1 | +0.7° |
| 2 | +1.4° |
| ... | ... |
| 127 | +89.3° |
| 128 | -90.0° |
| 129 | -89.3° |
| ... | ... |
| 255 | -0.7° |

*Table xx. Hue Control*

## DEFAULT VALUE Y (SUBADDRESS 0CH)

**DEF_Y[5 : 0] DEFAULT VALUE Y ( D7-D2 )**

The DEF_Y[5 : 0]bits are used output a default Y or Luminance value on the pixel output port (P0-P15). This Y value can be forced onto to output (using DEF_VAL_EN) or output when cropping is selected or when lock of the video source is lost.

| DEF_Y[5 : 0] | Function |
|---|---|
| 6 bit value | Default Y value<br>8 bit mode Y[7:0] = {DEF_Y[5:0],0,0} , range 0 - 252 |

*Table xx. Defauly Value Y*

**DEF_VAL_AUTO_EN DEFAULT VALUE AUTOMATIC ENABLE ( D1 )**

The DEF_VAL_AUTO_EN bits is used to enable the DEF_Y & DEF_C values to be used when Lock is lost or when Croppong is enabled.

| DEF_VAL_AUTO_EN | Function |
|---|---|
| 0 | Don't use default Y, Cr and Cb values if Cropping or if Lock is lost |
| 1 | Use default Y, Cr and Cb values if Cropping or if Lock is lost |

*Table xx. Defauly Value Automatic Enable*

**DEF_VAL_EN DEFAULT VALUE ENABLE ( D0)**

The DEF_VAL_EN bits is used to force the DEF_Y & DEF_C values to be used in all cases.

| DEF_VAL_EN | Function |
|---|---|
| 0 | Don't force the use of default Y, Cr and Cb values |
| 1 | Always use default Y, Cr and Cb values |

*Table xx. Defauly Value C*



## DEFAULT VALUE C (SUBADDRESS 0DH)

**DEF_C[7 : 0] DEFAULT VALUE C ( D7-D0 )**

The DEF_C[7 : 0]bits are used output a default C or Chrominance value on the pixel output port (P0-P19). This C value (Cb & Cr) can be forced onto to output (using DEF_VAL_EN) or output when cropping is selected or when lock of the video source is lost.

| DEF_C[7 : 0] | Function |
|---|---|
| 8 bit value | Default Cb & Cr values<br>8/16 bit mode Cr[7:0] = {DEF_C[7 : 4],0,0,0,0} , range 0 - 240<br>8/16 bit mode Cb[7:0] = {DEF_C[3 : 0],0,0,0,0} , range 0 - 240 |

*Table xx. Defauly Value C*

## TEMPORAL DECIMATION (SUBADDRESS 0EH)

**TDR[3 : 0]TEMPORAL DECIMATION RATE ( D6-D3 )**

The TDR[3 : 0]bits control how many fields/frames (as specified in the TDC[1 : 0] register) are to be skipped before a valid one is output.

| TDR3 | TDR2 | TDR1 | TDR | Function |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Skip no field/frame between valid output |
| 0 | 0 | 0 | 1 | Skip 1 field/frame between valid output |
| ... | ... | ... | ... | Skip .... field/frame between valid output |
| 1 | 1 | 1 | 1 | Skip no field/frame between valid output |

*Table xx. Temporal Decimation Rate*

**TDC[1 : 0]TEMPORAL DECIMATION CONTROL ( D2-D1 )**

The TDC[1 : 0]bits control the supperssion of selected fileds of video as shown in Table xx.

| TDC1 | TDC0 | Function |
|---|---|---|
| 0 | 0 | Suppress frames, start with even field |
| 0 | 1 | Suppress frames, start with odd field |
| 1 | 0 | Suppress even fields only |
| 1 | 1 | Suppress odd fields only |

*Table xx. Temporal Decimation Control*

## POWER MAMAGEMENT (SUBADDRESS 0FH)

**RES RESET CONTROL ( D7)**

The RES bit when set will generate a Reset. The $\overline{\text{RESET}}$ will be pulled to a logic low and then go high again after a short period of time. All $I^2C$ registers will be reset to their default values. After a reset sequence the ADV7183 starts to acquire the incoming video signal.

| RES | Function |
|---|---|
| 0 | Normal operation |
| 1 | Start Reset sequence, all register will be reset to their default values and the $\overline{\text{RESET}}$ pin will be pulled low for a short duration. |

*Table xx. Reset Control*



**TRAQ TIMING RE-ACQUIRE ( D6)**

The TRAQ bit when set will result in the ADV7183 re-acquiring the video signal and is a software version of the ISO pin function. Setting this bit will result in a shorter time that it takes the ADV7183 to acquire a new video signal since the decoder does not have to first determine that lost was locked. Once set this bit will be automatically cleared. The function of this bit is equivalent to a rest of the ADV7183 without re-intialising the I2C registers again. The RESET is unaffected by this control bit.

| TRAQ | Function |
|---|---|
| 0 | Normal operation |
| 1 | Start re-acquire of video signal immediately |

*Table xx. Timing Re-acquire*

**PWRDN POWER DOWN CONTROL ( D5)**

The PWRDN bit when set puts the ADV7183 in a shut down mode whereby only a ver small current is consumed by the decoder.

| PWRDN | Function |
|---|---|
| 0 | Normal operation |
| 1 | Power down part in ultra low current mode |

*Table xx. Power Down control*

**PS_CG POWER SAVE LLC CLOCK GENERATOR ( D4)**

The PS_CG bit when set puts the ADV7183 LLC Clock generator in power down mode and as a result the clock output is switched off.

| PS_CG | Function |
|---|---|
| 0 | LLC Clock generator in normal operation |
| 1 | LLC Clock generator in power save mode |

*Table xx. Power Save LLC Clock Generator*

**PS_REF POWER SAVE REFERENCE ( D3)**

The PS_REF bit when set puts the ADV7183 internal voltage reference in power down mode.

| PS_REF | Function |
|---|---|
| 0 | Analog voltage reference normal operation |
| 1 | Analog voltage reference power save mode |

*Table xx. Power Save Reference*



**PDBP POWER DOWN BIT PRIORITY ( D2)**

The PDBP bit sets weither the PWRDN pin or the I2C PWRDN(D5) bit has highest priority to put the ADV7183 in Power down mode.

| PDBP | Function |
|---|---|
| 0 | $\overline{\text{PWRDN}}$ pin has highest priority. |
| 1 | PWRDN $I^2C$ bit has highest priority. |

*Table xx. Power down bit proority*

**PSC [1 : 0] POWER SAVE CONTROL ( D1-D0)**

The PSC[1 : 0] bits allow for a variety of power save modes to be selected, see Table xx for more details.

| PSC1 | PSC0 | Function |
|---|---|---|
| 0 | 0 | Normal operation |
| 0 | 1 | Enable Power Saving mode for CVBS input only |
| 1 | 0 | Enable power down of digital core scetion and leave analog front end powered on |
| 1 | 1 | Enable Power Save mode which enables faster power on than PWRDN but consumes more current than the PWRDN state |

*Table xx. Power Save Control*

## STATUS REGISTER (SUBADDRESS 10H)

**STATUS[ 7 : 0] STATUS REGISTER ( D7-D0 )**

This STATUS [7 : 0] is a read only register. Table xx list the status bits which can be read back fron this register to help the user use the part more effectively.

| STATUS [7 : 0] | STATE | Function (Read only register) |
|---|---|---|
| STATUS[0] | 1 | Horizontal locked right now |
| STATUS[0] | 0 | Lost Horizontal Lock |
| STATUS[1] | 1 | Lost lock since last read of Status register |
| STATUS[1] | 0 | No lock lost since last read of Status register |
| STATUS[2] | 1 | Fsc locked right now |
| STATUS[2] | 0 | Fsc not locked |
| STATUS[3] | 1 | 50Hz field rate auto detected |
| STATUS[3] | 0 | 60Hz filed rate auto detected |
| STATUS[4] | 1 | ADC underflow detected |
| STATUS[4] | 0 | No ADC underflow detected |
| STATUS[5] | 1 | ADC overflow detected |
| STATUS[5] | 0 | No ADC overflow detected |
| STATUS[6] | 1 | White Peak Mode now active |
| STATUS[6] | 0 | White Paek mode is not active |
| STATUS[7] | 1 | Reserved |
| STATUS[7] | 0 | Reserved |



*Table xx. Status Register*

## INFO REGISTER (SUBADDRESS 11H)

**IDENT[ 2 : 0] INFO REGISTER ( D2-D0 )**

This IDENT[3 : 0] is a read only register. This register contains the revision code for the silicon.

| IDENT [2 : 0] | Function (Read only register) |
|---|---|
| 000 | Revision 1.0 Code |
| ..... | Reserved |
| 111 | Reserved |

*Table xx. Info Register*

# ADVANCED USER REGISTER MAP

## ANALOG CLAMP CONTROL (SUBADDRESS 14H)

### VCLEN VOLTAGE CLAMP ENABLE (D5)

The VCLEN bit allows the user to turn on and off the voltage clamp circuit in the ADV7183 front end.

| VCLEN | Function |
|---|---|
| 0 | Voltage Clamp disabled |
| 1 | Voltage Clamp enabled |

*Table xx. Voltage Clamp enable*

### CCLEN CURRENT CLAMP ENABLE (D4)

The CCLEN bit allows the user to turn on and off the current clamp circuit in the ADV7183 front end.

| CCLEN | Function |
|---|---|
| 0 | Current Clamp disabled |
| 1 | Current Clamp enabled |

*Table xx. Current Clamp enable*



### FACL[1 : 0] FAST CLAMP LENGHT (D3-D2)

The FACL[1 : 0] bits allows the user to select the number of clock cycles the fast current clamp is switched on for on each video line. Table xx shows the possible ranges which can be selected.

| FACL 1 | FACL 0 | Function |
|---|---|---|
| 0 | 0 | Current source switched on for 16 clock cycles |
| 0 | 1 | Current source switched on for 32 clock cycles |
| 1 | 0 | Current source switched on for 64 clock cycles |
| 1 | 1 | Current source switched on for 128 clock cycles |

*Table xx. Fast Clamp Lenght*

### FICL[1 : 0] FINE CLAMP LENGHT (D1-D0)

The FICL[1 : 0] bits allows the user to select the number of clock cycles the fine current clamp is switched on for on each video line. Table xx shows the possible ranges which can be selected.

| FICL 1 | FICL 0 | Function |
|---|---|---|
| 0 | 0 | Current source switched on for 16 clock cycles |
| 0 | 1 | Current source switched on for 32 clock cycles |
| 1 | 0 | Current source switched on for 64 clock cycles |
| 1 | 1 | Current source switched on for 128 clock cycles |

*Table xx. Fine Clamp Lenght*

## DIGITAL CLAMP CONTROL (SUBADDRESS 15H)

### DCCM DIGITAL COLOUR CLAMP MODE (D7)

The DCCM bit allows the user to select automatic digital clamp or manual clamp mode whereby the user can set a desired clamp offset value.

| DCCM | Function |
|---|---|
| 0 | Automatic Digital Clamp enabled |
| 1 | Manual offset correction via DCCO[11 : 0] for C only |

*Table xx. Digital Colour Clamp mode*

### DCT [1 : 0] DIGITAL CLAMP TIMING (D6-D5)

The DCT[1 : 0] bits allows the user to select the desired time constant for the digital clamping circuit in the ADV7183.

| DCT 1 | DCT 0 | Function |
|---|---|---|
| 0 | 0 | Slow clamp timing (time constant = 1sec) |
| 0 | 1 | Medium clamp timing (time constant = 0.5sec) |
| 1 | 0 | Fast clamp timing (time constant = 0.1sec) |
| 1 | 1 | Dependent on VID_QUAL selected |

*Table xx. Digital Clamp Timing*



### DCFE DIGITAL CLAMP FREEZE ENABLE(D4)

This register bit allows to freeze the digital clamp loop at any point in time. It is intended mainly for users who would like to do their own clamping. They should disable the current sources for analog clamping via the appropriate register bits and then freeze the digital clamp loop after letting it settle via the DCFE bit. This bit affects the digital clamp loops in both Y and C path.

| DCFE | Function |
|---|---|
| 0 | Digital Clamp loop operational |
| 1 | Digital Clamp loop frozen |

*Table xx. Digital Clamp Freeze Enable*

## DIGITAL COLOR CLAMP OFFSET (SUBADDRESS 15H)

### DCCO [1 1: 8] DIGITAL COLOUR CLAMP OFFSET (D3-D0)

## DIGITAL COLOR CLAMP OFFSET (SUBADDRESS 16H)

### DCCO[7 : 0] DIGITAL COLOUR CLAMP OFFSET (D7-D0)

The DCCO[11 : 0] bits allow the user the ADV7183 in manual offset mode. The value load here is the digital offset which is added to the output of the ADC.

| DCCO[11 : 0] | Function |
|---|---|
| 0....4095 | Manual digital clamp offset value added to ADC output |

*Table xx. Digital Colour Clamp Offset*

## SHAPING FILTER CONTROL (SUBADDRESS 17H)

### CSFM[3 : 0] CHROMA SHAPING FILTERS (D7-D5)

The CSFM[3 : 0] bits allow the user to select from a range of low pass filters for the chrominance signal, see Table xx for modes. When switched in automatic mode, then the filter is selected based on the scaling factor as selected by the user.

| CSFM 2 | CSFM 1 | CSFM 0 | Filter Responses |
|---|---|---|---|
| 0 | 0 | 0 | Auto selection 1.5Mhz |
| 0 | 0 | 1 | Auto selection 2.17Mhz |
| 0 | 1 | 0 | SH1 |
| 0 | 1 | 1 | SH2 |
| 1 | 0 | 0 | SH3 |
| 1 | 0 | 1 | SH4 |
| 1 | 1 | 0 | SH5 |
| 1 | 1 | 1 | reserved |

*Table xx. Digital Colour Clamp Offset*

**YSFM[4 : 0] LUMA SHAPING FILTERS (D4-D0)**

The YSFM[4 : 0] bits allow the user to select from a range of low pass and notch filters for the luminance signal, see Table xx for modes. When switched in automatic mode, then the filter is selected based on the video standard and the scaling factor as selected by the user.

| YSFM 4 | YSFM 3 | YSFM 2 | YSFM 1 | YSFM 0 | Filter Responses |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | Auto selection Wide Notch |
| 0 | 0 | 0 | 0 | 1 | Auto selection Narrow Notch |
| 0 | 0 | 0 | 1 | 0 | SVHS1 |
| 0 | 0 | 0 | 1 | 1 | SVHS2 |
| 0 | 0 | 1 | 0 | 0 | SVHS3 |
| 0 | 0 | 1 | 0 | 1 | SVHS4 |
| 0 | 0 | 1 | 1 | 0 | SVHS5 |
| 0 | 0 | 1 | 1 | 1 | SVHS6 |
| 0 | 1 | 0 | 0 | 0 | SVHS7 |
| 0 | 1 | 0 | 0 | 1 | SVHS8 |
| 0 | 1 | 0 | 1 | 0 | SVHS9 |
| 0 | 1 | 0 | 1 | 1 | SVHS10 |
| 0 | 1 | 1 | 0 | 0 | SVHS11 |
| 0 | 1 | 1 | 0 | 1 | SVHS12 |
| 0 | 1 | 1 | 1 | 0 | SVHS13 |
| 0 | 1 | 1 | 1 | 1 | SVHS14 |
| 1 | 0 | 0 | 0 | 0 | SVHS15 |
| 1 | 0 | 0 | 0 | 1 | SVHS16 |
| 1 | 0 | 0 | 1 | 0 | SVHS17 |
| 1 | 0 | 0 | 1 | 1 | PAL NN 1 |
| 1 | 0 | 1 | 0 | 0 | PAL NN 2 |
| 1 | 0 | 1 | 0 | 1 | PAL NN 3 |
| 1 | 0 | 1 | 1 | 0 | PAL WN 1 |
| 1 | 0 | 1 | 1 | 1 | PAL WN 2 |
| 1 | 1 | 0 | 0 | 0 | NTSC NN 1 |
| 1 | 1 | 0 | 0 | 1 | NTSC NN 2 |
| 1 | 1 | 0 | 1 | 0 | NTSC NN 3 |
| 1 | 1 | 0 | 1 | 1 | NTSC WN 1 |
| 1 | 1 | 1 | 0 | 0 | NTSC WN 2 |
| 1 | 1 | 1 | 0 | 1 | NTSC WN 3 |
| 1 | 1 | 1 | 1 | 0 | not used |
| 1 | 1 | 1 | 1 | 1 | not used |



*Table xx. Luma Shasping Filters*

## COMB FILTER CONTROL (SUBADDRESS 19H)

### CCMB_AD CHROMA COMB ADAPTIVE(D4)

The CCMB_AD bit controls the comb filter logic. If set to logic high the comb filters are configured in an adaptive mode which allows for comb filter to change modes.

| CCMB_AD | Function |
|---|---|
| 0 | Chroma Comb filter configure for non-adaptive mode |
| 1 | Chroma Comb filter configure for adaptive mode |

*Table xx. Digital Colour Clamp Offset*

### CCM[1 : 0] CHROMA COMB MODE(D3-D2)

The CCM[1 : 0] bits controls the chroma comb filter mode slected, see Table xx for available modes.

| CCM 1 | CCM 0 | Function |
|---|---|---|
| 0 | 0 | No comb selected |
| 0 | 1 | 1H Comb enabled |
| 1 | 0 | 2H Conmb enabled |
| 1 | 1 | reserved |

*Table xx. Chroma Comb mode*



### LCM[1 : 0] LUMA COMB MODE(D1-D0)

The LCM[1 : 0] bits controls the luma comb filter mode slected, see Table xx for available modes.

| LCM 1 | LCM 0 | Function |
|---|---|---|
| 0 | 0 | No comb selected |
| 0 | 1 | 1H Comb enabled |
| 1 | 0 | 2H Conmb enabled |
| 1 | 1 | Automatic selection of highest comb |

*Table xx. Luma Comb mode*

## SCALING/CROPPING MSB ( SUBADDRESS 1AH)

### SCE SCALING ENABLE (D0)

The SCE bits allow the user to enable and diable horizontal and vertical scaling on the ADV7183. Note when scaling/cropping is enable these registers must be loaded with a specific valid value as their value will be undetermined unless the register has been written to.

| SCE | Function |
|---|---|
| 0 | Scaling disabled |
| 1 | Scaling enabled |

*Table xx. Scaling Enable*

## ACTIVE VIDEO DESIRED LINES (SUBADDRESS 1BH)

### AVDL[7: 0] ACTIVE VIDEO DESIRED LINES (D7-DO)

## SCALING/CROPPING MSB (SUBADDRESS 1AH)

### AVDL [8] ACTIVE VIDEO DESIRED LINES (D7)

TheAVDL[8 : 0] bits allow the user to select the number of active video lines that are output. This register must be programmed for scaling/cropping to work properly, Table xx shoes the valid range which can be programmed. Note when scaling/cropping is enable these registers must be loaded with a specific valid value as their value will be undetermined unless the register has been written to.

| AVDL[8 : 0] | Function |
|---|---|
| 0 | Number of active video lines = 0 lines |
| 240 | CCIR number of active lines for NTSC |
| 287 | CCIR number of active lines for PAL |
| 241....512 | Forbidden values in this range in NTSC |
| 289....512 | Forbidden values in this range in PAL |

*Table xx. Active Video Desired Lines*

## ACTIVE IVDEO VERTICAL BEGIN (SUBADDRESS 1CH)

### AVVB[7: 0] ACTIVE VIDEO VERTICAL BEGIN (D7-DO)

## SCALING/CROPPING MSB (SUBADDRESS 1AH)

### AVVB [8] ACTIVE VIDEO VERTICAL BEGIN (D6)

TheAVVB[8 : 0] bits allow the user to select which line the first active video line is output on.This register must be programmed for scaling/cropping to work properly, Table xx shoes the valid range which can be programmed. Note when scaling/cropping is enable these registers must be loaded with a specific valid value as their value will be undetermined unless the register has been written to.

| AVVB[8 : 0] | Function |
|---|---|
| 0...21 | Forbidden values |
| 22-262 | Valid range for NTSC active video begin value |
| 23-310 | Valid range for PAL active video begin value |
| 311....512 | Forbidden values |

*Table xx. Active Video Vertical Begin*

## VERTICAL SCLE VALUE 1 (SUBADDRESS 1DH)

**VSCV[10 : 8] VERTICAL SCALE VALUE (D2-D0)**

## VERTICAL SCLE VALUE 2 (SUBADDRESS 1EH)

**VSCV[7 : 0] VERTICAL SCALE VALUE (D7-D0)**

The VSCV[10 : 0] bits allow the user to control the vertcal scaling factor, the formula used for scaling can be viewed earlier in this document. Table xx shows the valid range for scaling. Note when scaling/cropping is enable these registers must be loaded with a specific valid value as their value will be undetermined unless the register has been written to.

| VSCV[10 : 0] | Function |
|---|---|
| 0...255 | Scaling range for a scaling factor below 1 |
| 256 | Default Vertical scaling value, a scaling factor of 1 |
| 257...2047 | Forbidden values in this range |

*Table xx. Vertical Scaling Value*

## ACTIVE VIDEO HORIZONTAL BEGIN (SUBADDRESS 1FH)

**AVVB[8 : 1] ACTIVE VIDEO HORIZONTAL BEGIN (D7-D0)**

## SCALING/CROPPING MSB (SUBADDRESS 1AH)

**AVVB[9] ACTIVE VIDEO HORIZONTAL BEGIN (D5)**



The AVVB[9 : 1] bits allow the user to select the number of the first video sample pixel to be output by the ADV7183. Note that this position control is in minimum increments off 1 pixel (2 clock cycles).Also it should be noted that when scaling/cropping is enable these registers must be loaded with a specific valid value as their value will be undetermined unless the register has been written to.

| AVHB[9 : 1] | Function |
|---|---|
| 0 | First pixel output after falling edge of Hsync |
| 61 | CCIR value for first active video pixel for NTSC |
| 66 | CCIR value for first active video pixel for PAL |
| 511 | Maximum value for first video pixel |

*Table xx. Active Video Horizontal begin*

## ACTIVE VIDEO DESIRED PIXEL (SUBADDRESS 20H)

**AVDP[7 : 0] ACTIVE VIDEO DESIRED PIXEL (D7-D0)**

## SCALING/CROPPING MSB (SUBADDRESS 1AH)

**AVVB[9 : 8] ACTIVE VIDEO DESIRED PIXEL (D4-D3)**

The AVDP[9 : 0] bits allow the user when cropping/scaling to specify the total number of video samples which is output by the ADV7183. Note when scaling/cropping is enable these registers must be loaded with a specific valid value as their value will be undetermined unless the register has been written to.

| AVDP[9 : 0] | Function |
|---|---|
| 0 | no pixels output |
| 720 | Mamimum number of pixels allowed (720 pixels on a line) |
| 721..1023 | Forbidden range for this control |

*Table xx. Active Video Desired Pixel*



## HORIZONTAL SCALE VALUE 1 (SUBADDRESS 21H)

**HSCV[15 : 8] ACTIVE VIDEO DESIRED PIXEL (D7-D0)**

## HORIZONTAL SCALE VALUE 2 (SUBADDRESS 22H)

**HSCV[7 : 0] ACTIVE VIDEO DESIRED PIXEL (D7-D0)**

The HSCV[15 : 0] bits allow the user to select the horizontal scaling factor, the formula used for scaling can be viewed earlier in this document. Note when scaling/cropping is enable these registers must be loaded with a specific valid value as their value will be undetermined unless the register has been written to.

| HSCV[15 : 0] | Function |
|---|---|
| 0 | No video pixel output |
| 2427 | Default value for a scaling factor 1for PAL |
| 2444 | Default value for a scaling factor 1for NTSC |
| 2445...65,535 | forbidden values in this range |

*Table xx. Horizontal Scaling Value*

## COLOR SUBCARRIER CONTROL 1 (SUBADDRESS 24H)

**CSM COLOR SUBCARRIER MANUAL (D4)**

The CSM bit allow the user to overide any subcarrier frequency pre-selected by the video input bits. It works in conjunction with the CSMF[27 : 0] register.

| CSM | Function |
|---|---|
| 0 | Manual Fsc selection disabled |
| 1 | Use Fsc as specified in CSMF[27: 0], manual Fsc enabled |

*Table xx. Color Subcarrier Manual Enable*

## COLOR SUBCARRIER CONTROL 1 (SUBADDRESS 24H)

**CSMF[27 : 24] COLOR SUBCARRIER MANUAL FREQUENCY(D3-D0)**

## COLOR SUBCARRIER CONTROL 2 (SUBADDRESS 25H)

**CSMF[23 : 16] COLOR SUBCARRIER MANUAL FREQUENCY(D7-D0)**

## COLOR SUBCARRIER CONTROL 3 (SUBADDRESS 26H)

**CSMF[15 : 8] COLOR SUBCARRIER MANUAL FREQUENCY(D7-D0)**

## COLOR SUBCARRIER CONTROL 4 (SUBADDRESS 27H)

**CMSF[7 : 0] COLOR SUBCARRIER MANUAL FREQUENCY(D7-D0)**



The CSMF[27 : 0] bits allow the user to programme a desired subcarrier frequency when the CSM bit is enabled. The CSMF{27 : 0] control the internal DDFS to generate the user defined frequency. The formula for calculating the subcarrier frequency is shown earlier in this document.

| CSMF[27 : 0] | Function |
|---|---|
| 0...2000 | Forbidden range for subcarrier frequency |
| 35,588,034 | Default NTSC value for a subcarrier of 3.579545MHz |
| 44,079,277 | Default PAL B/D/G/H/I value for a subcarrier of 4.43361875MHz |
| 35,548,922 | Default PAL M value for a subcarrier of 3.57561149MHz |
| 35,612,996 | Default PAL Combinational N value for a subcarrier of 3.58205625MHz |

*Table xx. Color Subcarrier Manual Frequency*

## PIXEL DELAY CONTROL (SUBADDRESS 28H)

**SWPC SWAP PIXEL CB/CR(D7)**

The SWPC bit allow the user to swap the Cb and Cr samples on the video output port. This is usedul for timing alignment.

| SWPC | Function |
|---|---|
| 0 | No swapping of Cr and Cb values |
| 1 | Swap Cr and Cb values |

*Table xx. Swap Pixel Cb/Cr*

**CTA[2 : 0] CHROMA TIMING ADJUST (D5-D3)**

The CTA[2 : 0] bits allow the user to adjust the timing differences between the chroma and the luma samples. The range for chroma to lumma delay varies from +2 pixels to -3pixels.

| CTA 2 | CTA 1 | CTA 0 | Function |
|---|---|---|---|
| 0 | 0 | 0 | reserved |
| 0 | 0 | 1 | Chrominance delayed by 2 pixels with respect to Luminance |
| 0 | 1 | 0 | Chrominance delayed by 1 pixels with respect to Luminance |
| 0 | 1 | 1 | No delay on Chrominance or Luminance channels |
| 1 | 0 | 0 | Luminance delayed by 1 pixels with respect to Chrominance |
| 1 | 0 | 1 | Luminance delayed by 2 pixels with respect to Chrominance |
| 1 | 1 | 0 | Luminance delayed by 3 pixels with respect to Chrominance |
| 1 | 1 | 1 | reserved |

*Table xx. Chroma Timing Adjust*



## MANUAL CLOCK CONTROL 1 (SUBADDRESS 29H)

**FIX27E FIXED FREQUENCY 27MHz ENABLE(D7)**

The FIX27E bit allows the user to output the 27MHz crystal clock output via LLC1, LLC2 and LLCREF output pins. This feature is intended for usage during free run mode.

| FIX27E | Function |
|---|---|
| 0 | Ouput clock signals (LLC1 & LLC2) at a frequency determined by the clock generator (line locked) on board |
| 1 | Output a 27MHz fixed clock driven by the crystal source |

*Table xx. Fixed Frequency 27MHz Enable*

**CLKMANE CLOCK GENERATOR MANUAL ENABLE (D6)**

The CLKMANE bit configures the analog clock generator to produce a fixed clock frequency which is not dependent on the input video source. Output is acheived via LLC1, LLC2 and LLCREF output pins. Intended for usage during CAPI and SCAPI modes of operation.

| CLKMANE | Function |
|---|---|
| 0 | Clock output frequency determine by video source (LLC1) |
| 1 | Clock output frequency determined by value loaded into CLKVAL[13 : 0] |

*Table xx. Clock Generator Manual Enable*

## MANUAL CLOCK CONTROL 1 (SUBADDRESS 29H)

**CLKVAL[13 : 8] FIXED FREQUENCY VALUE (D5-D0)**

## MANUAL CLOCK CONTROL 2 (SUBADDRESS 2AH)

**CSMF[23 : 16] FIXED FREQUENCY VALUE (D7-D0)**

The CLKVAL[13 : 0] bits allow the user to programme a desired output frequency on the LLC!, LLC2 and LLCREF pins. Tablexx shows the possible programming range for this output clock. A formula for calculating this frequency is shown earlier in this document.

| CLKVAL [13 : 0] | Function |
|---|---|
| 0 | Minimum output frequency of LLC1 (2.7KHz) |
| 8826 | Output clock frequency of 24.54MHz for NTSC Square Pixel mode |
| 9709 | Output clock frequency of 27MHz for PAL/NTSC mode |
| 10608 | Output clock frequency of 29.5MHz for PAL Square Pixel mode |
| 16384 | Maximum output frequency of LLC1 (45.5625MHz) |

*Table xx. Fixed Frequency Value*



## AGC MODE CONTROL (SUBADDRESS 2CH)

**LAGC[2 : 0] LUMA AUTOMATIC GAIN CONTROL (D6-D4)**

The LAGC[2 : 0] bits control the mode of operation of the Luma Automatic Gain Cntrol block. Table xx shows the possible modes of operation.

| LAGC 2 | LAGC 1 | LAGC 0 | Function |
|---|---|---|---|
| 0 | 0 | 0 | Manual fixed gain (use LMG[11 : 0]) |
| 0 | 0 | 1 | AGC (blank level to sync tip)<br>manual maxIRE control<br>no overide through white peak |
| 0 | 1 | 0 | AGC (blank level to sync tip)<br>manual maxIRE control<br>automatic overide through white peak |
| 0 | 1 | 1 | AGC (blank level to sync tip)<br>automatic maxIRE control<br>no overide through white peak |
| 1 | 0 | 0 | AGC (blank level to sync tip)<br>automatic maxIRE control<br>automatic overide through white peak |
| 1 | 0 | 1 | AGC (active video with white peak) |
| 1 | 1 | 0 | AGC (active video with average video) |
| 1 | 1 | 1 | Freeze gain |

*Table xx. Luma Aoutomatic Gain Control*

**CAGC[2 : 0] CHROMA AUTOMATIC GAIN CONTROL (D1-D0)**

The cAGC[1 : 0] bits control the mode of operation of the Chroma Automatic Gain Cntrol block. Table xx shows the possible modes of operation.

| CAGC 1 | CAGC 0 | Function |
|---|---|---|
| 0 | 0 | Manual fixed gain use CMG[11 : 0] |
| 0 | 1 | Luminance gain used for Chrominance |
| 1 | 0 | Automatic Gain (based on colour burst) |
| 1 | 1 | Freeze Chrominance gain |

*Table xx. Chroma Automatic Gain Control*

## CHROMA GAIN CONTROL 1 (SUBADDRESS 2DH)

**CAGT[1 : 0] CHROMA AUTOMATIC GAIN TIMING (D7-D6)**

The CAGT[1 : 0] bits control the tracking speed of the Chroma AGC. Note these bits will only have effect if the CAGC[1:0] bits are set to 10(automatic gain).



| CAGT 1 | CAGT 0 | Function |
|---|---|---|
| 0 | 0 | Chroma AGC Slow |
| 0 | 1 | Chroma AGC Medium |
| 1 | 0 | Chroma AGC Fast |
| 1 | 1 | Chroma AGC dependent on VID_QUAL setting |

*Table xx. Chroma Automatic Gain Control Timing*

## CHROMA GAIN CONTROL 1 (SUBADDRESS 2DH)

**CMG[11 : 8] CHROMA GAIN (D3-D0)**

## CHROMA GAIN CONTROL 2 (SUBADDRESS 2EH)

**CMG[7 : 0] CHROMA GAIN (D7-D0)**

The CMG[11 : 0] bits act as a dual function register. If written to, a desired gain can be programmed for the chroma channel. This gain will become active if the CAGC{1 : 0] mode is switched to Manual fixed gain. If read from this register will return the currently actually used gain value for the chroma channel. Depending on the settings of the CAGC[1 : 0] bits this will be either one of the following, 1) Chroma manaul gain (CAGC[1 : 0] set to chroma manual gain mode, 2)Chroma automatic gain value (CAGC[1 : 0] set to any of the other automatic modes).

| | Mode | Function |
|---|---|---|
| **GMG[11 : 0] = X** | write | Manual gain for chrominance channel |
| **CG[11 : 0]** | read | actually used gain (same as write value if in manual gain mode or automatic gain value if in automatic gain mode) |

*Table xx. Chroma Gain*

## LUMA GAIN CONTROL 1 (SUBADDRESS 2FH)

**LAGT[1 : 0] LUMA AUTOMATIC GAIN TIMING (D7-D6)**

The LAGT[1 : 0] bits control the tracking speed of the Luma AGC. Note these bits will only have effect if the LAGC[2:0] bits are set to 001,010,011 or 100 (automatic gain control modes).

| LAGT 1 | LAGT 0 | Function |
|---|---|---|
| 0 | 0 | Luma AGC Slow |
| 0 | 1 | Luma AGC Medium |
| 1 | 0 | Luma AGC Fast |
| 1 | 1 | Luma AGC dependent on VID_QUAL setting |

*Table xx. Luma Automatic Gain Timing*

## LUMA GAIN CONTROL 1 (SUBADDRESS 2FH)

**LMG[11 : 8] CHROMA GAIN (D3-D0)**

## LUMA GAIN CONTROL 2 (SUBADDRESS 30H)

**LMG[7 : 0] LUMA GAIN (D7-D0)**



The LMG[11 : 0] bits act as a dual function register. If written to, a desired gain can be programmed for the chroma channel. This gain will become active if the LAGC[1 : 0] mode is switched to Manual fixed gain. If read from this register will return the currently actually used gain value for the luma channel. Depending on the settings of the LAGC[1 : 0] bits this will be either one of the following, 1) Luma manaul gain (LAGC[1 : 0] set to luma manual gain mode, 2)Luma automatic gain value (LAGC[1 : 0] set to any of the other automatic modes).

| LG[11 : 0] | Mode | Function |
|---|---|---|
| LMG[11 : 0] | write | Manual gain for luminance channel |
| LG[11 : 0] | read | actually used gain (same as write value if in manual gain mode or automatic gain value if in automatic gain mode) |

*Table xx. Luma Gain*

## MANUAL GAIN SHADOW CONTROL1 (SUBADDRESS 31H)

**SGUE SURVEILLANCE GAIN UPDATE ENABLE(D7)**

The SGUE when set enables an advanced feature for the surveillance mode of operation. Please refer to LMGS[11 : 0] for further details.

| SGUE | Function |
|---|---|
| 0 | Disable use of LMGS update facility |
| 1 | Use LMGS update facility |

*Table xx. Surveillance Gain Update Enable*

## MANUAL GAIN SHADOW CONTROL 1 (SUBADDRESS 31H)

**LMGS[11 : 8] LUMA GAIN STORE (D3-D0)**

## MANUAL GAIN SHADOW CONTROL 2 (SUBADDRESS 32H)

**LMGS[7 : 0] LUMA GAIN STORE (D7-D0)**

The LMGS[11 : 0] is a register store which allows the user in the surveillance mode to pre-program a gain into it. This gain value is simply stored and will be copied into the LMG[ 11 : 0] register only after the ISO pin has been toggled, the INSEL register has been changed or the TRAQ bit has been set. The register allows for the gain calibration of each channel. This function is not replicated in the chroma path, however it is suggested to adaptthe chroma gain from the luma path by setting CAGC[1 : 0] = 01.

| LMGS[11 : 0] | Function |
|---|---|
| 0...4095 | Gain for next input source which is switched (surveillance mode only) |

*Table xx. Luma Manual Gain Store*

## MISC GAIN CONTROL (SUBADDRESS 33H)

**CKE COLOR KILL ENABLE (D6)**

The CKE bit is used to control the optional color kill function to be switched on or off. If color kill is enabled, color processing will be switched off (only luma outptut) if the color burst of the incoming video signal is less than 22% of its nominal amplitude for 128 consecutive video lines. To switch the color processing back on, another 128 consecutive lines with a color burst greater than 22% of its nominal amplitude is required.



| CKE | Function |
|---|---|
| 0 | Colour Kill function disabled |
| 1 | Colour Kill function enabled |

*Table xx. Color Kill Enable*

**MIRE[2 : 0] MAX IRE(D4-D2)**

The MIRE[2 : 0] bits are used to select the maximum input IRE level which is dependent on the video standard selected. Table xx shows the possible ranges to select from.

| MIRE [2 : 0] | Function | |
|---|---|---|
| | PAL (IRE) | NTSC (IRE) |
| 0 0 0 | 133 | 122 |
| 0 0 1 | 125 | 115 |
| 0 1 0 | 120 | 110 |
| 0 1 1 | 115 | 105 |
| 1 0 0 | 110 | 100 |
| 1 0 1 | 105 | 100 |
| 1 1 0 | 100 | 100 |
| 1 1 1 | 100 | 100 |

*Table xx. Max IRE*

**AV_AL AVERAGE BRIGHTNESS ACTIVE LINES(D1)**

The gain can be determined based on the average brightness of the active video by using the average video mode in the LAGC[2 : 0] register. the AV_AL bit allows to select between two ranges of active video lines to determine the average brightness. Note that this bit can only be set to a logic high when the input signal confroms to the PAL 625 standard.

| AV_AL | Function |
|---|---|
| 0 | Use lines 33 -310 to determine average active video brightness |
| 1 | Use lines 33 -270 to determine average active video brightness |

*Table xx. Average Video Active Lines*

**PW_UPD PEAK WHITE UPDATE (D0)**

The peak white and average video algorithms determine the gain based on measurements taken from the active video. PW_UPD bit determines the rate of gain change. Note that the LAGC[2 : 0] must be set to the appropriate mode to enable the peak white or average video mode.

| PW_UPD | Function |
|---|---|
| 0 | Update gain once per video line |
| 1 | Update gain once per video field |

*Table xx. Peak White Update*



## HS POSITION CONTROL 1 (SUBADDRESS 34H)

**HSB[9 : 8] (D7-D6) HS BEGIN**

## HS POSITION CONTROL 2 (SUBADDRESS 35H)

**HSB[7 : 0] (D7-D0) HS BEGIN**

The HS Begin and HS End registers allow to freely position the HS output within the video line. The values in HSB[9 : 0] are measured in pixels units from the falling edge of HS. Using both registers the user can program both, position and lenght of the HS outptu signal.

| HSB[9 : 0] | Function |
|---|---|
| 0...863 | HSYNC pulse starts after HSB[9 : 0] pixels after falling edge of HSYNC |

*Table xx. HSYNC End*

## HS POSITION CONTROL 1 (SUBADDRESS 34H)

**HSE[9 : 8] (D5-D4) HS END**

## HS POSITION CONTROL 3 (SUBADDRESS 36H)

**HSE[7 : 0] (D7-D0) HS END**

The HS End and HS Begin registers allow to freely position the HS output within the video line. The values in HSE[9 : 0] are measured in pixels units from the falling edge of HS. Using both registers the user can program both, position and lenght of the HS outptu signal.

| HSE[9 : 0] | Function |
|---|---|
| 0...863 | HSync pulse ends after HSE[9 : 0] pixels after falling edge of HSync |

*Table xx. HSYNC End*

## POLARITY CONTROL (SUBADDRESS 37H)

### PXXX (D7-D0) POLARITY CONTROL BITS

The polarity of some output signals on the ADV7183 can be changed using the table as shown below.

| Bit | value | Function |
|---|---|---|
| PHS | 0 | HS active high |
| | 1 | HS active low |
| PHVR | 0 | HREF & VREF active high |
| | 1 | HREF & VREF active low |
| PVS | 0 | VS active high |
| | 1 | VS active low |
| PLLCREF | 0 | LLCREF active high |
| | 1 | LLCREF active low |
| PF | 0 | FIELD active high |
| | 1 | FIELD active low |
| PDV | 0 | DV active high |
| | 1 | DV active low |
| PFF | 0 | HFF,AEF & AFF active high |
| | 1 | HFF,AEF & AFF active low |
| PCLK | 0 | LLC1, LLC2 & QCLK active high |
| | 1 | LLC1, LLC2 & QCLK active low |

*Table xx. Polarity Control bits*

## APPENDIX 1

## BOARD DESIGN AND LAYOUT CONSIDERATIONS

The ADV7183 is a highly integrated circuit containing both precision analog and high speed digital circuitry. It has been designed to minimize interference effects on the integrity of the analog circuitry by the high speed digital circuitry. It is imperative that these same design and layout techniques be applied to the system level design such that high speed, accurate performance is achieved. The "Recommended Analog Circuit Layout" shows the analog interface between the device and monitor.

The layout should be optimized for lowest noise on the ADV71785 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VDD and GND pins should by minimized so as to minimize inductive ringing.

### Ground Planes

The ground plane should encompass all ADV7183 ground pins, voltage reference circuitry, power supply bypass circuitry for the ADV7183, the analog output/input traces, and all the digital signal traces leading up to the ADV7183. The ground plane is the board's common ground plane.

### Power Planes

The ADV7183 and any associated analog circuitry should have it's own power plane, referred to as the analog power plane (VDD). This power plane should be connected to the regular PCB power plane ($V_{CC}$) at a single point through a ferrite bead. This bead should be located within three inches of the ADV7183.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7183 power pins and voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

### Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. Best performance is obtained with 0.1 µF ceramic capacitor decoupling. Each group of VDD pins on the ADV71785 must have at least one 0.1 µF decoupling capacitor to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the ADV7183 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

### Digital Signal Interconnect

The digital inputs to the ADV7183 should be isolated as much as possible from the analog inputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV7183 should be avoided to reduce noise pickup.
Any active termination resistors for the digital inputs should be connected to the regular PCB power plane ($V_{CC}$), and not the analog power plane.

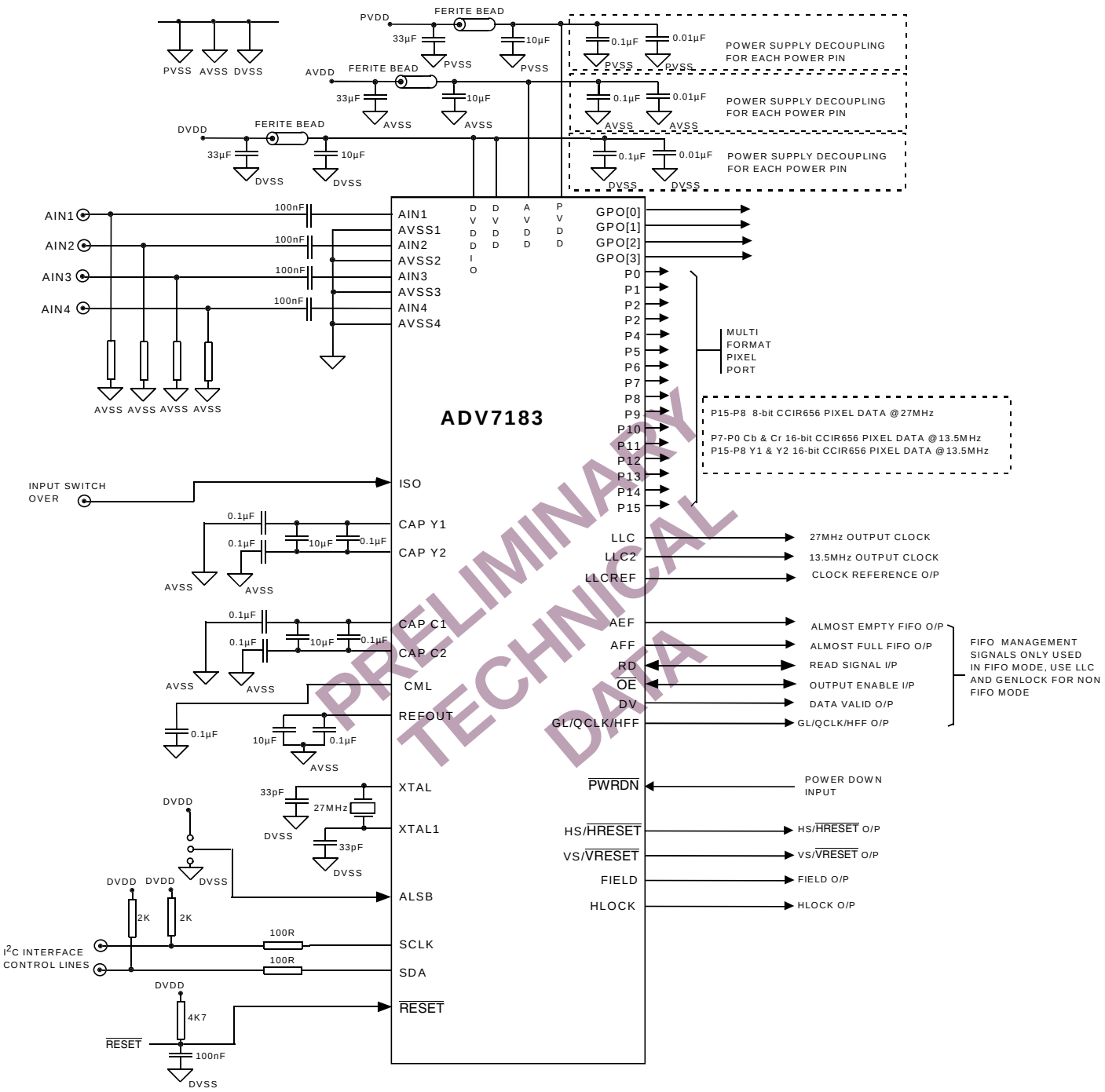
### Analog Signal Interconnect

The ADV7183 should be located as close as possible to the input connectors to minimize noise pickup and reflections due to impedance mismatch.

The video input signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

Digital Outputs, especially Pixel Data Inputs and clocking signals should never overlay any of the analog signal circuitry and should be kept as far away as possible.

The ADV7183 should have no inputs left floating. Any inputs that are not required should be tied to ground.



## OUTLINE DIMENSIONS

**Dimensions shown in inches and (mm).**

### 80-Lead LQFP
### (ST-80)