5-Bit Programmable 2-Phase Synchronous Buck Controller

Preliminary Technical Data — ADP3160

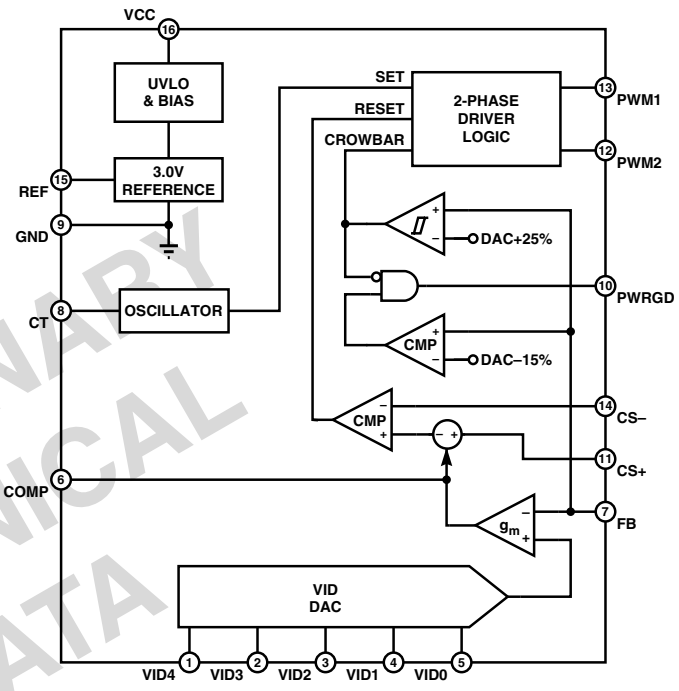
FEATURES

- ADOPT™ Optimal Positioning Technology for Superior Load Transient Response and Fewest Output Capacitors
- Complies with VRM 9.0 with Lowest System Cost
- Active Current Balancing Between Both Output Phases
- 5-Bit Digitally Programmable 1.1 V to 1.85 V Output
- Dual Logic-level PWM Outputs for Interface to External High-power Drivers
- Total Output Accuracy ±1% Over Temperature
- Current-Mode Operation
- Short Circuit Protection
- Power Good Output
- Overvoltage Protection Crowbar Protects Microprocessors with No Additional External Components

APPLICATIONS

Desktop PC Power Supplies for:
- High Performance Intel Processors
- AMD Athlon® Processors
- VRM Modules

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3160 is a highly efficient dual output synchronous buck switching regulator controller optimized for converting a 5 V or 12 V main supply into the core supply voltage required by high performance processors such as Pentium III and Athlon. The ADP3160 uses an internal 5-bit DAC to read a voltage identification (VID) code directly from the processor, which is used to set the output voltage between 1.1 V and 1.85 V. The ADP3160 uses a current mode PWM architecture to drive two logic-level outputs at a programmable switching frequency that can be optimized for VRM size and efficiency. The output signals are 180 degrees out of phase, allowing for the construction of two complementary buck switching stages. These two stages share the DC output current to reduce overall output voltage ripple. An active current balancing function ensures that both phases carry equal portions of the total load current, even under large transient loads, to minimize the size of the inductors.

The ADP3160 also uses a unique supplemental regulation technique called active voltage positioning to enhance load transient performance. Active voltage positioning results in a dc/dc converter that meets the stringent output voltage specifications for high performance processors, with the minimum number of output capacitors and smallest footprint. Unlike voltage-mode and standard current-mode architectures, active voltage positioning adjusts the output voltage as a function of the load current so that it is always optimally positioned for a system transient. The ADP3160 also provides accurate and reliable short circuit protection and adjustable current limiting.

The ADP3160 is specified over the commercial temperature range of 0°C to +70°C and is available in a 16-lead narrow body SOIC package.

REV. PrE 3/17/00

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ADP3160–SPECIFICATIONS[1] (VCC = 12 V, T_A = 0°C to +70°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
FEEDBACK INPUT						
Accuracy	V_{FB}					
1.1 V Output			1.089	1.1	1.111	V
1.5 V Output			1.460	1.475	1.490	V
1.85 V Output			1.831	1.85	1.869	V
Line Regulation	ΔV_{FB}	VCC = 10 V to 14 V		0.05		%
Input Bias Current	I_{FB}			5	50	nA
Crowbar Trip Point	$V_{CROWBAR}$	% of Nominal DAC Voltage	114	124	134	%
Crowbar Reset Point		% of Nominal DAC Voltage	50	60	70	%
Crowbar Response Time	$t_{CROWBAR}$	Overvoltage to PWM Going Low		300		ns
FB Low Comparator Threshold	$V_{FB(LOW)}$		375	425	500	mV
REFERENCE						
Output Voltage	V_{REF}	$0 \le I_{REF} \le 1$ mA	2.952	3.0	3.048	V
Output Current	I_{REF}		1	3		mA
VID INPUTS						
Input Low Voltage	$V_{IL(VID)}$				0.6	V
Input High Voltage	$V_{IH(VID)}$		2.0			V
Input Current	I_{VID}	VID(X) = 0 V		180	250	µA
Pull-up Resistance	R_{VID}		20	28		kΩ
Internal Pull-up Voltage			4.5	5.0	5.5	V
OSCILLATOR						
Maximum Frequency[2]	$f_{CT(MAX)}$		2000			kHz
Frequency Variation	Δf_{CT}	T_A = +25°C, CT = 91 pF	430	500	570	kHz
CT Charge Current	I_{CT}	T_A = +25°C, V_{FB} in Regulation	130	150	170	µA
		T_A = +25°C, V_{FB} = 0 V	26	36	46	µA
ERROR AMPLIFIER						
Output Resistance	$R_{O(ERR)}$			200		kΩ
Transconductance	$g_{m(ERR)}$		2.0	2.2	2.4	mmho
Output Current	$I_{O(ERR)}$	FB Forced to V_{OUT} - 3%		1		mA
Maximum Output Voltage	$V_{COMP(MAX)}$	FB Forced to V_{OUT} - 3%		3.0		V
Output Disable Threshold	$V_{COMP(OFF)}$		560	720	800	mV
-3 dB Bandwidth	BW_{ERR}	COMP = Open		500		kHz
CURRENT SENSE						
Threshold Voltage	$V_{CS(TH)}$	CS+ = VCC, FB Forced to V_{OUT} – 3%	142	157	172	mV
		FB ≤ 375 mV	75	95	115	mV
		0.8 V ≤ COMP ≤ 1 V		0	15	mV
Input Bias Current	I_{CS+}, I_{CS-}	CS+ = CS– = VCC		0.5	5	µA
Response Time	t_{CS}	CS+ – (CS–) ≥ 170 mV to PWM Going Low		50		ns
POWER GOOD COMPARATOR						
Undervoltage Threshold	$V_{PWRGD(UV)}$	Percent of Nominal Output	76	82	88	%
Overvoltage Threshold	$V_{PWRGD(OV)}$	Percent of Nominal Output	114	124	134	%
Output Voltage Low	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)}$ = 100 µA		30	200	mV
Response Time		FB Going High		2		µs
		FB Going Low		200		ns
PWM OUTPUTS						
Output Voltage Low	$V_{OL(PWM)}$	$I_{PWM(SINK)}$ = 400 µA		100	500	mV
Output Voltage High	$V_{OH(PWM)}$	$I_{PWM(SOURCE)}$ = 400 µA	4.0	5.0		V
Output Current	I_{PWM}		0.4	1		mA
Duty Cycle Limit[2]	DC	Per Phase, Relative to f_{CT}			50	%

NOTES
[1] All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.
[2] Guaranteed by design, not tested in production.
Specifications subject to changewithout notice.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SUPPLY						
DC Supply Current						
Normal Mode	I_{CC}			3.8	5.5	mA
No CPU Mode	$I_{CC(NO\ CPU)}$	VID4 - VID0 = Floating		3.8	5.5	mA
UVLO Mode	$I_{CC(UVLO)}$	VCC ≤ V_{UVLO}, VCC Rising		220	400	µA
UVLO Threshold Voltage	V_{UVLO}		5.9	6.4	6.9	V
UVLO Hysteresis			0.1	0.4	0.6	V

ABSOLUTE MAXIMUM RATINGS*

VCC ..... –0.3 V to 15 V
CS+, CS– ..... –0.3 V to VCC + 0.3 V
All Other Inputs & Outputs ..... –0.3 V to 10 V
Operating Ambient Temperature Range .... 0°C to +70°C
Operating Junction Temperature ..... +125°C
Storage Temperature Range ..... –65°C to +150°C
θ_{JA} ..... 125°C/W
Lead Temperature (Soldering, 10 sec) ..... +300°C
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

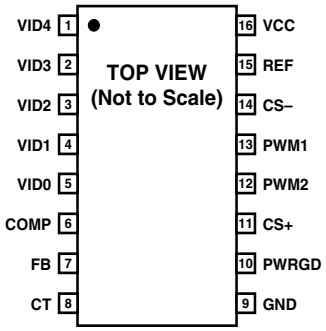
*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged. Unless otherwise specified, all voltages are referenced to GND

ORDERING GUIDE

Model	Temperature Range	Package
ADP3160JR	0°C to +70°C	R-16A (SO-16)*

* Narrow Body Small Outline Package

PIN CONFIGURATION
R-16A



PIN FUNCTION DESCRIPTIONS

Pin	Name	Function
1–5	VID4 – VID0	Voltage Identification DAC Inputs. These pins are pulled up to an internal reference, providing a logic one if left open. The DAC output programs the FB regulation voltage from 1.1 V to 1.85 V. Leaving all five DAC inputs open results in the ADP3160 going into a "No CPU" mode, shutting off its PWM outputs.
6	COMP	Error amplifier output and compensation point. The voltage at this output programs the output current control level between CS+ and CS–.
7	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage.
8	CT	External capacitor CT connection to ground sets the frequency of the device.
9	GND	Ground. All internal signals of the ADP3160 are referenced to this ground.
10	PWRGD	Open drain output that signals when the output voltage is in the proper operating range.
11	CS+	Current Sense Positive node. Positive input for the current comparator. The output current is sensed as a voltage at this pin with respect to CS–.
12	PWM2	Logic-level output for the phase 2 driver.
13	PWM1	Logic-level output for the phase 1 driver.
14	CS–	Current Sense Negative node. Negative input for the current comparator.
15	REF	3.0 V reference output.
16	VCC	Supply Voltage for the ADP3160.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

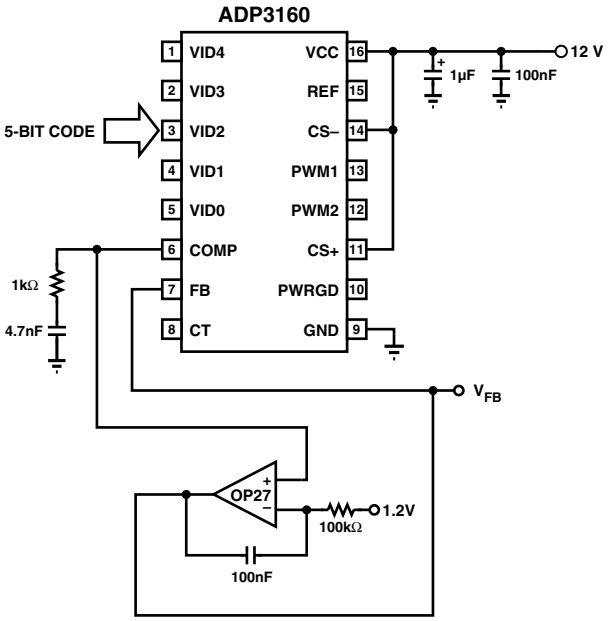


Figure 1. Closed-loop Output Voltage Accuracy Test Circuit

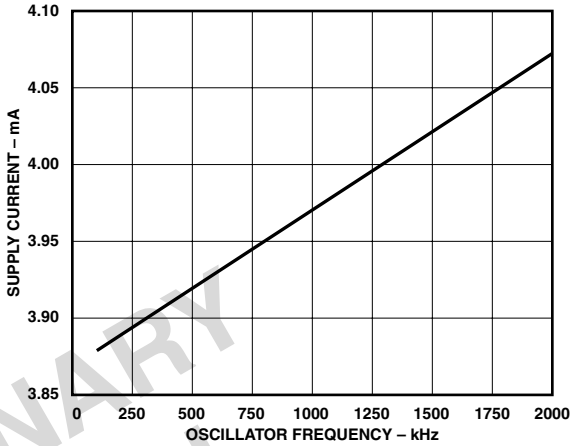


Figure 3. Supply Current vs. Oscillator Frequency

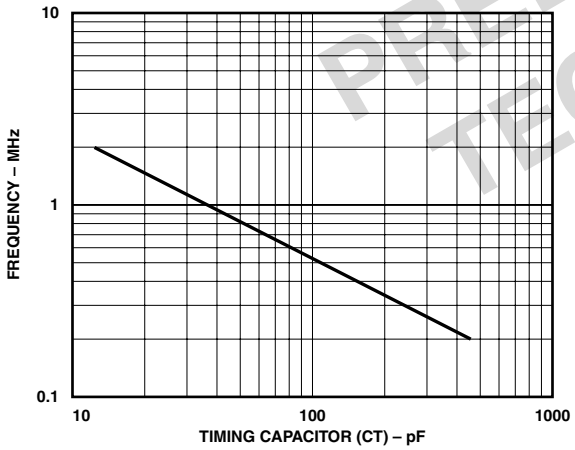


Figure 2. Frequency vs. Timing Capacitor

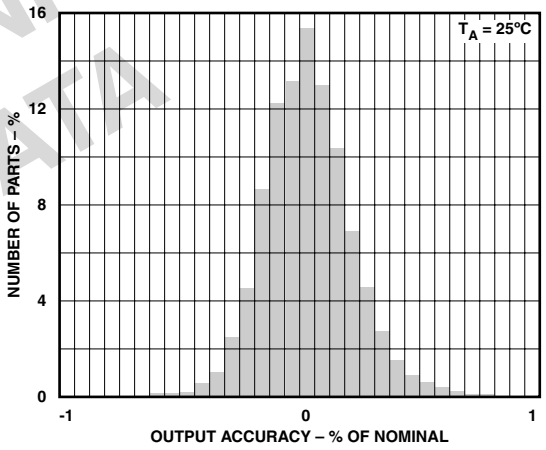


Figure 4. Output Accuracy Distribution, V_{OUT} = 1.6 V

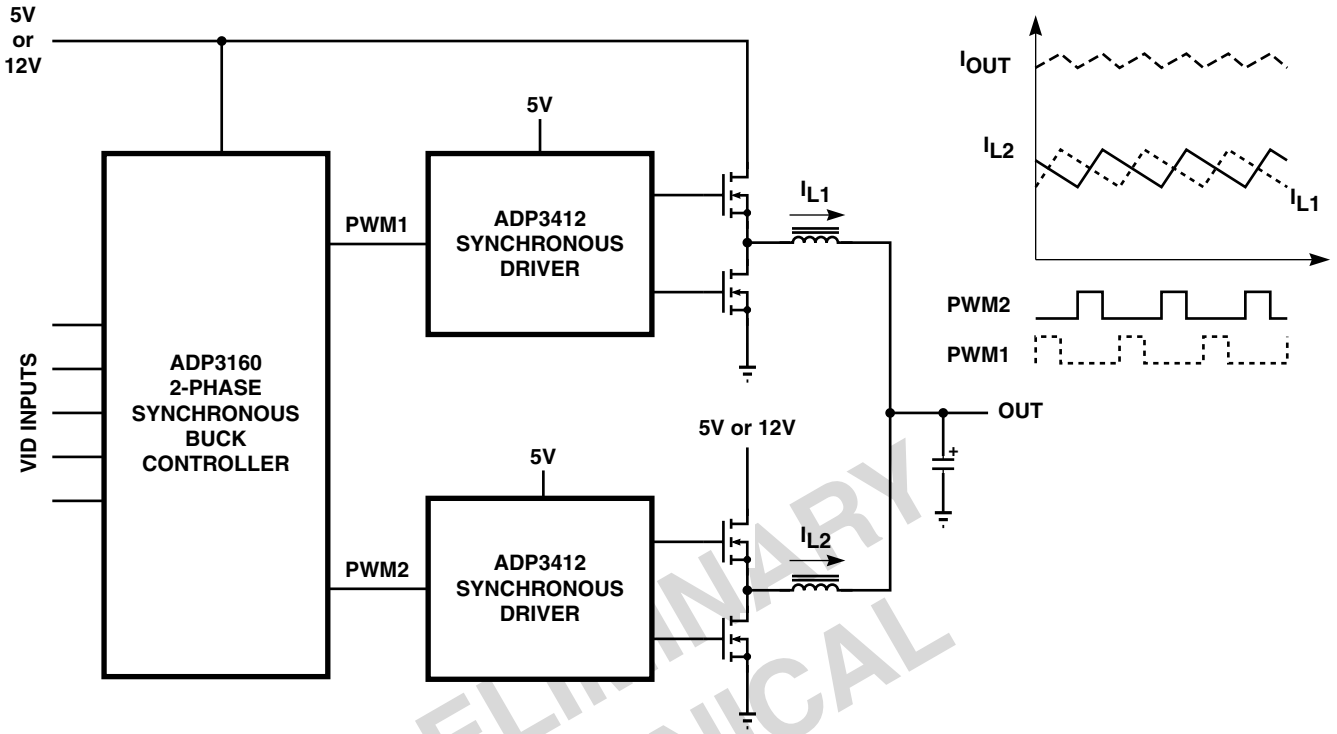


Figure 5. 2-Phase CPU Supply System Level Block Diagram.

THEORY OF OPERATION

The ADP3160 combines a current-mode, fixed frequency PWM controller with anti-phase logic outputs in a controller for a two-phase synchronous buck power converter. Two-phase operation is important for switching the high currents required by high performance microprocessors. Handling the high current in a single-phase converter would place difficult requirements on the power components such as inductor wire size, MOSFET ON-resistance and thermal dissipation. The ADP3160's high-side current sensing topology ensures that the load currents are balanced in each phase, such that neither phase has to carry more than half of the power. An additional benefit of high side current sensing over output current sensing is that the average current through the sense resistor is reduced by the duty cycle of the converter allowing the use of a lower power, lower cost resistor. The outputs of the ADP3160 are logic drivers only and are not intended to directly drive external power MOSFETs. Instead, the ADP3160 should be paired with drivers such as the ADP3412. A system level block diagram of a 2-phase power supply for high current CPUs is shown in Figure 5.

The frequency of the ADP3160 is set by an external capacitor connected to the CT pin. Each output phase of the ADP3160 operates at half of the frequency set by the CT pin. The error amplifier and current sense comparator control the duty cycle of the PWM outputs to maintain regulation. The maximum duty cycle per phase is inherently limited to 50% because the PWM outputs toggle in two-phase operation. While one phase is on, the other phase is off. In no case can both outputs be high at the same time.

Active Voltage Positioning

The output voltage is sensed at the FB pin allowing for remote sensing. To maintain the accuracy of the remote sensing, the GND pin should also be connected close to the load. A voltage error amplifier (gm) amplifies the difference between the output voltage and a programmable reference voltage. The reference voltage is programmed between 1.1V and 1.85V by an internal 5-bit DAC, which reads the code at the voltage identification (VID) pins. (Refer to Table 1 for the output voltage vs. VID pin code information.) The ADP3160 uses Analog Devices Optimal Positioning Technology (ADOPT™), a unique supplemental regulation technique that uses active voltage positioning and provides optimal compensation for load transients. When implemented, ADOPT adjusts the output voltage as a function of the load current, so that it is always optimally positioned for a load transient. Standard (passive) voltage positioning has poor dynamic performance, rendering it ineffective under the stringent repetitive transient conditions required by high performance processors. ADOPT, however, provides a bandwidth for transient response that is limited only by parasitic output inductance. This yields optimal load transient response with the minimum number of output capacitors.

Reference Output

A 3.0 V reference is available on the ADP3160. This reference is normally used to set the voltage positioning accurately using a resistor divider to the COMP pin. In addition, the reference can be used for other functions such as generating a regulated voltage with an external amplifier. The reference is bypassed with a 100 pF capacitor to ground. It is not intended to drive larger capacitive loads, and it should not be used to provide more than 1 mA of output current.

Cycle-by Cycle Operation

During normal operation (when the output voltage is regulated), the voltage-error amplifier and the current comparator are the main control elements. The free running oscillator ramps between 0 V and 3 V. When the voltage on the CT pin reaches 3 V, the oscillator sets the driver logic, which sets PWM1 high. During the ON time of phase 1, the driver IC turns on the high side MOSFET. The CS+ and CS– pins monitor the current through the sense resistor that feeds both high side MOSFETs. When the voltage between the two pins exceeds the threshold level, the driver logic is reset and the PWM output goes low. This signals the driver IC to turn off the high side MOSFET and turn on the low-side MOSFET. On the next cycle of the oscillator, the driver logic toggles and sets PWM2 high. The current is then steered through the second phase. On each following cycle of the oscillator, the outputs toggle between PWM1 and PWM2. In each case, the current comparator resets the PWM output low when the VT1 is reached. On both phases the current is sensed with the same resistor and the same comparator, so the current is inherently balanced. As the load current increases, the output voltage starts to decrease. This causes an increase in the output of the voltage error amplifier (g_m), which in turn leads to an increase in the current comparator threshold VT1, thus tracking the load current.

Active Current Sharing

The ADP3160 ensures current balance in the two phases by actively sensing the current through a single sense resistor. During one phase's ON time, the current through the respective high side MOSFET and inductor is measured through the sense resistor (R4 in Figure 6). When the comparator threshold is reached, the high side MOSFET turns off. On the next cycle the ADP3160 switches to the second phase. The current is measured with the same sense resistor and the same internal comparator, ensuring accurate matching. This scheme is immune to imbalances in the MOSFET's $R_{DS(ON)}$ and inductor parasitic resistance.

If for some reason one of the phases fails, the other phase will still be limited to its maximum output current (one half of the short circuit current limit). If this is not sufficient to supply the load, the output voltage will droop and cause the PWRGD output to signal that the output voltage has fallen out of its specified range.

Short Circuit Protection

The ADP3160 has multiple levels of short circuit protection to ensure fail-safe operation. The peak current limit is set by the sense resistor and the maximum current sense threshold voltage given in the specifications. To choose the sense resistor use the following formula:

$$I_{SC(PK)} = 2 \times \frac{172mV}{R_{SENSE}} \quad (1)$$

The factor of two is a result of the two phase operation. For example, an 86 A current limit is set with a 4 mΩ sense resistor. During current limit, each phase will carry 43 A.

When the load current exceeds the current limit, the output voltage is pulled low, and a second level of protection is enabled. When the output voltage is below 375 mV (given by the FB Low Comparator Threshold specification), the current limit threshold voltage is folded back to 95 mV. In the above example, this reduces the peak current limit from 86 A to 47.5 A (23.75 A per phase). Along with current fold back, the oscillator frequency is reduced by a factor of 5 when the output is 0 V. This further reduces the average current in short circuit.

Table 1. Output Voltage vs. VID Code

VID4	VID3	VID2	VID1	VID0	$V_{OUT(NOM)}$
1	1	1	1	1	No CPU
1	1	1	1	0	1.100 V
1	1	1	0	1	1.125 V
1	1	1	0	0	1.150 V
1	1	0	1	1	1.175 V
1	1	0	1	0	1.200 V
1	1	0	0	1	1.225 V
1	1	0	0	0	1.250 V
1	0	1	1	1	1.275 V
1	0	1	1	0	1.300 V
1	0	1	0	1	1.325 V
1	0	1	0	0	1.350 V
1	0	0	1	1	1.375 V
1	0	0	1	0	1.400 V
1	0	0	0	1	1.425 V
1	0	0	0	0	1.450 V
0	1	1	1	1	1.475 V
0	1	1	1	0	1.500 V
0	1	1	0	1	1.525 V
0	1	1	0	0	1.550 V
0	1	0	1	1	1.575 V
0	1	0	1	0	1.600 V
0	1	0	0	1	1.625 V
0	1	0	0	0	1.650 V
0	0	1	1	1	1.675 V
0	0	1	1	0	1.700 V
0	0	1	0	1	1.725 V
0	0	1	0	0	1.750 V
0	0	0	1	1	1.775 V
0	0	0	1	0	1.800 V
0	0	0	0	1	1.825 V
0	0	0	0	0	1.850 V

Power Good Monitoring

The Power Good comparator monitors the output voltage of the supply via the FB pin. The PWRGD pin is an open drain output whose high level (when connected to a pull-up resistor) indicates that the output voltage is within a range of 85% to 125% of the nominal output voltage requested by the VID DAC. PWRGD will go low if the output is outside this regulation band.

Output Crowbar

The ADP3160 includes a crowbar comparator that senses when the output voltage rises higher than 125% of nominal. This comparator overrides the control loop and sets both PWM outputs low. The driver ICs turn off the high side MOSFETs and turn on the low-side MOSFETs, thus pulling the output down as the reversed current builds up in the inductors. If the output overvoltage is due to a short of the high side MOSFET, this action will current limit the input supply or blow its fuse, protecting the microprocessor from destruction. The crowbar comparator releases when the output drops below 40% of nominal, and the controller returns to normal operation if the cause of the over voltage failure does not persist.

Output Disable

The ADP3160 includes an output disable function that turns off the control loop to bring the output voltage to 0 V. Because an extra pin is not available, the disable feature is accomplished by pulling the COMP pin to ground. When the COMP pin drops below 0.8 V, the oscillator stops and both PWM signals are driven low. This function does not place the part in low current shutdown and the reference voltage is still available. The COMP pin should be pulled down with an open collector or open drain type of output capable of sinking at least 1 mA

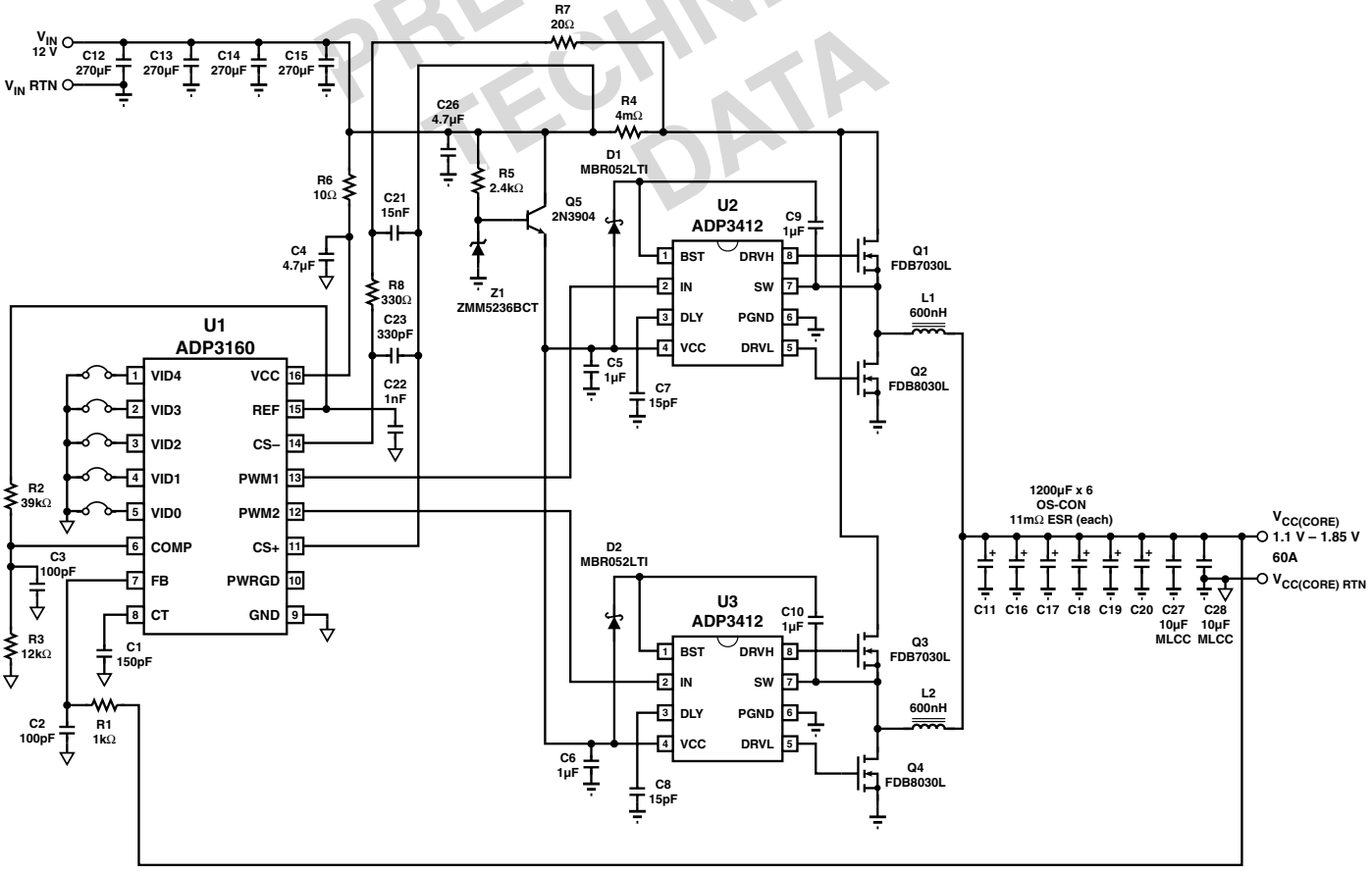


Figure 6. 60 A Intel CPU Supply Circuit.

APPLICATION INFORMATION

A VRM 9.0 Compliant Design Example

The design parameters for a typical high performance Intel CPU application (see Figure 6) are as follows:

Input voltage (V_{IN}) = 12 V
Nominal output voltage (V_{OUT}) = 1.6 V
Maximum output current ($I_{OUT(MAX)}$) = 60 A
Minimum output current ($I_{OUT(MIN)}$) = 1 A
Output voltage tolerance (ΔV_{OUT}) = 125 mV
Output current di/dt < 50 A/μs

C_T Selection for Operating Frequency

The ADP3160 uses a fixed frequency peak current control architecture. The switching frequency is determined by an external timing capacitor C_T. The value of C_T for a given switching frequency can be calculated by:

$$C_T = 0.9 \times \frac{150\mu A}{3V \times f_{OSC}} \qquad (2)$$

Assuming an operating frequency of 300 kHz, the timing capacitor value is 150 pF. The operating frequency is very stable over line and load, so the variation of f_{OSC} for a given device is highly dependent upon CT tolerance. For frequency stability, it is recommended to use an NPO-rated MLCC capacitor with 5% or better initial accuracy.

C_{OUT} Selection – Determining the ESR

The required ESR and capacitance drive the selection of the type and quantity of the output capacitors. The ESR must be small enough that both the resistive voltage deviation due to a step change in the load current and the output ripple voltage stay below the values defined in the specification of the microprocessor. The capacitance must be large enough that the output is held up while the inductor current ramps up or down to the value corresponding to the new load current.

The total tolerance of the processor is 125 mV. Taking into account a typical tolerance of ±0.5% (16 mV) set point accuracy of the ADP3160, and assuming a 0.5% (8 mV) peak-to-peak ripple, the allowed static voltage deviation of the output voltage when the load changes between the minimum and maximum values is 101 mV. Assuming a step change of $\Delta I = I_{O(MAX)} - I_{O(MIN)} = 59$ A, and allocating all of the total allowed static deviation to the contribution of the ESR sets the following limit:

$$R_{E(MAX)} = ESR_{MAX} = \frac{101mV}{59A} = 1.71m\Omega \qquad (3)$$

The output filter capacitor bank must have an ESR of less than 1.71 mΩ. One can use, for example, 6 SP-Type OS-CON capacitors from Sanyo, with 1200 μF capacitance, a 2.5 V voltage rating, and 11 mΩ ESR. The six capacitors have a maximum total ESR of 1.83 mΩ when connected in parallel. Another possibility is the ZA series from Rubycon. The trade-off is size versus cost. Twelve 1000 μF capacitors would give an ESR of 2 mΩ. These twelve capacitors take up more space, but are significantly less expensive than six OS-CON capacitors. To reach the 1.71 mΩ ESR limit, several MLCC capacitors in parallel with the bulk capacitance will bring the total ESR down to the required value. In the case of the OS-CONs, two 10 μF MLCC capacitors are enough to do the job.

Inductor Selection

The inductor design in this example is based on the assumption that the inductor ripple current is 30% of the maximum DC output current per phase with a nominal 12 V input. The inductor ripple current and inductor value are not critical, but do affect the trade-offs between cost, size, efficiency and volume. The higher the ripple current, the lower the inductor size and volume. Conversely, a higher inductor value means lower ripple current and smaller output capacitors, but results in slower transient response.

The design of the inductor should be based on 115% of the maximum output current (one half of the 30% ripple current allowance) at the nominal input voltage:

$$L > 3 \times \frac{(V_{IN(NOM)} - V_{OUT}) \times V_{OUT}}{V_{IN(NOM)} \times \frac{I_{OUT(MAX)}}{2} \times f} \qquad (4)$$

For a frequency of 300 kHz, each of the two phase-shifted outputs should have an inductor designed to carry half of the total maximum output current ($I_{O(MAX)}$):

$$L > 3 \times \frac{(12V - 1.6V) \times 1.6V}{12V \times \frac{60A}{2} \times 300kHz} = 462nH$$

A value of 600 nH at 30 A would be a good choice. The inductor should be able to handle 30 A of continuous current, and have a 30% to 50% saturation safety margin. Once the inductance is known, the next choice is to either design an inductor or find a standard inductor that comes as close a possible to meeting the overall design goals.

Designing an Inductor

The first decision in designing the inductor is to choose the core material. There are several possibilities for providing low core loss at high frequencies. Two examples are distributed gap powdered iron core (such as Kool-Mu) and soft ferrite cores (such as type 3F3, 3F4, or 4C4 from Philips Magnetics). Low frequency powdered iron cores should be avoided due to their high AC core loss, especially when the inductor value is relatively low and ripple current is high. Actual core loss is directly proportional to the applied input voltage and inversely proportional to the number of turns. The ripple current is a key factor for optimization of the converter design and determines the core losses to a large extent.

There are two main core types that can be used in this application. Open magnetic loop types, such as beads, beads on leads, rods and slugs provide the lowest cost but do not have a focused magnetic field in the core. The radiated EMI from the distributed magnetic field may create problems with noise interference in the circuitry surrounding the inductor. Closed loop types, such as pot cores, PQ, U and E cores or toroids cost more, but have much better EMI/RFI performance. A good compromise between price and performance are cores with a toroidal shape.

There are many useful references for quickly designing a power inductor. Table 2 gives some examples.

Selecting a Standard Inductor

The companies listed in Table 3 can provide design consultation and deliver power inductors optimized for high power applications upon request.

C_{OUT} Selection – Determining the Capacitance

In addition to the ESR requirements for transient response, the output capacitor bank has to be sized to properly filter the output ripple current.

The minimum capacitance required to handle the energy in the inductor, which is derived by determining what would be the output voltage deviation across a pure capacitance in the event of a full load step, can be calculated using:

$$C_{OUT(MIN)} = \frac{0.5 \times L \times I_{OUT(MAX)}^{2}}{V_{OUT} \times \Delta V} \quad (5)$$

$$C_{OUT(MIN)} = \frac{0.5 \times 600nH \times 60A^{2}}{1.6V \times 101mV} = 6700\mu F$$

where ΔV is the allowed static voltage deviation of the output.

The minimum capacitance required to properly filter the output ripple current can be calculated using:

$$C_{OUT(MIN)} = \frac{1}{\left(\frac{V_{RIPPLE}}{0.5 \times I_{RIPPLE}} - ESR\right) \times 2\pi \times f} \quad (6)$$

where I_{RIPPLE} is the inductor ripple current. A good rule of thumb is to limit the output ripple to 1% of the nominal output voltage. In this case, I_{RIPPLE} is 30% of $I_{OUT(MAX)}$ divided by 2, or 9 A.

For this example:

$$C_{OUT(MIN)} = \frac{1}{\left(\frac{16mV}{0.5 \times 9A} - 1.71m\Omega\right) \times 6.28 \times 300kHz} = 287\mu F$$

Equation 5 is only applicable when the ripple product caused by the ESR is less than the specified ripple voltage.

Normally, the transient model will give an adequate result for most applications. However, it is a good practice to calculate $C_{OUT(MIN)}$ values based on both the transient and ripple and use the larger of the two.

R_{SENSE}

The value of R_{SENSE} is based on the required output current. The current comparator of the ADP3160 has a threshold of 142 mV (minimum). Note that the 142 mV value cannot be used for the maximum specified nominal current, as headroom is needed for ripple current and transients.

The current comparator threshold sets the peak of the inductor current yielding a maximum output current, $I_{O(MAX)}$, which equals the peak value less half of the peak-to-peak ripple current. Solving for R_{SENSE}, allowing a 10% margin for overhead and using the minimum current sense threshold of 142 mV yields:

Table 2. Magnetics Design References

Magnetic Designer Software Intusoft (http://www.intusoft.com)
Designing Magnetic Components for High Frequency DC-DC Converters, McLyman, Kg Magnetics ISBN 1-883107-00-08

Table 3. Power Inductor Manufacturers

Coilcraft (847) 639-6400 http://www.coilcraft.com
Coiltronics (561) 241-7876 http://www.coiltronics.som
Sumida Electric Company (408) 982-9660 http://www.sumida.com

$$R_{SENSE} = \frac{V_{CS(TH)}}{1.1 \times \left(\frac{I_{OUT(MAX)}}{2} + \frac{I_{RIPPLE}}{2}\right)} \quad (7)$$

$$R_{SENSE} = \frac{142mV}{1.1 \times (30A + 4.5A)} = 3.7m\Omega$$

In this case, 4 mΩ was chosen as the closest standard value.

Once R_{SENSE} has been chosen, the peak maximum short-circuit current ($I_{SC(PK)}$) can be predicted using:

$$I_{SC(PK)} = \frac{V_{CS(TH)}}{R_{SENSE}} \quad (8)$$

$$I_{SC(PK)} = \frac{172mV}{4m\Omega} = 43A \text{ (per phase)}$$

The actual short-circuit current is less than the calculated $I_{SC(PK)}$ value because the frequency rapidly decreases when the output voltage drops below 0.5 V. To safely carry the short-circuit current, the sense resistor must have a power rating of at least:

$$P_{R_{SENSE}} = I_{SC(PK)}^{2} \times \left(\frac{V_{OUT}}{V_{IN}} \times R_{SENSE}\right) \quad (9)$$

$$P_{R_{SENSE}} = 43A^{2} \times \left(\frac{1.6V}{12V} \times 4m\Omega\right) = 986mW$$

Power MOSFETs

Two external N-channel power MOSFETs must be selected for use with the ADP3160 and ADP3412, one for the main switch, and one for the synchronous switch. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$ and $R_{DS(ON)}$.

The minimum input voltage dictates whether standard threshold or logic-level threshold MOSFETs must be used. For V_{IN} > 8 V, standard threshold MOSFETs ($V_{GS(TH)}$ < 4 V) may be used. If V_{IN} is expected to drop below 8 V, logic-level threshold MOSFETs ($V_{GS(TH)}$ < 2.5 V) are strongly recommended.

The maximum output current $I_{O(MAX)}$ determines the $R_{DS(ON)}$ requirement for the power MOSFETs. When the ADP3160 is operating in continuous mode, the simplifying assumption can be made that one of the two MOSFETs is always conducting the average load current. For V_{IN} = 12 V and V_{OUT} = 1.6 V, the maximum duty ratio of the high side MOSFET is:

$$D_{HSF(MAX)} = \frac{V_{OUT}}{V_{IN}} = 13.3\% \quad (10)$$

The maximum duty ratio of the low-side (synchronous rectifier) MOSFET is:

$$D_{LSF(MAX)} = 1 - D_{HSF(MAX)} = 86.7\% \quad (11)$$

The maximum rms current of the high-side MOSFET is:

$$I_{HSF(RMS)} = \sqrt{D_{HSF(MAX)} \times \frac{\left(\frac{I_{L(VALLEY)}^2}{2} + \frac{I_{L(VALLEY)} \times I_{(PEAK)}}{4} + \frac{I_{L(PEAK)}^2}{2}\right)}{3}} \quad (12)$$

For this example, $I_{L(VALLEY)}$ is 85% of $I_{OUT(MAX)}$ or 51A, $I_{L(PEAK)}$ is 115% of $I_{OUT(MAX)}$ or 69 A, and the high-side MOSFET rms current is 14.2 A. The maximum rms current of the low-side MOSFET is:

$$I_{LSF(RMS)} = \sqrt{D_{LSF(MAX)} \times \frac{\left(\frac{I_{L(VALLEY)}^2}{2} + \frac{I_{L(VALLEY)} \times I_{(PEAK)}}{4} + \frac{I_{L(PEAK)}^2}{2}\right)}{3}} \quad (13)$$

Using the same conditions as Equation 10 gives a low-side MOSFET rms current of 36.3 A. The $R_{DS(ON)}$ for each MOSFET can be derived from the allowable dissipation. If 10% of the maximum output power is allowed for MOSFET dissipation, the total dissipation will be:

$$P_{MOSFET} = 0.1 \times V_{OUT} \times I_{OUT(MAX)} \quad (14)$$

$$P_{MOSFET} = 0.1 \times 1.6V \times 60A = 9.6W$$

Allocating half of the total dissipation for the high-side MOSFET and half for the low-side MOSFET, the required minimum MOSFET resistances will be:

$$HSR_{DS(ON)(MIN)} = \frac{4.8W}{14.2A^2} = 24m\Omega \quad (15)$$

$$LSR_{DS(ON)(MIN)} = \frac{4.8W}{36.3A^2} = 3.6m\Omega \quad (16)$$

Note that there is a trade-off between converter efficiency and cost. Larger MOSFETs reduce the conduction losses and allow higher efficiency, but increase the system cost. If efficiency is not a major concern, a Fairchild FDB6035AL for the high side and a Fairchild FDB8030L for the low side is a good choice.

The high-side MOSFET dissipation is:

$$P_{HSF} = I_{HS(RMS)}^2 \times HSR_{DS(ON)} + \frac{0.5 \times V_{IN} \times I_{L(PEAK)} \times Q_G \times f}{I_G} \quad (17)$$

where the second term represents the turn-off loss of the MOSFET. (In the second term, Q_G is the gate charge to be removed from the gate for turn-off and IG is the gate current. From the data sheet, Q_G is a 23 nC and the peak gate drive current provided by the ADP3412 is about 1 A). For this example, P_{HSF} is approximately 4.7 W.

The low-side MOSFET dissipation is:

$$P_{LSF} = I_{LS(RMS)}^2 \times LSR_{DS(ON)} = 5.9W \quad (18)$$

(Note that there are no switching losses in the low-side MOSFET.)

C_{IN} Selection and Input Current di/dt Reduction

In continuous inductor-current mode, the source current of the high-side MOSFET is approximately a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} = \sqrt{V_{OUT} \times (V_{IN} - V_{OUT})} \times \frac{I_{OUT}}{V_{IN}} \quad (19)$$

In this example, the current is separated into to equal paths, so the RMS current is:

$$I_{RMS} = 0.5 \times \sqrt{1.6V \times (12V - 1.6V)} \times \frac{60A}{12V} = 10.2A$$

Note that the capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be placed in parallel to meet size or height requirements in the design. If this example, the input capacitor bank is formed by four 270 µF, 16 V OS-CON capacitors.

The ripple voltage across the paralleled capacitors is:

$$V_{C_{IN(RIPPLE)}} = \left(\frac{ESR_{IN}}{4} + \frac{D_{HSF(MAX)}}{4 \times C_{IN} \times f}\right) \times \frac{I_{OUT(MAX)}}{2} \quad (20)$$

$$V_{C_{IN(RIPPLE)}} = \left(\frac{ESR_{IN}}{4} + \frac{13.3\%}{4 \times 1080\mu F \times 300kHz}\right) \times \frac{60A}{2} = 93mV_{P-P}$$

To further reduce the effect of the ripple voltage on the system supply voltage bus and to reduce the input-current di/dt to below the recommended maximum of 0.1 A/ms, an additional small inductor (L > 1 µH @ 15 A) should be inserted between the converter and the supply bus.

Feedback Loop Compensation Design for ADOPT

Optimized compensation of the ADP3160 allows the best possible containment of the peak-to-peak output voltage deviation. Any practical switching power converter is inherently limited by the inductor in its output current slew rate to a value much less than the slew rate of the load. Therefore, any sudden change of load current will initially flow through the output capacitors, and this will produce an output voltage deviation equal to the ESR of the output capacitor array times the load current change.

If the time constant of the output capacitors (ESR x C) is greater than the switching period programmed by CT, as tends to be true of aluminum and even organic electrolytic capacitors, the ADOPT design technique will allow the lowest number of capacitors to be used for a given peak-to-peak containment of output voltage deviation caused by fast dynamic load swings. For design purposes, the assumption is made that capacitors of this category will be chosen.

The optimal implementation of voltage positioning, ADOPT, will create an output impedance of the power converter that is entirely resistive over the widest possible frequency range - including DC - and equal to the maximum acceptable ESR of the output capacitor array. This can be achieved by having a single pole roll-off of the voltage gain of the g_m error amplifier, where the pole frequency coincides with the ESR zero of the output capacitor. A gain with single pole roll-off requires that the g_m amplifier output pin be terminated by the parallel combination of resistance and capacitance.

The first step is to determine the targeted output resistance, $R_{E(MAX)}$ of the power converter using equation 2. Then the compensation can be tailored to create that impedance for the power converter, and the quantity of output capacitors can be chosen to create a net ESR that is less than or equal to $R_{E(MAX)}$.

The next step in the ADOPT design procedure is to determine the termination resistance of the g_m amplifier that will yield the correct output resistance:

$$R_T = \frac{n_I \times R_{SENSE}}{g_m \times R_{E(MAX)}} \quad (21)$$

for this example:

$$R_T = \frac{12.5 \times 4m\Omega}{2.0mmho \times 1.71m\Omega} = 14.6k\Omega$$

where n_I is the division ratio from the g_m output voltage signal to the PWM comparator. For the ADP3160, n_I = 12.5. To ensure that the output voltage plus ripple is not positioned beyond the static regulation limits, use the maximum R_{CS} and minimum g_m values.

Next, the bottom resistor (i.e., the resistor from COMP to GND) is calculated:

$$R_B = \frac{V_{REF}}{\frac{V_{REF} - V_{GNL}}{R_T} + \frac{V_{REF} - \frac{V_{CC}}{2}}{R_{O(ERR)}} + (g_m \times V_{OS})} \quad (22)$$

where V_{REF} is the 3 V supply voltage to which the upper compensation resistor is connected, V_{GNL} is the output voltage of the g_m amplifier that commands zero current, given by:

$$V_{GNL} = 1V + \frac{g_m \times R_T \times R_{SENSE} \times I_{RIPPLE}}{n_I} \quad (23)$$

$$V_{GNL} = 1V + \frac{2.0mmho \times 14.6k\Omega \times 4m\Omega \times 9A}{12.5} = 1.084V$$

$R_{O(ERR)}$ is the specified output resistance of the g_m amplifier, and V_{OS} is the desired DC output voltage offset (from the nominal value) at no load, given by:

$$V_{OS} = \frac{I_{RIPPLE} \times R_{E(MAX)}}{2} - \frac{\Delta V_{OUT} - \Delta V}{2} \quad (24)$$

$$V_{OS} = \frac{9A \times 1.71m\Omega}{2} - \frac{125mV - 101mV}{2} = 19.7mV$$

where $R_{E(MAX)}$ is the series resistance of all the bulk output capacitors in parallel. The subtracted terms in the V_{OS} equation are to provide design margin for ripple and error.

Using these results to solve equation 21 yields:

$$R_B = \frac{3V}{\frac{3V - 1.084V}{14.6k\Omega} + \frac{3V - 6V}{200k\Omega} + (2.0mmho \times -19.7mV)} = 18.8k\Omega$$

The upper compensation resistor (connected from COMP to REF) can now be calculated using:

$$R_U = \frac{1}{\frac{1}{R_T} - \frac{1}{R_{O(ERR)}} - \frac{1}{R_B}} \quad (25)$$

$$R_U = \frac{1}{\frac{1}{14.6k\Omega} - \frac{1}{200k\Omega} - \frac{1}{18.8k\Omega}} = 97.1k\Omega$$

Finally, the capacitor that optimally compensates the power converter's response is calculated:

$$C_{OC} = \frac{C_{OUT} \times R_{E(MAX)}}{R_T} \quad (26)$$

$$C_{OC} = \frac{7200\mu F \times 1.71m\Omega}{14.6k\Omega} = 840pF$$

where C_{OUT} and R_E are the capacitance and ESR of the output capacitor bank. Two characteristics of the switching voltage regulator suggest that emperical optimization of C_{OC} may be needed: the non-linearity of a switching power supply and the dynamic increase of inductance when switching from high to low currents. Both of these characteristics may tend to required a lower value of C_{OC} than calculated if the output capacitance is near the minimum allowed value.

Trade-Offs Between DC Load Regulation and AC Load Regulation

Casual observation of the circuit operation — e.g., with a voltmeter — would make it appear that the DC load regulation appears to be rather poor compared to a conventional regulator. This would be especially noticeable under very light or very heavy loads where the voltage is "positioned" near one of the extremes of the regulation window rather than near the nominal center value. It must be noted and understood that this low gain characteristic (i.e., loose DC load regulation) is inherently required to allow improved transient containment (i.e., to achieve tighter AC load regulation). That is, the DC load regulation is intentionally sacrificed (but kept within specification) in order to minimize the number of capacitors required to contain the load transients produced by the CPU.

Figure 7 shows an oscilloscope photo of the circuit of Figure 6 being subjected to a 1 A to 55 A transient at a slew rate of 50 A/µs.

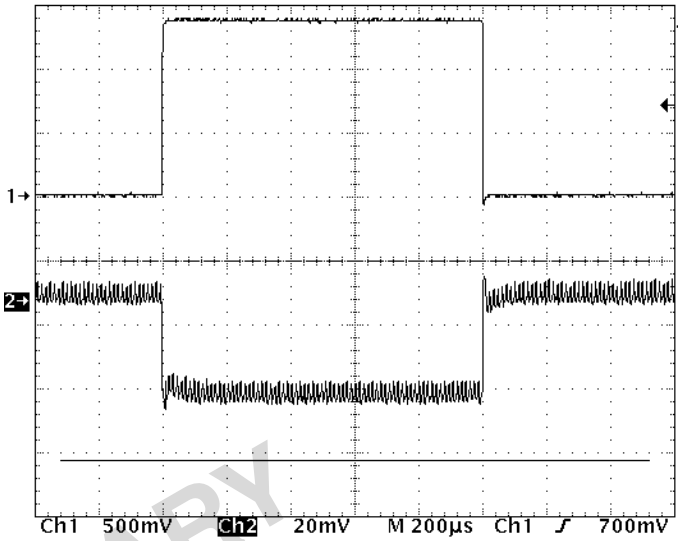


Figure 7. Transient Response of the 60A Design Example of Figure 6.

An AMD Athlon VRM Design Example

The design parameters for a typical AMD Athlon application (see Figure 8) are as follows:

Input voltage (V_{IN}) = 5 V
Nominal output voltage (V_{OUT}) = 1.6 V
Maximum output current ($I_{OUT(MAX)}$) = 35 A
Minimum output current ($I_{OUT(MIN)}$) = 3 A
Output voltage tolerance (ΔV_{OUT}) = +100 mV / -50 mV
Output current di/dt < 30 A/µs

The only changes from the previous design example stem from the changes in input voltage, output current, and the output voltage tolerance.

Unlike the previous example, this circuit does not derive its power from the 12 V supply, but converts the 5 V supply down to the 1.6 V required by the Athlon processor. The change in input voltage and output current allows for the use of higher $R_{DS(ON)}$ MOSFETs and fewer output capacitors. The input capacitor bank has also been optimized for the lower input voltage.

LAYOUT AND COMPONENT PLACEMENT GUIDELINES

The following guidelines are recommended for optimal performance of a switching regulator in a PC system:

General Recommendations

1. For best results, a four-layer (minimum) PCB is recommended. This should allow the needed versatility for control circuitry interconnections with optimal placement, a signal ground plane, power planes for both power ground and the input power (e.g., 5 V), and wide interconnection traces in the rest of the power delivery current paths. Each square unit of 1 ounce copper trace has a resistance of ~ 0.53 mΩ at room temperature.
2. Whenever high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.
3. The power and ground planes should overlap each other as little as possible. It is generally easiest (although not necessary) to have the power and signal ground planes on the same PCB layer. The planes should be connected nearest to the first input capacitor where the input ground current flows from the converter back to the power source (e.g., 5 V).
4. If critical signal lines (including the voltage and current sense lines of the ADP3160) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.
5. The power ground plane should not extend under signal components, including the ADP3160 itself. If necessary, follow the preceding guideline to use the signal plane as a shield between the power ground plane and the signal circuitry.
6. The GND pin of the ADP3160 should connect first to the timing capacitor (on the CT pin), and then into the signal ground plane. In cases where no signal ground plane can be used, short interconnections to other signal ground circuitry in the power converter should be used — the compensation capacitor being the next most critical.
7. The output capacitors of the power converter should be connected to the signal ground plane even though power current flows in the ground of these capacitors. For this reason, it is advised to avoid critical ground connections (e.g., the signal circuitry of the power converter) in the signal ground plane between the input and output capacitors. It is also advised to keep

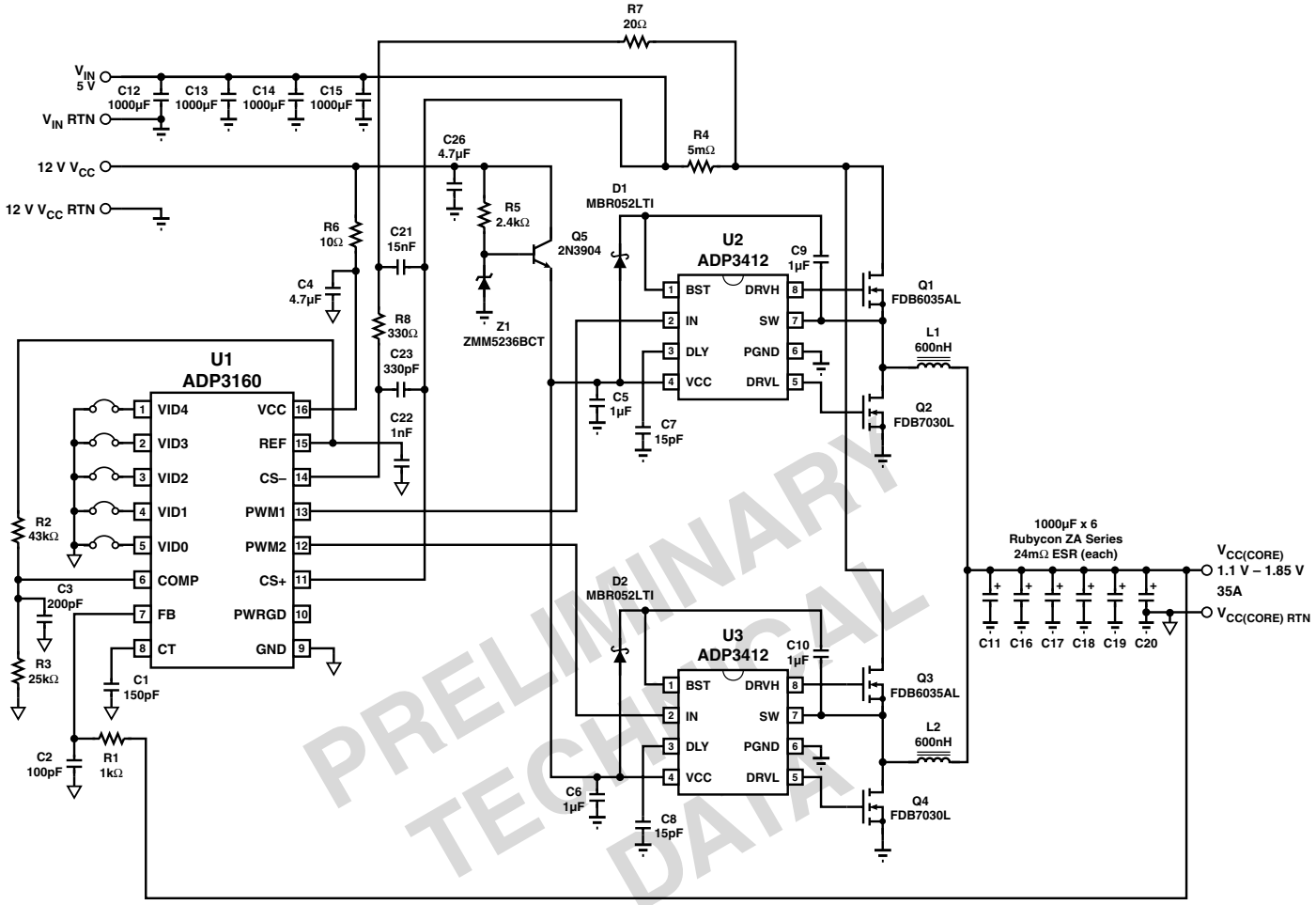


Figure 8. 35 A Athlon CPU Supply Circuit.

the planar interconnection path short (i.e., have input and output capacitors close together).

8. The output capacitors should also be connected as closely as possible to the load (or connector) that receives the power (e.g., a microprocessor core). If the load is distributed, the capacitors also should be distributed, and generally in proportion to where the load tends to be more dynamic.

9. Absolutely avoid crossing any signal lines over the switching power path loop, described below.

Power Circuitry

10. The switching power path should be routed on the PCB to encompass the smallest possible area in order to minimize radiated switching noise energy (i.e., EMI). Failure to take proper precaution often results in EMI problems for the entire PC system as well as noise related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors, the two MOSFETs, and the power Schottky diode if used, including all interconnecting PCB traces and planes. The use of short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high-energy ringing, and it accommodates the high current demand with minimal voltage loss.

11. An optional power Schottky diode (3-5 A dc rating) placed from each lower MOSFET's source (anode) to drain (cathode) will help to minimize switching power dissipation in the upper MOSFETs. In the absence of an effective Schottky diode, this dissipation occurs through the following sequence of switching events. The lower MOSFET turns off in advance of the upper MOSFET turning on (necessary to prevent cross-conduction). The circulating current in the power converter, no longer finding a path for current through the channel of the lower MOSFET, draws current through the inherent body-drain diode of the MOSFET. The upper MOSFET turns on, and the reverse recovery characteristic of the lower MOSFET's body-drain diode prevents the drain voltage from being pulled high quickly. The upper

MOSFET then conducts very large current while it momentarily has a high voltage forced across it, which translates into added power dissipation in the upper MOSFET. The Schottky diode minimizes this problem by carrying a majority of the circulating current when the lower MOSFET is turned off, and by virtue of its essentially nonexistent reverse recovery time.

12. A small ferrite bead inductor placed in series with the drain of the lower MOSFET can also help to reduce this previously described source of switching power loss.
13. Whenever a power dissipating component (e.g., a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are: improved current rating through the vias (if it is a current path), and improved thermal performance — especially if the vias extended to the opposite side of the PCB where a plane can more readily transfer the heat to the air.
14. The output power path, though not as critical as the switching power path, should also be routed to encompass a small area. The output power path is formed by the current path through the inductor, the current sensing resistor, the output capacitors, and back to the input capacitors.
15. For best EMI containment, the power ground plane should extend fully under all the power components except the output capacitors. These are: the input capacitors, the power MOSFETs and Schottky diode, the inductor, the current sense resistor and any snubbing elements that might be added to dampen ringing. Avoid extending the power ground under any other circuitry or signal lines, including the voltage and current sense lines.

Signal Circuitry

16. The output voltage is sensed and regulated between the FB pin and the GND pin (which connects to the signal ground plane). The output current is sensed (as a voltage) and regulated between the CS+ pin and the CS– pin. In order to avoid differential mode noise pickup in those sensed signals, their loop areas should be small. Thus the FB trace should be routed atop the signal ground plane, and the CS+ and CS– traces should be routed as a closely coupled pair (CS+ should be over the signal ground plane as well).
17. The CS+ and CS– traces should be Kelvin connected to the current sense resistor so that the additional voltage drop due to current flow on the PCB at the current sense resistor connections does not affect the sensed voltage.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead SOIC
R-16A/SO-16