

FEATURES

- Two Independent Controllers on One Chip
- 1.515 V and 1.818 V Outputs
- Shutdown Inputs to Control Each Channel
- Compatible with PC Motherboard TYPEDET Signal
- ±2.5% Accuracy Over, Line, Load, and Temperature
- Low Quiescent Current
- Low Shutdown Current
- Works with External N-Channel MOSFETs for Low Cost
- "Hiccup Mode" Fault Protection
- No External Voltage or Current Setting Resistors
- Small, 8-Lead SOIC Package

APPLICATIONS

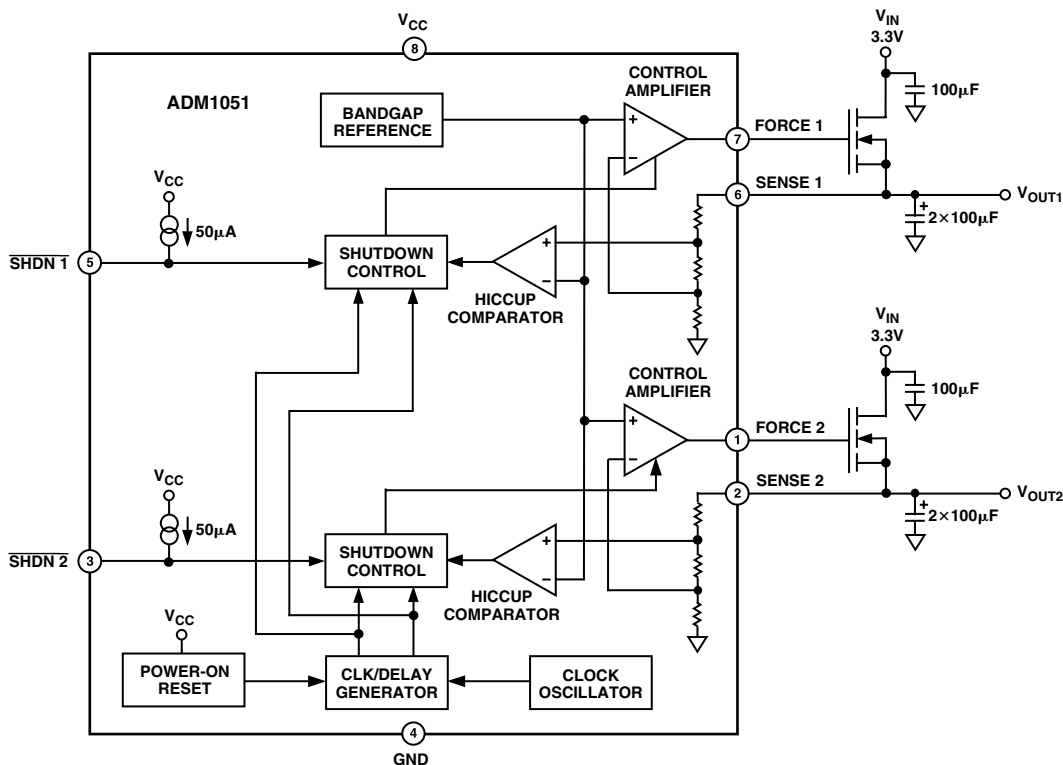
- Desktop Computers
- Servers
- Workstations

GENERAL DESCRIPTION

The ADM1051 is a dual, precision, voltage regulator controller intended for power rail generation and active bus termination on personal computer motherboards. It contains a precision 1.2 V bandgap reference and two channels consisting of control amplifiers driving external power devices. Each channel has a shutdown input to turn off amplifier output and Hiccup Mode protection circuitry for the external power device. The shutdown input on the 1.5 V channel can also be used with the TYPEDET signal on a PC motherboard to select the output voltage.

The ADM1051 operates from a 12 V supply. This gives sufficient headroom for the amplifiers to drive external N-channel MOSFETs, operating as source-followers, as the external series pass devices. This has the advantage that N-channel devices are cheaper than P-channel devices of similar performance, and the circuit is easier to stabilize than one using P-channel devices in a common-source configuration.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

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ADM1051—SPECIFICATIONS ($V_{CC} = 12\text{ V} \pm 6\%$, $V_{IN} = 3.3\text{ V}$, $T_A = 0^\circ\text{C}$ to 70°C , both channels, unless otherwise noted. See Test Circuit.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT VOLTAGE					
Channel 1		1.515		V	$\overline{\text{SHDN 1}}$ Floating
Channel 2		1.818		V	
OUTPUT VOLTAGE ACCURACY					
Load Regulation	-2.5		+2.5	%	$V_{IN} = 3.0\text{ V}$ to 3.6 V , $I_{OUT} = 10\text{ mA}$ to 1 A
Line Regulation	-5		+5	mV	$V_{IN} = 3.3\text{ V}$, $I_{OUT} = 10\text{ mA}$ to 1 A ¹
	-5		+5	mV	$V_{IN} = 3.0\text{ V}$ to 3.6 V , $I_{OUT} = 1\text{ A}$ ¹
CONTROL AMPLIFIER					
Control Amplifier Open-Loop Gain		100		dB	$I_O = 10\text{ mA}$ to 2 A To 90% of Force High Output Level ($C_L = 470\text{ pF}$)
Control Amplifier Slew Rate		3		V/ μs	
Closed-Loop Settling Time		5		μs	
Turn-On Time			5	μs	
Sense Input Impedance ¹		50		k Ω	
Force Output Voltage Swing, V_F (High)		10		V	
Force Output Voltage Swing, V_F (Low)		2		V	$R_L = 10\text{ k}\Omega$ to GND $R_L = 10\text{ k}\Omega$ to V_{CC}
HICCUP MODE					
Hiccup Mode Hold-Off Time	30	60	90	ms	Figure 16
Hiccup Mode Threshold			$0.8 \times V_{OUT}$	V	
Hiccup Comparator Glitch Immunity		100		μs	
Hiccup Mode On-Time	0.5	1.0	1.5	ms	
Hiccup Mode Off-Time	20	40	60	ms	
Power-On Reset Threshold	6		9	V	
SHUTDOWN, $\overline{\text{SHDN 1}}$					
Mode 1 (Shutdown)			0.8	V	
Mode 2 (1.5 V Out)	2		3.9	V	
Mode 3 (3.3 V Out)	4.3		5.3	V	
Mode 4 (1.5 V Out)	6.2		12	V	
SHUTDOWN, $\overline{\text{SHDN 2}}$					
Shutdown Input Low Voltage, V_{IL}			0.8	V	Shutdown Inputs Floating Both Channels Shut Down
Shutdown Input High Voltage, V_{IH}	2.0			V	
Supply Current, Normal Operation		2.4	4.0	mA	
Supply Current, Shutdown Mode		600	1000	μA	

NOTES

¹Guaranteed by design.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

($T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{CC} to GND	14 V
SHDN 1, SHDN 2 to GND	-0.3 V to ($V_{CC} + 0.3$ V)
SENSE 1, SENSE 2 to GND	-0.3 V to +5.5 V
FORCE 1, FORCE 2	Short-Circuit to GND or V_{CC}
Continuous Power Dissipation ($T_A = 70^\circ\text{C}$)	650 mW
8-Lead SOIC (Derate 8.3 mW/ $^\circ\text{C}$ above 70°C)	
Operating Temperature Range	
Commercial (J Version)	0°C to 70°C
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	300°C

*This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

THERMAL CHARACTERISTICS

8-Lead Small Outline Package:

$$\theta_{JA} = 150^\circ\text{C}/\text{W}$$

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM1051JR	0°C to 70°C	8-Lead SOIC	R-8

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	FORCE 2	Output of Channel 2 control amplifier to gate of external N-channel MOSFET.
2	SENSE 2	Input from source of external MOSFET to inverting input of Channel 2 control amplifier, via output voltage-setting feedback resistor network.
3	$\overline{\text{SHDN 2}}$	Digital Input. Active-low shutdown control with $50\ \mu\text{A}$ internal pull-up. The output of Channel 2 control amplifier goes to ground when $\overline{\text{SHDN 2}}$ is taken low.
4	GND	Device Ground Pin.
5	$\overline{\text{SHDN 1}}$	Digital Input. Active-low shutdown control with $50\ \mu\text{A}$ internal pull-up. See text for more details of $\overline{\text{SHDN 1}}$ functionality.
6	SENSE 1	Input from source of external MOSFET to inverting input of Channel 1 control amplifier, via output voltage-setting feedback resistor network.
7	FORCE 1	Output of Channel 1 control amplifier to gate of external N-channel MOSFET.
8	V_{CC}	12 V Supply.

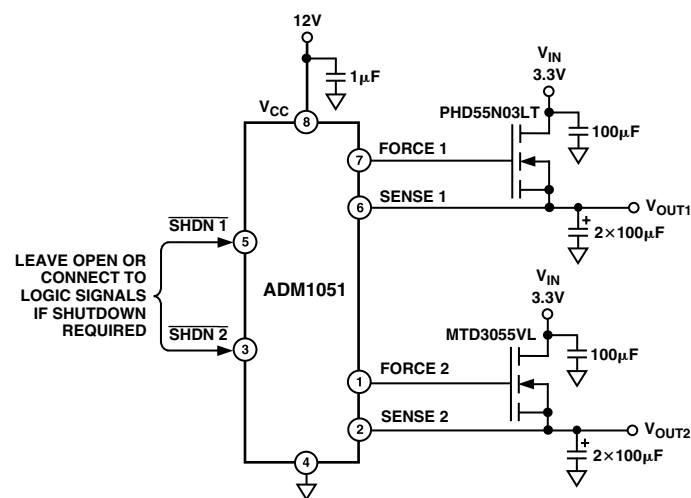
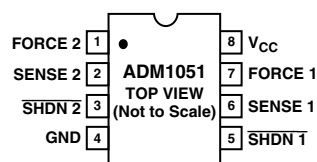


Figure 1. Test Circuit

PIN CONFIGURATION



ADM1051–Typical Performance Characteristics

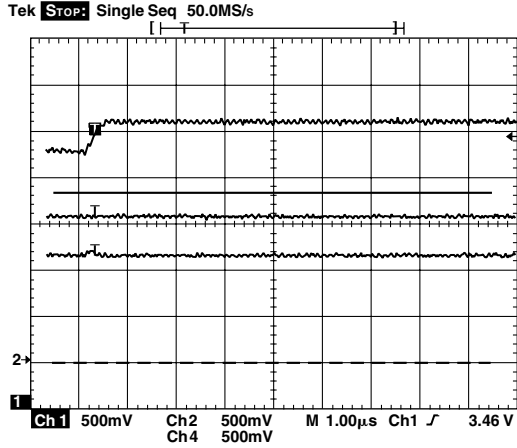


Figure 2. Line Transient Response, Channel 1 and Channel 2

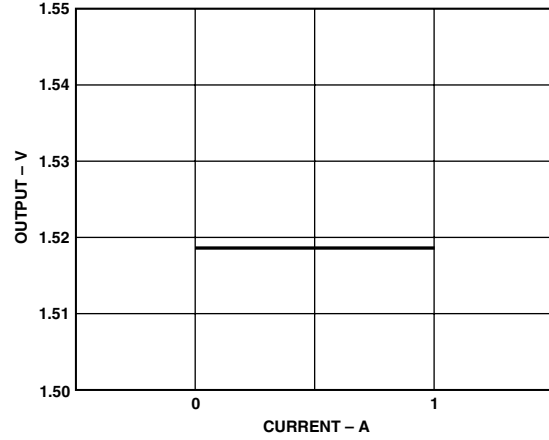


Figure 5. Load Regulation, Channel 1

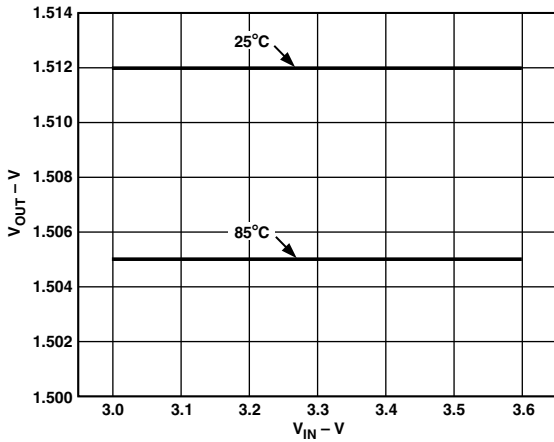


Figure 3. Line Regulation, Channel 1

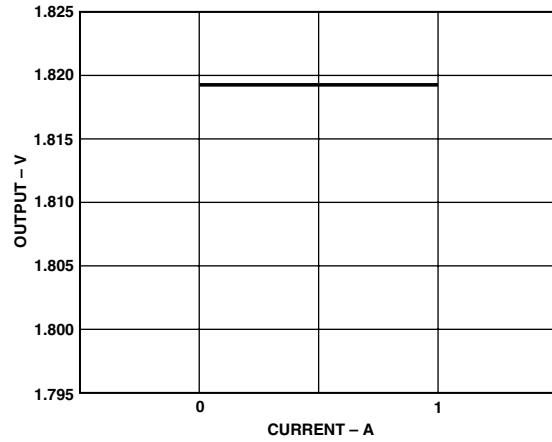


Figure 6. Load Regulation, Channel 2

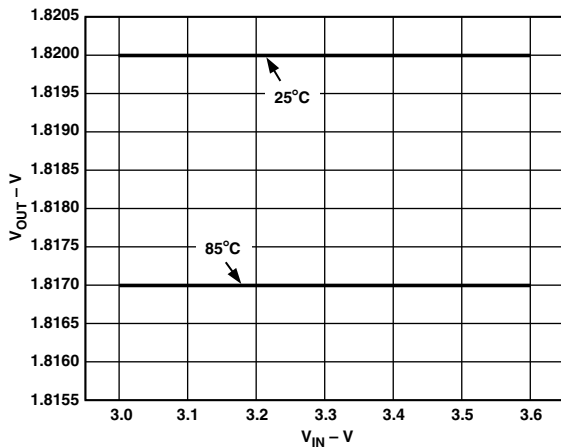


Figure 4. Line Regulation, Channel 2

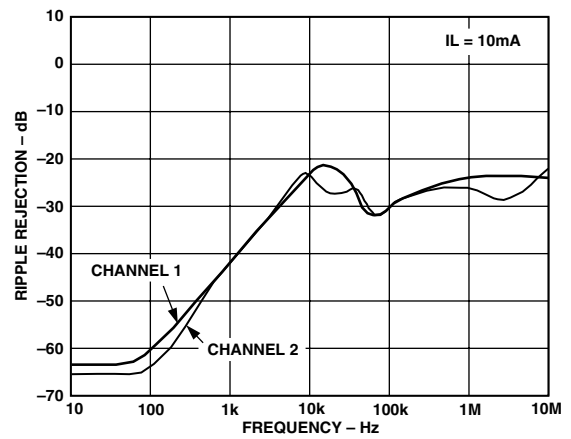


Figure 7. V_{CC} Supply Ripple Rejection

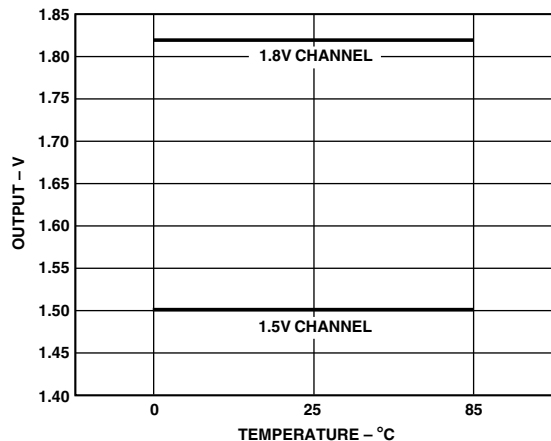


Figure 8. Regulator Output Voltage vs. Temperature

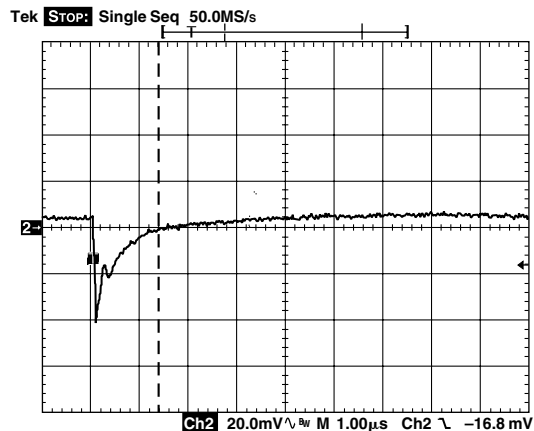


Figure 11. Transient Response Channel 1, 10 mA to 2 A Output Load Step

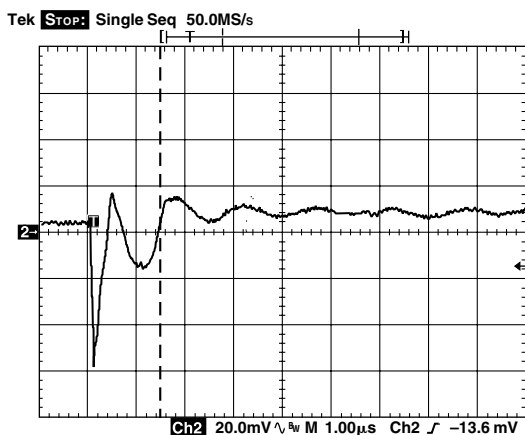


Figure 9. Transient Response Channel 1, 10 mA to 2 A Output Load Step

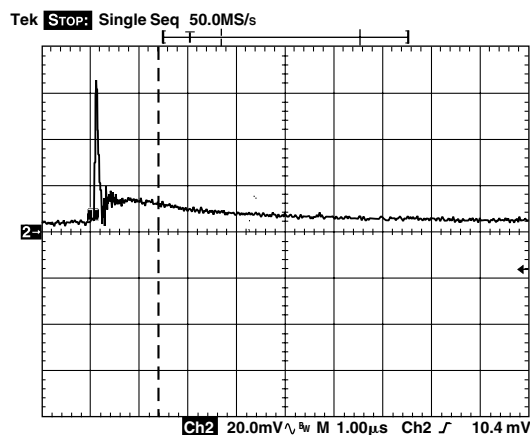


Figure 12. Transient Response Channel 2, 2 A to 10 mA Output Load Step

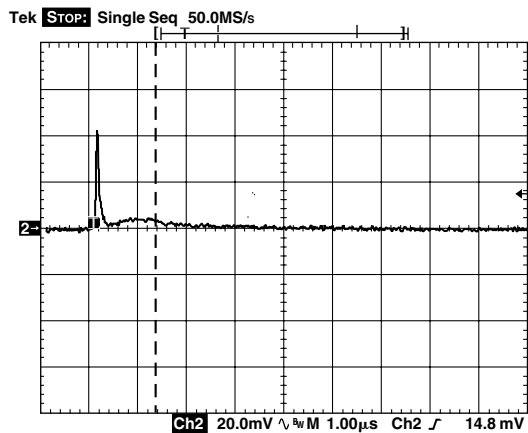


Figure 10. Transient Response Channel 1, 2 A to 10 mA Output Load Step

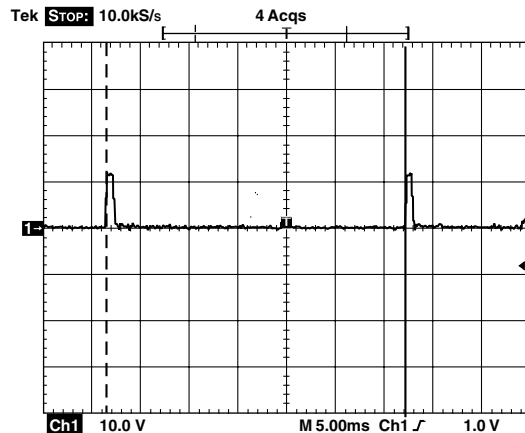


Figure 13. Force Output in Hiccup Mode, Channel 1

ADM1051

GENERAL DESCRIPTION

The ADM1051 is a dual, precision, voltage regulator controller intended for power rail generation and active bus termination in AGP and GTL applications on personal computer motherboards. It contains a precision 1.2 V bandgap reference and two almost identical channels consisting of control amplifiers driving external power devices. The main difference between the two channels is the regulated output voltage, defined by the resistor ratios on the voltage sense inputs of each channel. Channel 1 has an output of nominally 1.515 V, but can be switched to a 3.3 V output, while Channel 2 has a nominal output of 1.818 V. Channel 1 is also optimized for driving MOSFETs with lower on-resistance and higher gate capacitance, as explained later.

Each channel has a shutdown input to turn off amplifier output and protection circuitry for the external power device. The shutdown input of Channel 1 has additional functionality as described later.

The ADM1051 operates from a 12 V V_{CC} supply. The output is disabled until V_{CC} climbs above the reset threshold (6 V–9 V). The output from the ADM1051 is used to drive external N-channel MOSFETs, operating as source-followers. This has the advantage that N-channel devices are cheaper than P-channel devices of similar performance, and the circuit is easier to stabilize than one using P-channel devices in a common-source configuration.

The external power devices are protected by a Hiccup Mode circuit that operates if the circuit goes out of regulation due to an output short-circuit. In this case, the power device is pulsed on/off with a 1:40 duty cycle to limit the power dissipation until the fault condition is removed.

CIRCUIT DESCRIPTION

CONTROL AMPLIFIERS

The reference voltage is amplified and buffered by the control amplifiers and external MOSFETs, the output voltage of each channel being determined by the feedback resistor network between the sense input and the inverting input of the control amplifier.

The two control amplifiers in the ADM1051 are almost identical, apart, from the ratios of the feedback resistor networks on the sense inputs. A power-on reset circuit disables the amplifier output until V_{CC} has risen above the reset threshold (6 V–9 V).

Each amplifier output drives the gate of an N-channel power MOSFET, whose drain is connected to the unregulated supply input and whose source is the regulated output voltage, which is also fed back to the appropriate sense input of the ADM1051. The control amplifiers have high current-drive capability so they can quickly charge and discharge the gate capacitance of the external MOSFET, thus giving good transient response to changes in load or input voltage. In particular, Channel 1 is optimized to drive MOSFETs with very low on resistance and correspondingly higher gate capacitance such as the PHD55N03LT from Philips. This is to minimize voltage drop across the MOSFET when Channel 1 is used in 3.3 V mode, as explained later.

SHUTDOWN INPUTS AND TYPEDET COMPATIBILITY

Each channel has a separate shutdown input, which may be controlled by a logic signal and allows the output of the regulator to be turned on or off. If the shutdown input is held high or

not connected, the regulator operates normally. If the shutdown input is held low, the enable input of the control amplifier is turned off and the amplifier output goes low, turning off the regulator.

The $\overline{\text{SHDN 1}}$ input on Channel 1 has additional functionality that can be controlled by the TYPEDET signal on PC motherboards.

The AGP bus on a PC motherboard can have two different modes of operation, requiring different regulated voltages of 3.3 V or 1.5 V. These two modes are signaled by the TYPEDET signal on the PC motherboard, as follows:

TYPEDET = 0 V – Regulated Voltage 1.5 V (4× AGP Graphics)

TYPEDET floating – Regulated Voltage 3.3 V (2× AGP Graphics)

For compatibility with the TYPEDET signal, the regulator output voltage of Channel 1 may be selected using the shutdown pin. This is a multilevel, dual-function input that allows selection of the regulator output voltage as well as shutdown of the regulator.

By setting $\overline{\text{SHDN 1}}$ to different voltages, the regulator can be put into four different operating modes.

Table I. Shutdown Functionality for 1.5 V Channel

$\overline{\text{SHDN 1}}$ Voltage	Mode	Function
< 0.8 V	1	Force Output Low, Regulator Shutdown
2 V–3.9 V	2	1.5 V Output
4.3 V–5.3 V	3	Force Output High, $V_{OUT} = 3.3$ V
>6.2 V or Floating	4	1.5 V Output

If the $\overline{\text{SHDN 1}}$ pin is connected to a voltage less than 0.8 V, the FORCE output will go low and the regulator will be shut down.

If the $\overline{\text{SHDN 1}}$ pin is connected to a voltage greater than 6.2 V, or simply left open-circuit, the regulator will operate normally and provide 1.5 V output. This allows the regulator to operate normally with no external connection to $\overline{\text{SHDN 1}}$.

If the $\overline{\text{SHDN 1}}$ pin is connected to a voltage between 2 V and 3.9 V, the regulator will also operate normally and provide 1.5 V out.

If the $\overline{\text{SHDN 1}}$ pin is connected to a voltage between 4.3 V and 5.3 V, the FORCE output will be high and the external MOSFET will be turned hard on, making the output voltage equal to the 3.3 V input (less any small drop due to the on-resistance of the MOSFET). In this mode it is not actually regulating, but simply acting as a switch for the 3.3 V supply. The voltage drop across the Channel 1 MOSFET in Mode 3 can be minimized by using a MOSFET with very low on resistance, for which Channel 1 is optimized, such as the PHD55N03LT.

The latter two modes allow the regulator to be controlled by the TYPEDET signal simply by using potential divider, as shown in Figure 14.

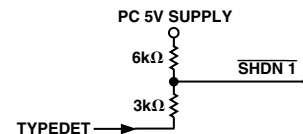


Figure 14. Using $\overline{\text{SHDN 1}}$ with TYPEDET Signal

A shutdown function can be added by connecting an open-drain/open-collector logic output to $\overline{\text{SHDN 1}}$, or by using a totem-pole logic output with a Schottky diode, as shown in Figure 15.

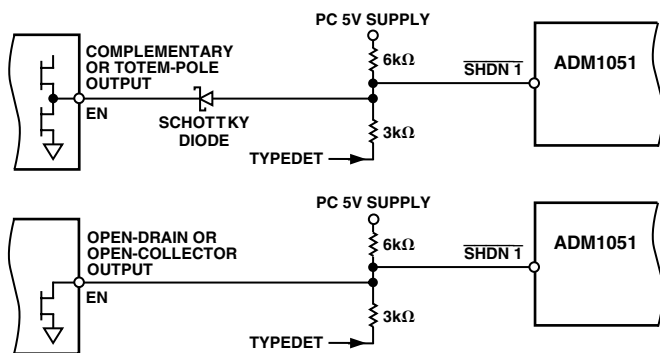


Figure 15. TYPEDET Voltage Selection Combined with Shutdown Function

When the logic output is high or turned off, the regulator mode will be controlled by TYPEDET. When the logic output is low, the regulator will be shut down.

Table II. TYPEDET and Shutdown Truth Table

TYPEDET	EN	Regulator Mode
X	0	Shutdown
0	1	1.5 V
1	1	3.3 V

X = Don't care.

HICCUP MODE FAULT PROTECTION

Hiccup mode fault protection is a simple method of protecting the external power device without the added cost of external sense resistors or a current sense pin on the ADM1051. In the event of a short-circuit condition at the output, the output voltage will fall. When the output voltage of a channel falls 20% below the nominal voltage, this is sensed by the hiccup comparator and the channel will go into hiccup mode, where the enable signal to the control amplifier is pulsed on and off with a 1:40 duty cycle.

To prevent the device inadvertently going into hiccup mode during power-up or during channel enabling, the hiccup mode is held off for approximately 60 ms on both channels. By this time the

output voltage should have reached its correct value. In the case of power-up, the hold-off period starts when V_{CC} reaches the power-on reset threshold of 6 V–9 V. In the case of channel enabling, the hold-off period starts when SHDN is taken high. Note that the hold-off timeout applies to both channels even if only one channel is disabled/enabled.

As the 3.3 V input to the drain of the MOSFET is not monitored, it should ideally rise at the same or a faster rate than V_{CC} . At the very least it must be available in time for V_{OUT} to reach its final value before the end of the power-on delay. If the output voltage is still less than 80% of the correct value after the power-on delay, the device will go into hiccup mode until the output voltage exceeds 80% of the correct value during a hiccup mode on-period. Of course, if there is a fault condition at the output during power-up, the device will go into hiccup mode after the power-up delay and remain there until the fault condition is removed.

The effect of power-on delay is illustrated in Figure 16. This shows an ADM1051 being powered up with a fault condition. The output current rises to a very high value during the power-on delay, then the device goes into hiccup mode and the output is pulsed on and off at 1:40 duty cycle. When the fault condition is removed, the output voltage recovers to its normal value at the end of the hiccup mode off period.

The load current at which the ADM1051 will go into hiccup mode is determined by three factors:

- the input voltage to the drain of the MOSFET, V_{IN}
- the output voltage V_{OUT} (–20%)
- the on-resistance of the MOSFET, R_{ON}

$$I_{HICCUP} = (V_{IN} - (0.8 \times V_{OUT})) / R_{ON}$$

It should be emphasized that the hiccup mode is not intended as a precise current limit but as a simple method of protecting the external MOSFET against catastrophic fault conditions such as output short-circuits.

APPLICATIONS INFORMATION

PCB LAYOUT

For optimum voltage regulation, the loads should be placed as close as possible to the source of the output MOSFETs and

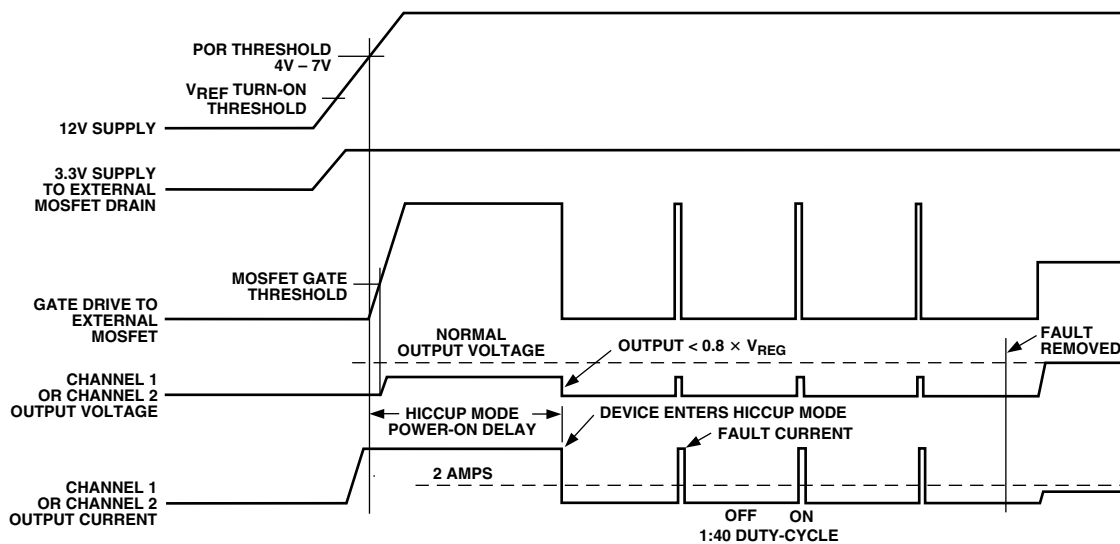


Figure 16. Power-On Reset and Hiccup Mode

ADM1051

feedback to the sense inputs should be taken from a point as close to the loads as possible. The PCB tracks from the loads back to the sense inputs should be separate from the output tracks and not carry any load current.

Similarly, the ground connection to the ADM1051 should be made as close as possible to the ground of the loads, and the ground track from the loads to the ADM1051 should not carry load current. Good and bad layout practice is illustrated in Figure 17.

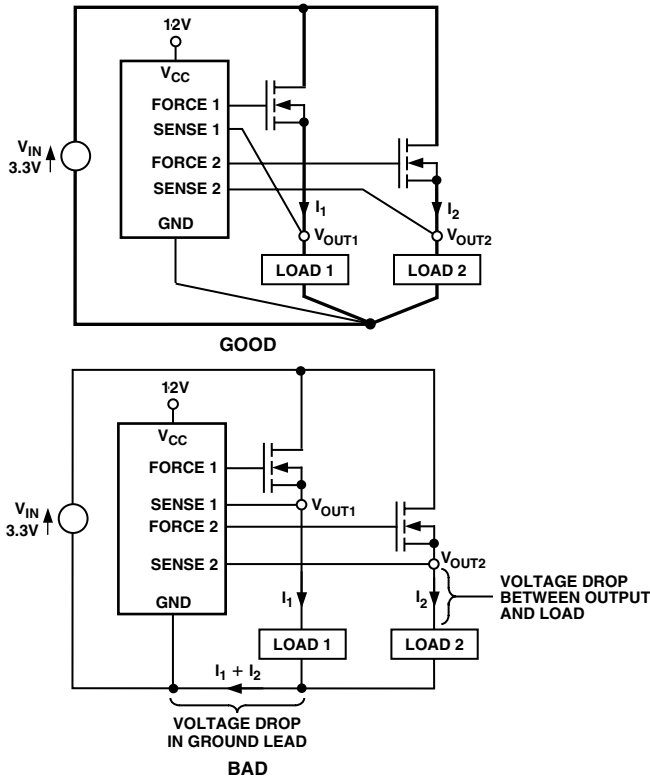


Figure 17. Good and Bad Layout Practice

SUPPLY DECOUPLING

The supply to the drain of an external MOSFET should be decoupled as close as possible to the drain pin of the device, with at least 100 μF to ground. The output from the source of the MOSFET should be decoupled as close as possible to the source pin of the device. Decoupling capacitors should be chosen to have a low Equivalent Series Resistance (ESR), typically 50 m Ω or lower. With the MOSFETs specified, and two 100 μF capacitors in parallel, the circuit will be stable for load currents up to 2 A. The V_{CC} pin of the ADM1051 should be decoupled with at least 1 μF to ground, connected as close as possible to the V_{CC} and GND pins.

In practice, the amount of decoupling required will depend on the application. PC motherboards are notoriously noisy environments, and it may be necessary to employ distributed decoupling to achieve acceptable noise levels on the supply rails.

CHOICE OF MOSFET

As previously discussed, the load current at which an output goes into hiccup mode depends on the on-resistance of the external MOSFET. If the on-resistance is too low, this current may be very high; if the on-resistance is high, the trip current may be lower than the maximum required load current. For the primary

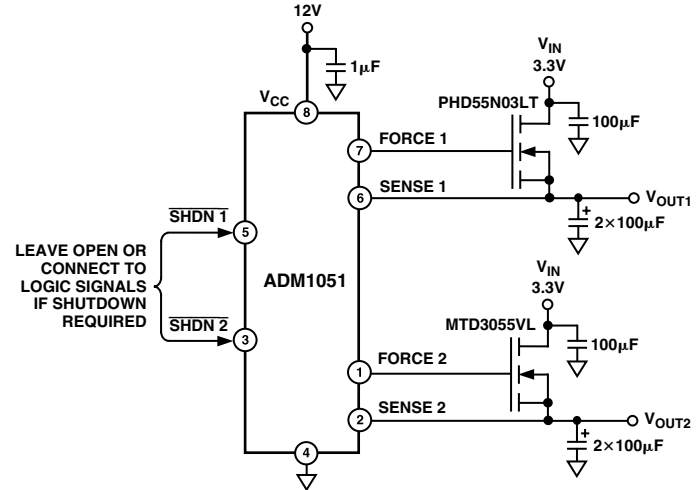


Figure 18. Typical Application Circuit

application of AGP and GTL power supplies and bus termination on personal computer motherboards, devices with very low on-resistance such as the PHD55N03LT from Philips, or the SUB60N06-18 from Siliconix are suitable. For Channel 2, suitable devices are the MTD3055VL from Motorola and the PHB11N06LT from Philips.

THERMAL CONSIDERATIONS

Heat generated in the external MOSFET must be dissipated and the junction temperature of the device kept within acceptable limits. The power dissipated in the device is, of course, the drain-source voltage multiplied by the load current. The required thermal resistance to ambient is given by

$$\theta_{JA} = T_{J(MAX)} - T_{AMB(MAX)} / (V_{DS(MAX)} \times I_{OUT(MAX)})$$

Surface-mount MOSFETs such as those specified must rely on heat conduction through the device leads and the PCB. One square inch of copper (645 sq. mm) gives a thermal resistance of around 60°C/W for an SOT-223 surface-mount package and 80°C/W for an SO-8 surface-mount package.

For high power dissipation that can be accommodated by a surface-mount package, D²PAK or TO-220 devices are recommended. These should be mounted on a heatsink with a thermal resistance low enough to maintain the required maximum junction temperature.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead SOIC (Narrow Body, R-8)

