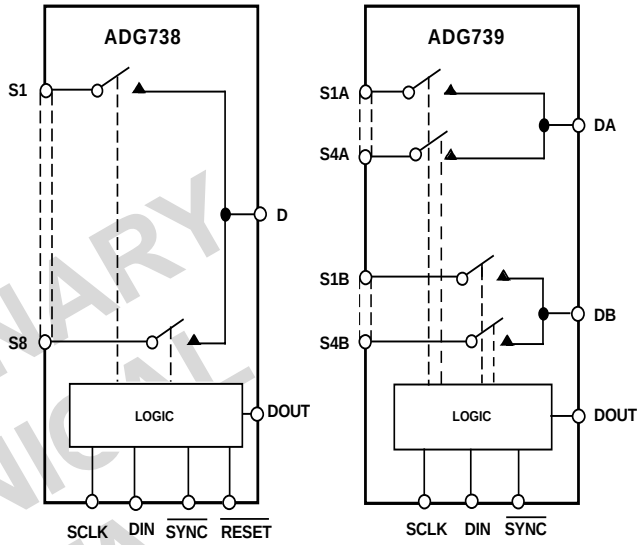
CMOS, Low Voltage, Serially Controlled Matrix Switches

Preliminary Technical Data — ADG738/ADG739

FEATURES
Three wire Serial Interface
+2.7 V to +5.5 V Single Supply
Low On Resistance (4 Ω)
Low On Resistance Flatness
Low Leakage
Single 8 to 1 Multiplexer ADG738
Dual 4 to 1 Multiplexer ADG739
Power on Reset
Fast Switching Times
Low Power Consumption
TTL/CMOS compatible

APPLICATIONS
Data Acquisition Systems
Communication Systems
Relay replacement
Audio and Video Switching

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG738 and ADG739 are CMOS analog matrix switches with a serially controlled three wire interface. The ADG738 is an 8 channel matrix switch, while the ADG739 is a dual 4 channel matrix switch. On resistance is closely matched between switches and very flat over the full signal range.

The ADG738 and ADG739 utilize a three wire serial interface that is compatible with SPI™, QSPI™ and MICROWIRE™ interface standards. The output of the shift register DOUT enables a number of these parts to be daisy chained. On power up of the devices, the internal shift register contains all zeros and all switches are in the OFF state.

Each switch conducts equally well in both direction when on, making these parts suitable for both multiplexing and demultiplexing applications. As each switch is turned on or off by a seperate bit, these parts can also be configured as a type of switch array, where any, all or none of the 8 switches may be closed at any time. The input signal range extends to the supply rails.

All channels exhibit break before make switching action preventing momentary shorting when switching channels.

The ADG738 and ADG739 are available in 16 lead TSSOP package.

PRODUCT HIGHLIGHTS

1. Three Wire Serial Interface.
2. Single Supply Operation. The ADG738 and ADG739 are fully specified and guaranteed with +3 V and +5 V supply rails.
3. Low R_{ON} (4 Ω).
4. Any configuration of switches may be on or off at any one time.
5. Break before make switching action.
6. Small 16 lead TSSOP package.

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MICROWIRE is a trademark of National Semiconductor Corporation.

REV. PrC August '99

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ADG738/ADG739–SPECIFICATIONS[1]

(V_{DD} = +5 V ±10%, GND = 0 V. All specifications –40°C to +85°C unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On-Resistance (R_{ON})	2.5		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA;
	4	4.5	Ω max	Test Circuit 1;
On-Resistance Match Between		0.1	Ω typ	
Channels (ΔR_{ON})		0.4	Ω max	V_S = 0 V to V_{DD} , Is = 10 mA;
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.75		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA;
		1.2	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
	±0.1	±0.3	nA max	Test Circuit 2;
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
	±0.1	±0.3	nA max	Test Circuit 3;
Channel ON Leakage I_D (ON)	±0.01		nA typ	V_D = V_S = 1 V, or 4.5V;
	±0.1	±0.3	nA max	Test Circuit 4;
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
C_{IN}, Digital Input Capacitance	3		pF typ	
DIGITAL OUTPUTS				
DOUT Output High Voltage		V_{DD}	max	
DOUT Output Low Voltage		0.4	max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	30		ns typ	R_L = 300 Ω, C_L = 35 pF;
		TBD	ns max	V_S = 3 V, Test Circuit 5;
t_{OFF}	21		ns typ	R_L = 300 Ω, C_L = 35 pF;
		TBD	ns max	V_S = 3 V, Test Circuit 5;
Break-Before-Make Time Delay, t_D	15		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_S = 3.5 V, Test Circuit 6
Charge Injection	5		pC typ	V_S = 2 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 8;
Off Isolation	-60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz; Test Circuit 9;
Channel to Channel Crosstalk	-60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz; Test Circuit 10;
-3 dB Bandwidth	200		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 11;
C_S (OFF)	TBD		pF typ	
C_D (OFF)	TBD		pF typ	
C_D, C_S (ON)	TBD		pF typ	
POWER REQUIREMENTS				V_{DD} = +5.5 V
I_{DD}	10		µA typ	Digital Inputs = 0 V or 5.5 V
		TBD	µA max	

NOTES

[1]Temperature range is as follows: B Version: –40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS[1] (V_{DD} = 3V ± 10%, GND = 0 V. All specifications -40°C to +85°C, unless otherwise noted.)

Parameter	B Version +25°C	B Version –40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On-Resistance (R_{ON})	4.5	5	Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA;
		8	Ω max	Test Circuit 1;
On-Resistance Match Between Channels (ΔR_{ON})	0.1		Ω typ	V_S = 0 V to V_{DD} , Is = 10 mA;
		0.4	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)		2.5	Ω max	V_S = 0 V to V_{DD}, I_S = 10 mA;
LEAKAGE CURRENTS				V_{DD} = +3.3 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V;
	±0.1	±0.3	nA max	Test Circuit 2;
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	V_S = 1 V/3 V, V_D = 3 V/1 V;
	±0.1	±0.3	nA max	Test Circuit 3;
Channel ON Leakage I_D (ON)	±0.01		nA typ	V_S = V_D = +1 V or +3 V;
	±0.1	±0.3	nA max	Test Circuit 4;
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.4	V max	
Input Current, I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
C_{IN}, Digital Input Capacitance	3		pF typ	
DIGITAL OUTPUTS				
DOUT Output High Voltage		V_{DD}	max	
DOUT Output Low Voltage		0.4	max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	35		ns typ	R_L = 300 Ω, C_L = 35 pF;
		TBD	ns max	V_S = 2 V, Test Circuit 5;
t_{OFF}	27		ns typ	R_L = 300 Ω, C_L = 35 pF;
		TBD	ns max	V_S = 2 V, Test Circuit 5;
Break-Before-Make Time Delay, t_D	15		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_S = 2 V, Test Circuit 6
Charge Injection	5		pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 8;
Off Isolation	-60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz; Test Circuit 9;
Channel to Channel Crosstalk	-60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz; Test Circuit 10;
-3 dB Bandwidth	200		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 11;
C_S (OFF)	TBD		pF typ	
C_D (OFF)	TBD		pF typ	
C_D, C_S (ON)	TBD		pF typ	
POWER REQUIREMENTS				V_{DD} = +3.3 V
I_{DD}	10		µA typ	Digital Inputs = 0 V or 3.3 V
		TBD	µA max	

NOTES
[1]Temperature ranges are as follows: B Versions: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1,2] (V_{DD} = +2.5V to +5.5V. All specifications -40°C to +85°C, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX}	Units	Conditions/Comments
t_1	33	ns min	SCLK Cycle time
t_2	13	ns min	SCLK High Time
t_3	13	ns min	SCLK Low Time
t_4	0	ns min	$\overline{SYNC}$ to SCLK active edge setup time
t_5	5	ns min	Data Setup Time
t_6	4.5	ns min	Data Hold Time
t_7	0	ns min	SCLK Falling edge to $\overline{SYNC}$ Rising edge
t_8	33	ns min	Minimum $\overline{SYNC}$ high time
t_9	20	ns min	SCLK rising edge to DOUT valid

NOTES
[1]See Figure 1.
[2]All input signals are specified with tr =tf = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

Specifications subject to change without notice.

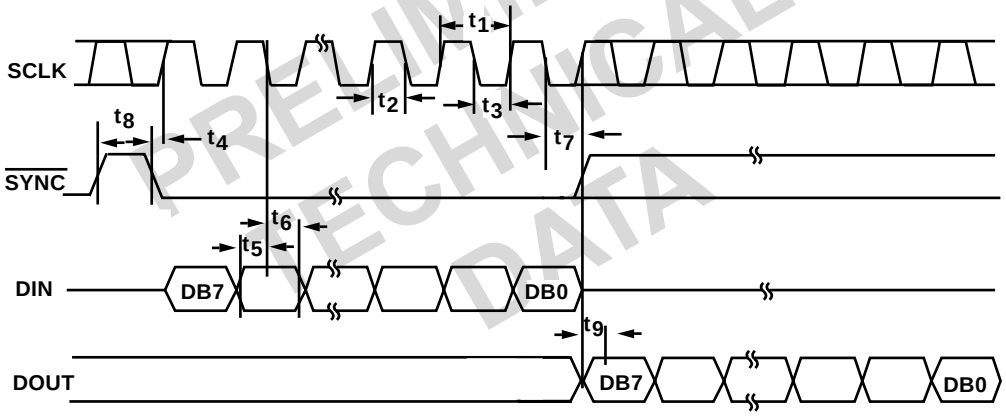
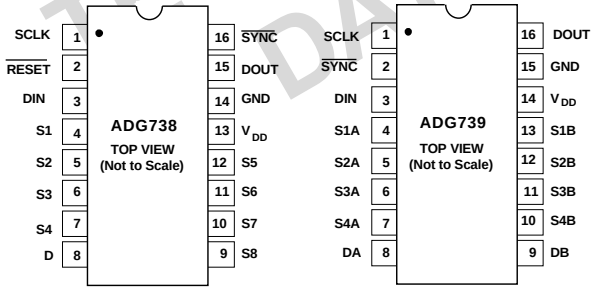


Figure 1. 3-Wire Serial Interface Timing Diagram.

PIN FUNCTION DESCRIPTION

ADG738	ADG739	Mnemonic	Function
1	1	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. These devices can accomodate serial input rates of up to 30MHz.
2	-	$\overline{\text{RESET}}$	Active low control input that clears the input register and turns all switches to the OFF condition.
3	3	DIN	Serial Data Input. Data is clocked into the 8-bit input register on the falling edge of the serial clock input.
4,5,6,7	4,5,6,7	SXX	Source. May be an input or output.
8	8,9	DX	Drain. May be an input or output.
9,10,11,12	10,11,12,13	SXX	Source. May be an input or output.
13	14	V_{DD}	Power Supply Input. These parts can be operated from a supply of +2.5V to +5.5V.
14	15	GND	Ground reference.
15	16	DOUT	Data Output. This allows a number a parts to be daisy chained. Data is clocked out of the input shift register on the rising edge of SCLK.
16	2	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and the input shift register is enabled. Data is transferred on the falling edges of the following 8 clocks. Taking $\overline{\text{SYNC}}$ high, updates the switches.

PIN CONFIGURATIONS



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG738BRU	-40 °C to +85 °C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG739BRU	-40 °C to +85 °C	Thin Shrink Small Outline Package (TSSOP)	RU-16

TERMINOLOGY

R_{ON}	Ohmic resistance between D and S.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	"OFF" switch source capacitance. Measured with reference to ground.
C_D (OFF)	"OFF" switch drain capacitance. Measured with reference to ground.
C_D,C_S(ON)	"ON" switch capacitance. Measured with reference to ground.
C_{IN}	Digital input capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on. See test circuit 4.
t_{OFF}	Delay between applying the digital control input and the output switching off.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Bandwidth	The frequency at which the output is attenuated by -3dBs.
On Response	The Frequency response of the "ON" switch.
On Loss	The voltage drop across the "ON" switch seen on the On Response vs. Frequency plot as how many dBs the signal is away from 0dB.
V_{INL}	Maximum input voltage for logic "0".
V_{INH}	Minimum input voltage for logic "1".
I_{INL}(I_{INH})	Input current of the digital input.
I_{DD}	Positive supply current.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	–0.3 V to +7 V
Analog, Digital Inputs[2]	-0.3V to V_{DD} +0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D	100mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, each S	30mA
Continuous Current D, ADG729	80mA
Continuous Current D, ADG728	120mA
Operating Temperature Range	
Industrial (B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
TSSOP Package, Power Dissipation	mW
θ_{JA} Thermal Impedance	150.4°C/W
θ_{JC} Thermal Impedance	27.6°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C
ESD	2kV

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG738/ADG739 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

GENERAL DESCRIPTION

The ADG738 and ADG739 are serially controlled, 8 channel and dual 4 channel matrix switches respectively. While providing the normal multiplexing and demultiplexing functions, these parts also provide the user with some more flexibility as to where their signal may be routed. Each bit of the 8 bit serial word corresponds to one switch of the part. A logic '1' in the particular bit position turns on the switch, while a logic '0' turns the switch off. Because each switch is independently controlled by an individual bit, this provides the option of having any, all or none of the switches ON. This feature may be particularly useful in the demultiplexing application where the user may wish to direct one signal from the drain to a number of outputs (sources). Care must be taken, however, in the multiplexing situation where a number of inputs may be shorted together, (only separated by the small on resistance of the switch).

POWER ON RESET

On power up of the device, all switches will be in the OFF condition and the internal shift register is filled with zeros and will remain so until a valid write takes place.

SERIAL INTERFACE

The ADG738 and ADG739 have a three wire serial interface ($\overline{SYNC}$, SCLK, and DIN), which is compatible with SPI, QSPI, MICROWIRE interface standards and most DSP's. Figure 1 shows the timing diagram of a typical write sequence.

Data is written to the 8-bit shift register via DIN under the control of the $\overline{SYNC}$ and SCLK signals. Data may be written to the shift register in more or less than 8 bits. In each case the shift register retains the last eight bits that were written.

When $\overline{SYNC}$ goes low, the input shift register is enabled. Data from DIN is clocked into the shift register on the falling edge of SCLK. Each bit of the eight bit word corresponds to one of the eight switches. Figure 2 shows the contents of the input shift register. Data appears on the DOUT pin on the rising edge of SCLK suitable for daisy chaining, delayed of course by eight bits. When all eight bits have been written into the shift register, the $\overline{SYNC}$ line is brought high again. The switches are updated with the new configuration and the input shift register is disabled. With $\overline{SYNC}$ held high, any further data or noise on the DIN line will have no effect on the shift register.

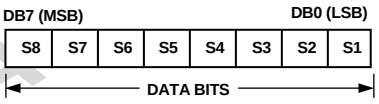


Figure 2. Input Shift Register Contents

TEST CIRCUITS

TBD

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead TSSOP
(RU-16)