ANALOG DEVICES

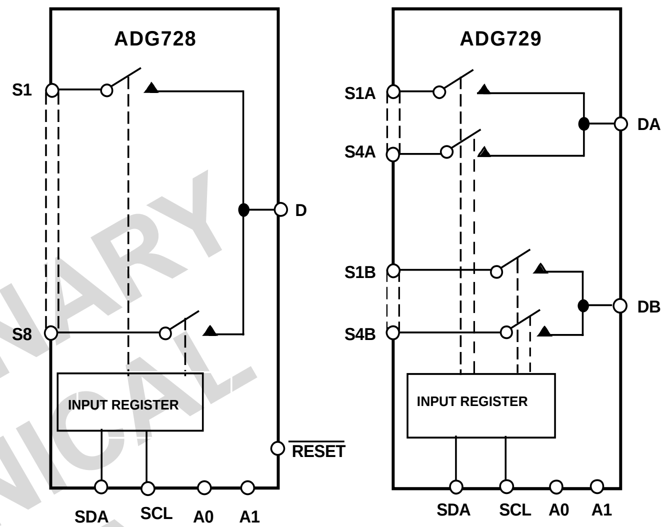
CMOS, Low Voltage, 2 Wire, Serially Controlled Matrix Switches

Preliminary Technical Data — ADG728/ADG729

FEATURES
Two Wire Serial Interface
+2.7 V to +5.5 V Single Supply
Low On Resistance (4 Ω)
Low On Resistance Flatness
Low Leakage
Single 8 to 1 Matrix Switch ADG728
Dual 4 to 1 Matrix Switch ADG729
Power On Reset
Fast Switching Times
Low Power Consumption

APPLICATIONS
Data Acquisition Systems
Communication Systems
Relay replacement
Audio and Video Switching

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG728 and ADG729 are CMOS analog matrix switches with a serially controlled two wire interface. The ADG728 is an 8 channel matrix switch, while the ADG729 is a dual 4 channel matrix switches. On resistance is closely matched between switches and very flat over the full signal range. These parts can operate equally well as either Multiplexers, De-Multiplexers or Switch arrays and the input signal range extends to the supplies.

The ADG728 and ADG729 utilize a two wire serial interface that is compatible with the I^2C^{TM} interface standard. Both have two external address pins (A0 and A1). This allows the 2 LSB's of the 7-bit slave address to be set by the user. Four of each devices can be connected to the one bus. The ADG728 also has a $\overline{\text{RESET}}$ pin, this should be tied high if not in use.

Each channel is controlled by one bit of an 8 bit word. This means that these devices may be used in a number of different configurations, all, any or none of the channels may be on at any one time.

On power up of the device, all switches will be in the OFF condition and the internal shift register will contain all zeros.

All channels exhibit break before make switching action preventing momentary shorting when switching channels.

The ADG728 and ADG729 are available in a 16 lead TSSOP package.

PRODUCT HIGHLIGHTS

1. Two Wire Serial Interface.
2. Single Supply Operation. The ADG728 and ADG729 are fully specified and guaranteed with +3 V and +5 V supply rails.
3. Low R_{ON} (4 Ω).
4. Any configuration of switches may be on at any one time.
5. Break before make switching action.
6. Small 16 lead TSSOP package.

I^2C is a trademark of Philips Corporation.

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ADG728/ADG729–SPECIFICATIONS[1] (V_{DD} = +5 V ±10%, GND = 0 V)

Parameter	B Version +25°C	B Version –40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On-Resistance (R_{ON})	2.5		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA;
	4	4.5	Ω max	Test Circuit 1;
On-Resistance Match Between		0.1	Ω typ	
Channels (ΔR_{ON})		0.4	Ω max	V_S = 0 V to V_{DD} , I_S = 10 mA;
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.75		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA;
		1.2	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
	±0.1	±0.3	nA max	Test Circuit 2;
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
	±0.1	±0.3	nA max	Test Circuit 2;
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_D = V_S = 1 V, or 4.5V;
	±0.1	±0.3	nA max	Test Circuit 3;
LOGIC INPUTS (A0, A1)[2]				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	
		±0.1	µA max	
Cin, Input Capacitance	3		pF typ	
LOGIC INPUTS (SCL, SDA)[2]				
Input High Voltage, V_{INH}		0.7V_{DD}	V min	
		V_{DD} +0.3	Vmax	
Input Low Voltage, V_{INL}		-0.3	V min	
		0.3V_{DD}	V max	
I_{IN}, Input Leakage Current	TBD		µA typ	V_{IN} = 0V to V_{DD}.
		±TBD	µA max	
V_{HYST}, Input Hysteresis	0.05V_{DD}		V min	
C_{IN}, Input Capacitance	3		pF typ	
LOGIC OUTPUT (SDA)[2]				
V_{OL}, Output Low Voltage		0.4	V max	I_{SINK} = 3 mA
		0.6	V max	I_{SINK} = 6 mA
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	30		ns typ	R_L = 300 Ω, C_L = 35 pF;
		TBD	ns max	V_S = 3 V, Test Circuit 4;
t_{OFF}	21		ns typ	R_L = 300 Ω, C_L = 35 pF;
		TBD	ns max	V_S = 3 V, Test Circuit 4;
Break-Before-Make Time Delay, t_D	15		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_{S1} = V_{S2} = 3 V, Test Circuit 5
Charge Injection	5		pC typ	V_S = 2 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 5;
Off Isolation	-60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10MHz; Test Circuit 6;
Crosstalk	-80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10MHz; Test Circuit 7;
-3 dB Bandwidth	200		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 6;
C_S (OFF)	TBD		pF typ	
C_D (OFF)	TBD		pF typ	
C_D, C_S (ON)	TBD		pF typ	
POWER REQUIREMENTS				V_{DD} = +5.5 V
I_{DD}	10		µA typ	Digital Inputs = 0 V or 5.5 V
		TBD	µA max	

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

ADG728/ADG729–SPECIFICATIONS[1] (V_{DD} = +5 V ±10%, GND = 0 V)

Parameter	+25°C	–40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On-Resistance (R_{ON})	4.5	5	Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA;
		8	Ω max	Test Circuit 1;
On-Resistance Match Between	0.1		Ω typ	V_S = 0 V to V_{DD} , I_S = 10 mA;
Channels (ΔR_{ON})		0.4	Ω max	V_S = 0 V to V_{DD}, I_S = 10 mA;
On-Resistance Flatness ($R_{FLAT(ON)}$)		2.5	Ω max	
LEAKAGE CURRENTS				V_{DD} = +3.3 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V;
	±0.1	±0.3	nA max	Test Circuit 2;
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	V_S = 1 V/3 V, V_D = 3 V/1 V;
	±0.1	±0.3	nA max	Test Circuit 2;
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_S = V_D = +1 V or +3 V;
	±0.1	±0.3	nA max	Test Circuit 3;
LOGIC INPUTS (A0, A1)[2]				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.4	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	
		±0.1	μA max	
Cin, Input Capacitance	3		pF typ	
LOGIC INPUTS (SCL, SDA)[2]				
Input High Voltage, V_{INH}		0.7V_{DD}	V min	
		V_{DD} +0.3	Vmax	
Input Low Voltage, V_{INL}		-0.3	V min	
		0.3V_{DD}	V max	
I_{IN}, Input Leakage Current	TBD		μA typ	V_{IN} = 0V to V_{DD}.
		±TBD	μA max	
V_{HYST}, Input Hysteresis	0.05V_{DD}		V min	
C_{IN}, Input Capacitance	3		pF typ	
LOGIC OUTPUT (SDA)[2]				
V_{OL}, Output Low Voltage		0.4	V max	I_{SINK} = 3 mA
		0.6	V max	I_{SINK} = 6 mA
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	35		ns typ	R_L = 300 Ω, C_L = 35 pF;
		TBD	ns max	V_S = 2 V, Test Circuit 4;
t_{OFF}	27		ns typ	R_L = 300 Ω, C_L = 35 pF;
		TBD	ns max	V_S = 2 V, Test Circuit 4;
Break-Before-Make Time Delay, t_D	15		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_{S1} = V_{S2} = 2 V, Test Circuit 5
Charge Injection	5		pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 5;
Off Isolation	-60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz; Test Circuit 6;
Crosstalk	-80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10MHz; Test Circuit 7;
-3 dB Bandwidth	200		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 6;
C_S (OFF)	TBD		pF typ	
C_D (OFF)	TBD		pF typ	
C_D, C_S (ON)	TBD		pF typ	
POWER REQUIREMENTS				V_{DD} = +3.3 V
I_{DD}	10		μA typ	Digital Inputs = 0 V or 3.3 V
		TBD	μA max	

NOTES
[1]Temperature ranges are as follows: B Versions: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +2.5 V to +5.5 V . All specifications –40°C to +85°Cunless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX}	Units	Conditions/Comments
FSCL	400	kHz max	SCL Clock Frequency
t_1	2.5	µs min	SCL Cycle Time
t_2	0.6	µs min	t_{HIGH}, SCL High Time
t_3	1.3	µs min	t_{LOW}, SCL Low Time
t_4	0.6	µs min	$t_{HD, STA}$, Start/Repeated Start Condition Hold Time
t_5	100	ns min	$t_{SU, DAT}$, Data Setup Time
t_6[2]	0.9	µs max	$t_{HD, DAT}$, Data Hold Time
	0	µs min	
t_7	0.6	µs min	$t_{SU, STA}$, Setup Time for Repeated Start
t_8	0.6	µs min	$t_{SU, STO}$, Stop Condition Setup Time
t_9	1.3	µs min	t_{BUF}, Bus Free Time Between a STOP Condition and a Start Condition
t_{10}	300	ns max	t_R, Rise Time of both SCL and SDA when receiving
	20 + 0.1C_b[3]	ns min	
t_{11}	250	ns max	t_F, Fall Time of SDA when receiving
	300	ns max	t_F, Fall Time of both SCL and SDA when transmitting
	20 + 0.1C_b[3]	ns min	
C_b	400	pF max	Capacitive Load for Each Bus Line
t_{SP}[4]	50	ns max	Pulse width of spike suppressed

NOTES
[1]See Figure 1.
[2]A master device must provide a hold time of at least 300ns for the SDA signal (referred to the V_{IH} min of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
[3]C_b is the total capacitance of one bus line in pF. t_R and t_F measured between 0.3V_{DD} and 0.7V_{DD}.
[4]Input filtering on both the SCL and SDA inputs suppress noise spikes which are less than 50ns.

Specifications subject to change without notice.

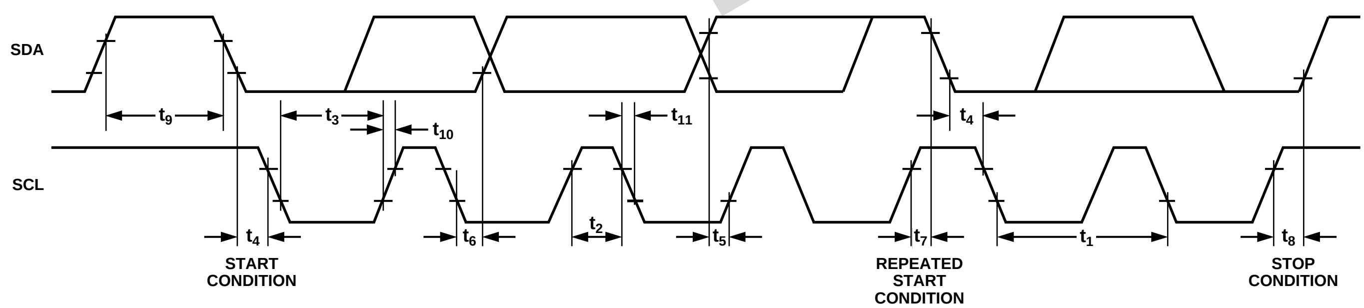


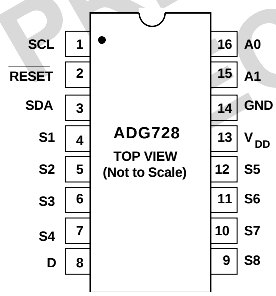
Figure 1. 2-Wire Serial Interface Timing Diagram.

PIN FUNCTION DESCRIPTION

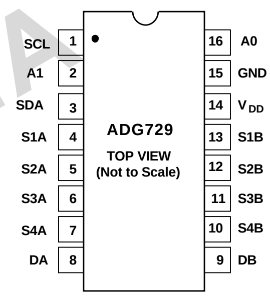
ADG728	ADG729	Mnemonic	Function
1	1	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into the 16-bit input shift register. Clock rates of up to 400kbit/s can be accommodated with this 2-wire serial interface.
2	-	$\overline{RESET}$	Active low control input that clears the input register and turns all switches to the OFF condition.
3	3	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into the 8-bit input shift register during the write cycle and used to read back 1 byte of data during the read cyle. It is a bidirectional open-drain data line which should be pulled to the supply with an external pull-up resistor.
4,5,6,7	4,5,6,7	SXX	Source. May be an input or output.
8	8,9	DX	Drain. May be an input or output.
9,10,11,12	10,11,12,13	SXX	Source. May be an input or output.
13	14	V_{DD}	Power Supply Input. These parts can be operated from a supply of +2.5V to +5.5V.
14	15	GND	Ground reference.
15	2	A1	Address Input. Sets the 2nd Least Significant bit of the 7 bit slave address.
16	16	A0	Address Input. Sets the Least Significant bit of the 7 bit slave address.

PIN CONFIGURATIONS

ADG728



ADG729



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG728BRU	-40 °C to +85 °C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG729BRU	-40 °C to +85 °C	Thin Shrink Small Outline Package (TSSOP)	RU-16

TERMINOLOGY

R_{ON}	Ohmic resistance between D and S.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	"OFF" switch source capacitance.
C_D (OFF)	"OFF" switch drain capacitance.
C_D,C_S(ON)	"ON" switch capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on. See test circuit 4.
t_{OFF}	Delay between applying the digital control input and the output switching off.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Bandwidth	The frequency at which the output is attenuated by -3dBs.
On Response	The Frequency response of the "ON" switch.
On Loss	The voltage drop across the "ON" switch seen on the On Response vs. Frequency plot as how many dBs the signal is away from 0dB.
V_{INL}	Maximum input voltage for logic "0".
V_{INH}	Minimum input voltage for logic "1".
I_{INL}(I_{INH})	Input current of the digital input.
I_{DD}	Positive supply current.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	–0.3 V to +7 V
Analog, Digital Inputs[2]	-0.3V to V_{DD} +0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D	100mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, each S	30mA
Continuous Current D, ADG729	80mA
Continuous Current D, ADG728	120mA
Operating Temperature Range	
Industrial (B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
TSSOP Package, Power Dissipation	mW
θ_{JA} Thermal Impedance	150.4°C/W
θ_{JC} Thermal Impedance	27.6°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C
ESD	TBDkV

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG728/ADG729 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

GENERAL DESCRIPTION

The ADG728 and ADG729 are serially controlled, 8 channel and dual 4 channel matrix switches respectively. While providing the normal multiplexing and demultiplexing functions, these devices also provide the user with some more flexibility as to where their signal may be routed. Each bit of the serial word corresponds to one switch of the device. A logic '1' in the particular bit position turns on the switch, while a logic '0' turns the switch off. Because each switch is independently controlled by an individual bit, this provides the option of having any, all or none of the switches ON. This feature may be particularly useful in the demultiplexing application where the user may wish to direct one signal from the drain to a number of outputs (sources). Care must be taken, however, in the multiplexing situation where a number of inputs may be shorted together, (only seperated by the small on resistance of the switch).

POWER ON RESET

On power up of the device, all switches will be in the OFF condition and the internal shift register is filled with zeros and will remain so until a valid write takes place.

SERIAL INTERFACE

2-WIRE SERIAL BUS

The ADG728/ADG729 are controlled via an I^{2}C compatible serial bus. These parts are connected to this bus as a slave device (no clock is generated by the multiplexer)

The ADG728/ADG729 have different 7-bit slave addresses. The five MSBs of the ADG728 are 10011, while the MSB's of the ADG729 are 10001 and the two LSBs are determined by the state of the A0 and A1 pins.

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition which is when a high to low transition on the SDA line occurs while SCL is high. The following byte is the address byte which consists of the 7-bit slave address followed by a R/$\overline{W}$ bit (this bit determines whether data will be read from or written to the slave device).

The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the Acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{W}$ bit is high, the master will read from the slave device. However, if the R/$\overline{W}$ bit is low, the master will write to the slave device.

2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an Acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.

3) When all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low to high transition on the SDA line while SCL is high. In Write mode, the master will pull the SDA line high during the 10th clock pulse to establish a STOP condition. In Read mode, the master will issue a No Acknowledge for the 9th clock pulse (i.e. the SDA line remains high). The master will then bring the SDA line low before the 10th clock pulse and then high during the 10th clock pulse to establish a STOP condition.

See Figure 3 below for a graphical explanation of the serial interface.

A repeated write function gives the user flexibility to update the matrix switch a number of times after addressing the part only once. During the write cycle, each data byte will update the configuration of the switches. For example, after the matrix switch has acknowledged its address byte, and receives one data byte, the switches will update after the data byte, if another data byte is written to the matrix switch while it is still the addressed slave device, this data byte will also cause an switch configuration update. Repeat read of the matrix switch is also allowed.

INPUT SHIFT REGISTER

The input shift register is 8-bits wide. Figure 2 illustrates the contents of the input shift register. Data is loaded into the device as an 8-bit word under the control of a serial clock input, SCL. The timing diagram for this operation is shown in Figure 1. The 8-bit word consists of 8 data bits each controlling one switch. MSB (Bit 7) is loaded first.

DB7 (MSB) — DB0 (LSB)

S8	S7	S6	S5	S4	S3	S2	S1

← DATA BITS →

Figure 2. ADG728/ADG729 Input Shift Register Contents

WRITE OPERATION

When writing to the ADG728/ADG729, the user must begin with an address byte and R/$\overline{W}$ bit, after which the switch will Acknowledge that it is prepared to receive data by pulling SDA low. This address byte is followed by the 8-bit word. The write operations for each matrix switch are shown in the figures below.

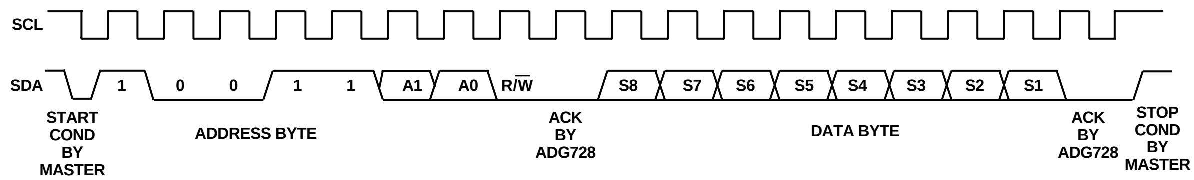


Figure 3. ADG728 Write Sequence

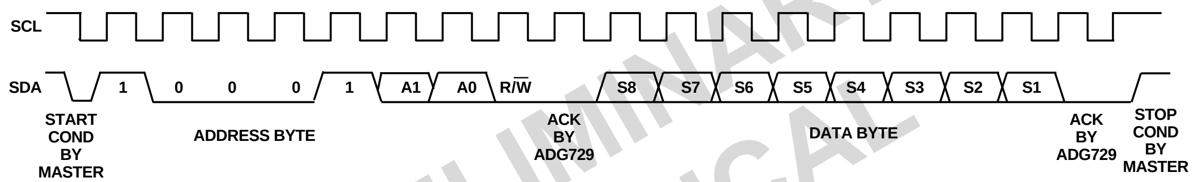


Figure 4. ADG729 Write Sequence

READ OPERATION

When reading data back from the ADG728/ADG729, the user must begin with an address byte and R/$\overline{W}$ bit, after which the matrix switch will Acknowledge that it is prepared to transmit data by pulling SDA low. The readback operation is a single byte which consists of the 8 data bits in the input register. The read operations for each part are shown in the figures below.

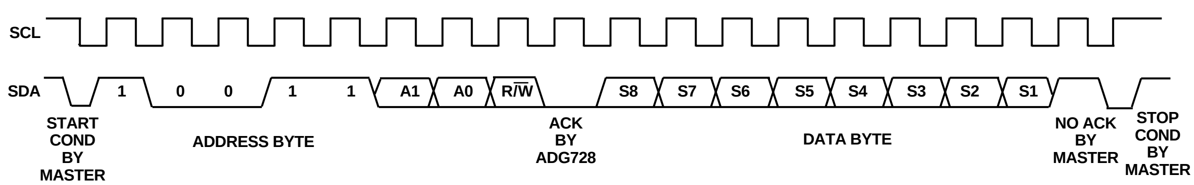


Figure 5. ADG728 Readback Sequence

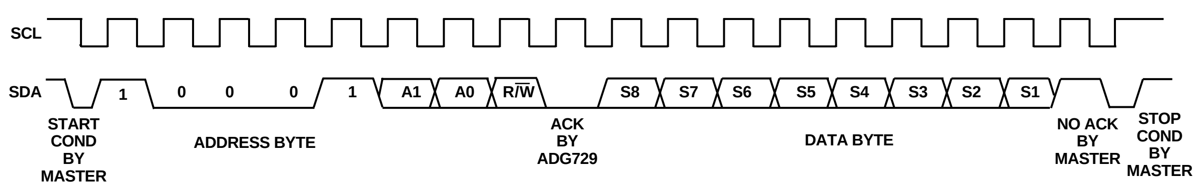
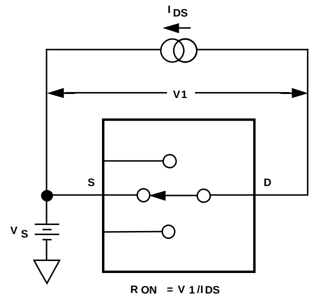
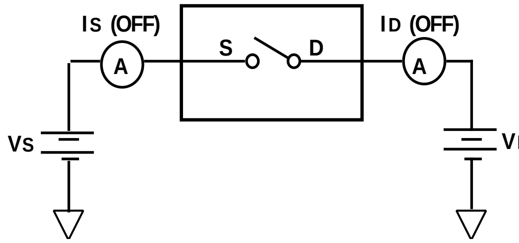


Figure 6. ADG729 Readback Sequence

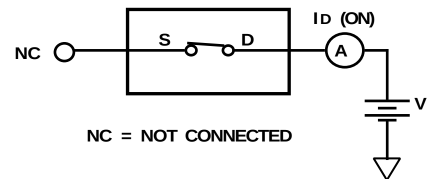
Test Circuits



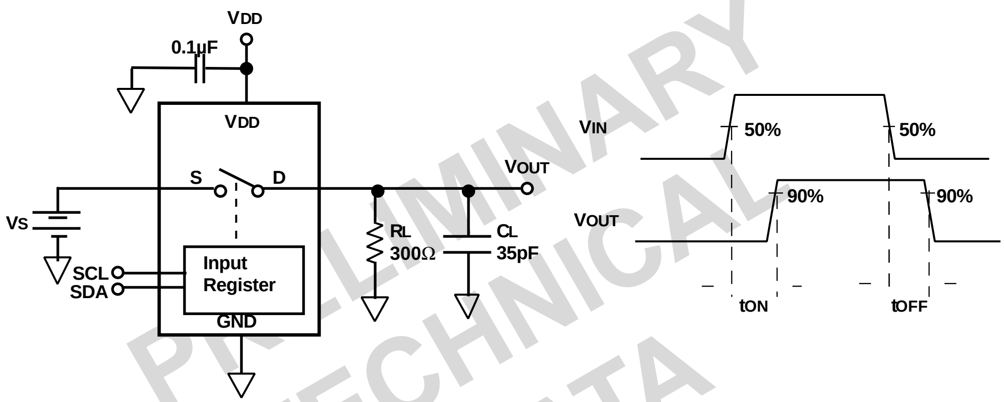
Test Circuit 1. On Resistance.



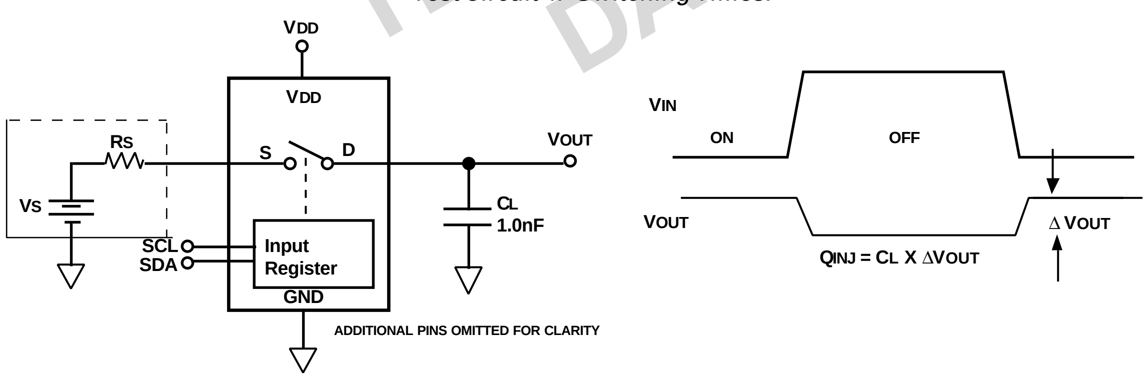
Test Circuit 2. Off Leakage.



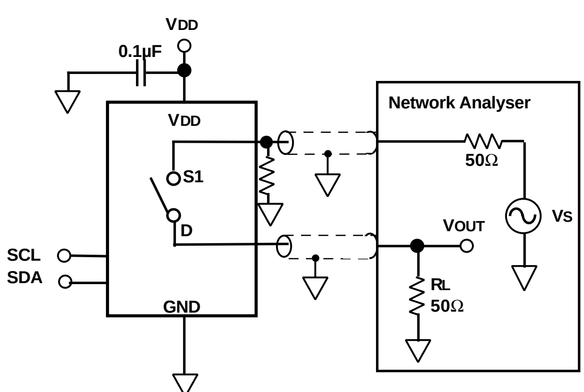
Test Circuit 3. On Leakage.



Test Circuit 4. Switching Times.

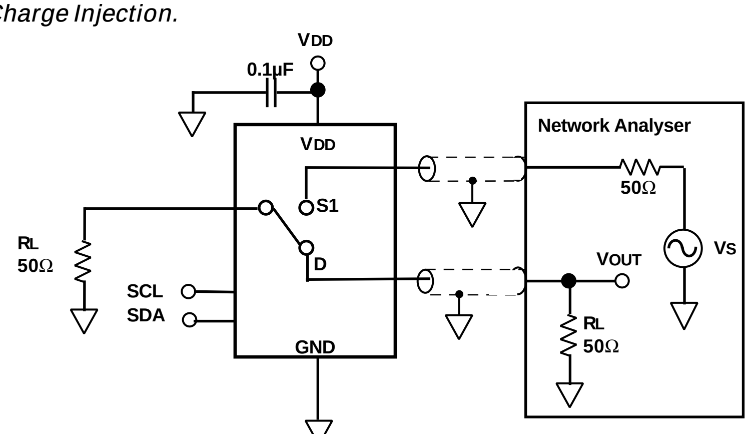


Test Circuit 5. Charge Injection.



OFF ISOLATION = 20 LOG V_{OUT}/V_S
INSERTION LOSS = 20 LOG $\frac{V_{OUT} \text{ with Switch}/V_S}{V_{OUT} \text{ without Switch}/V_S}$

Test Circuit 6. Off Isolation, Bandwidth.



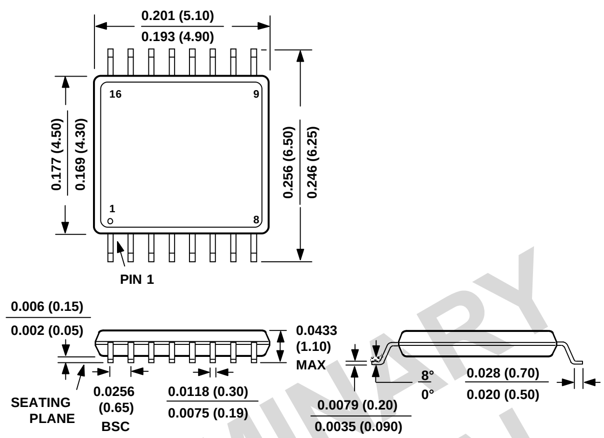
CROSSTALK = 20 LOG VOUT/Vs

Test Circuit 7. Crosstalk.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead TSSOP (RU-16)



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