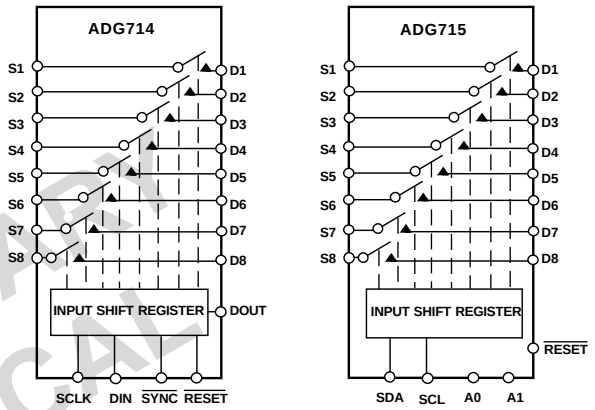
CMOS, Low Voltage, Serially Controlled, Octal SPST Switches

Preliminary Technical Data — ADG714/ADG715

FEATURES
ADG714 SPI/QSPI/Microwire Compatible Interface
ADG715 I^2C Compatible Interface
+2.7 V to +5.5 V Single Supply
+/-3 V Dual Supply
Low On Resistance (2.5 Ω typ)
Low On Resistance Flatness
Low Leakage
Octal SPST
Power on Reset
Fast Switching Times
TTL/CMOS compatible

APPLICATIONS
Data Acquisition Systems
Communication Systems
Relay replacement
Audio and Video Switching

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG714/ADG715 are CMOS, octal SPST (single pole, single throw) switches controlled via either a two or three wire serial interface. On resistance is closely matched between switches and very flat over the full signal range. Each switch conducts equally well in both directions and the input signal range extends to the supplies. Data is written to these devices in the form of 8-bits, each bit corresponding to one channel.

The ADG714 utilizes a three wire serial interface that is compatible with SPI™, QSPI™ and MICROWIRE™ and DSP interface standards. The output of the shift register DOUT enables a number of these parts to be daisy chained.

The ADG715 utilizes a two wire serial interface that is compatible with the I^2C™ interface standard. The ADG715 has four hard wired addresses, selectable from two external address pins (A0 and A1). This allows the 2 LSB's of the 7-bit slave address to be set by the user. A maximum of four of these devices maybe connected to the bus.

On power up of these devices, all switches are in the OFF condition, and the internal registers contain all zeros.

Low power consumption and operating supply range of +2.7V to +5.5V make this part ideal for many applications. These parts may also be supplied from a dual +/-3V supply. The ADG714 and ADG715 are available in a small 24-Lead TSSOP package.

PRODUCT HIGHLIGHTS

1. Three Wire Serial Interface.
2. Single/Dual Supply Operation. The ADG714 is fully specified and guaranteed with +3 V, +5 V and +/-3 V supply rails.
3. Low On Resistance, typically 2.5 Ω.
4. Low Leakage.
5. Power on Reset.
6. Small 24-Lead TSSOP package.

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ADG714/ADG715–PRELIMINARY SPECIFICATIONS[1]

(V_{DD} = +5 V ±10%, V_{SS} = 0 V, GND = 0 V unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On-Resistance (R_{ON})	2.5		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA;
	4	4.5	Ω max	Test Circuit 1;
On-Resistance Match Between		0.1	Ω typ	
Channels (ΔR_{ON})		0.4	Ω max	V_S = 0 V to V_{DD} , Is = 10 mA;
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.75		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA;
		1.2	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
	±0.1	±0.3	nA max	Test Circuit 2;
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
	±0.1	±0.3	nA max	Test Circuit 3;
Channel ON Leakage I_D (ON)	±0.01		nA typ	V_D = V_S = 1 V, or 4.5V;
	±0.1	±0.3	nA max	Test Circuit 4;
DIGITAL INPUTS(SCLK,DIN, $\overline{SYNC}$, A0, A1)				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
C_{IN}, Digital Input Capacitance[2]	3		pF typ	
DIGITAL OUTPUT ADG714 D_{OUT}[2]				
DOUT Output High Voltage		V_{DD}	max	
DOUT Output Low Voltage		0.4	max	
DIGITAL INPUTS (SCL, SDA)[2]				
Input High Voltage, V_{INH}		0.7V_{DD}	V min	
		V_{DD} +0.3	Vmax	
Input Low Voltage, V_{INL}		-0.3	V min	
		0.3V_{DD}	V max	
I_{IN}, Input Leakage Current	TBD		µA typ	V_{IN} = 0V to V_{DD}.
		±1	µA max	
V_{HYST}, Input Hysteresis	0.05V_{DD}		V min	
C_{IN}, Input Capacitance	3		pF typ	
LOGIC OUTPUT (SDA)[2]				
V_{OL}, Output Low Voltage		0.4	V max	I_{SINK} = 3 mA
		0.6	V max	I_{SINK} = 6 mA
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	30		ns typ	R_L = 300 Ω, C_L = 35 pF;
		TBD	ns max	V_S = 3 V, Test Circuit 5;
t_{OFF}	21		ns typ	R_L = 300 Ω, C_L = 35 pF;
		TBD	ns max	V_S = 3 V, Test Circuit 5;
Break-Before-Make Time Delay, t_D	15		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_S = 3.5 V, Test Circuit 6
Charge Injection	5		pC typ	V_S = 2 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 8;
Off Isolation	-60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz; Test Circuit 9;
Channel to Channel Crosstalk	-60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz; Test Circuit 10;
-3 dB Bandwidth	200		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 11;
C_S (OFF)	9		pF typ	
C_D (OFF)	TBD		pF typ	
C_D, C_S (ON)	TBD		pF typ	
POWER REQUIREMENTS				V_{DD} = +5.5 V
I_{DD}	10		µA typ	Digital Inputs = 0 V or 5.5 V
		TBD	µA max	

NOTES

[1]Temperature range is as follows: B Version: –40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS[1] (V_{DD} = 3V ± 10%, V_{SS} = 0 V, GND = 0 V.)

Parameter	B Version +25°C	B Version –40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On-Resistance (R_{ON})	4.5	5	Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA;
		8	Ω max	Test Circuit 1;
On-Resistance Match Between Channels (ΔR_{ON})	0.1		Ω typ	V_S = 0 V to V_{DD} , Is = 10 mA;
		0.4	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)		2.5	Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA;
LEAKAGE CURRENTS				V_{DD} = +3.3 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V;
	±0.1	±0.3	nA max	Test Circuit 2;
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	V_S = 1 V/3 V, V_D = 3 V/1 V;
	±0.1	±0.3	nA max	Test Circuit 3;
Channel ON Leakage I_D (ON)	±0.01		nA typ	V_S = V_D = +1 V or +3 V;
	±0.1	±0.3	nA max	Test Circuit 4;
DIGITAL INPUTS (SCLK, DIN, $\overline{SYNC}$, A0, A1)				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.4	V max	
Input Current, I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
C_{IN}, Digital Input Capacitance[2]	2		pF typ	
DIGITAL OUTPUT ADG714 D_{OUT}[2]				
DOUT Output High Voltage		V_{DD}	max	
DOUT Output Low Voltage		0.4	max	
DIGITAL INPUTS (SCL, SDA)[2]				
Input High Voltage, V_{INH}		0.7V_{DD}	V min	
		V_{DD} +0.3	Vmax	
Input Low Voltage, V_{INL}		-0.3	V min	
		0.3V_{DD}	V max	
I_{IN}, Input Leakage Current	TBD		µA typ	V_{IN} = 0V to V_{DD}.
		±1	µA max	
V_{HYST}, Input Hysteresis	0.05V_{DD}		V min	
C_{IN}, Input Capacitance	3		pF typ	
LOGIC OUTPUT (SDA)[2]				
V_{OL}, Output Low Voltage		0.4	V max	I_{SINK} = 3 mA
		0.6	V max	I_{SINK} = 6 mA
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	32		ns typ	R_L = 300 Ω, C_L = 35 pF;
		TBD	ns max	V_S = 2 V, Test Circuit 5;
t_{OFF}	23		ns typ	R_L = 300 Ω, C_L = 35 pF;
		TBD	ns max	V_S = 2 V, Test Circuit 5;
Break-Before-Make Time Delay, t_D	8		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_S = 2 V, Test Circuit 6
Charge Injection	5		pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF, Test Circuit 8;
Off Isolation	-60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz, Test Circuit 9;
Channel to Channel Crosstalk	-60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz, Test Circuit 10;
-3 dB Bandwidth	200		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 11;
C_S (OFF)	9		pF typ	
C_D (OFF)	TBD		pF typ	
C_D, C_S (ON)	TBD		pF typ	
POWER REQUIREMENTS				V_{DD} = +3.3 V
I_{DD}	10		µA typ	Digital Inputs = 0 V or 3.3 V
		TBD	µA max	

NOTES

[1]Temperature ranges are as follows: B Versions: –40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Dual Supply[1] (V_{DD} = +3 V ± 10%, V_{SS} = -3 V ± 10%, GND = 0 V.)

Parameter	B Version +25°C	B Version –40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On-Resistance (R_{ON})	5		Ω typ	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA;
			Ω max	Test Circuit 1;
On-Resistance Match Between Channels (ΔR_{ON})		TBD	Ω typ	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA;
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.75		Ω typ	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA;
		TBD	Ω max	
LEAKAGE CURRENTS				V_{DD} = +2.75 V, V_{SS} = -2.75 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	TBD
	±0.1	±0.3	nA max	Test Circuit 2;
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	TBD
	±0.1	±0.3	nA max	Test Circuit 3;
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	TBD
	±0.1	±0.3	nA max	Test Circuit 4;
DIGITAL INPUTS				
Input High Voltage, V_{INH}		TBD	V min	
Input Low Voltage, V_{INL}		0.4	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
C_{IN}, Digital Input Capacitance	2		pF typ	
DIGITAL OUTPUT ADG714 D_{OUT}				
DOUT Output High Voltage		V_{DD}	max	
DOUT Output Low Voltage		0.4	max	
DIGITAL INPUTS (SCL, SDA)[2]				
Input High Voltage, V_{INH}		0.7V_{DD}	V min	
		V_{DD} +0.3	Vmax	
Input Low Voltage, V_{INL}		-0.3	V min	
		0.3V_{DD}	V max	
I_{IN}, Input Leakage Current	TBD		µA typ	V_{IN} = 0V to V_{DD}.
		±1	µA max	
V_{HYST}, Input Hysteresis	0.05V_{DD}		V min	
C_{IN}, Input Capacitance	3		pF typ	
LOGIC OUTPUT (SDA)[2]				
V_{OL}, Output Low Voltage		0.4	V max	I_{SINK} = 3 mA
		0.6	V max	I_{SINK} = 6 mA
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	32		ns typ	R_L = 300 Ω, C_L = 35 pF;
		TBD	ns max	V_S = 1.5 V, Test Circuit 5;
t_{OFF}	23		ns typ	R_L = 300 Ω, C_L = 35 pF;
		TBD	ns max	V_S = 1.5 V, Test Circuit 5;
Break-Before-Make Time Delay, t_D	8		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_S = 1.5 V, Test Circuit 6
Charge Injection	5		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, Test Circuit 8;
Off Isolation	-60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz, Test Circuit 9;
Channel to Channel Crosstalk	-60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz, Test Circuit 10;
-3 dB Bandwidth	200		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 11;
C_S (OFF)	9		pF typ	
C_D (OFF)	TBD		pF typ	
C_D, C_S (ON)	TBD		pF typ	
POWER REQUIREMENTS				V_{DD} = +3.3 V, V_{SS} = -3.3 V
I_{DD}	10		µA typ	Digital Inputs = 0 V or +3.3 V
		TBD	µA max	
I_{SS}	10		µA typ	
		TBD	µA max	

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

ADG714 TIMING CHARACTERISTICS[1,2] (V_{DD} = +2.5 V to +5.5 V . All specifications –40°C to +85°C unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX}	Units	Conditions/Comments
t_1	33	ns min	SCLK Cycle time
t_2	13	ns min	SCLK High Time
t_3	13	ns min	SCLK Low Time
t_4	0	ns min	$\overline{SYNC}$ to SCLK active edge setup time
t_5	5	ns min	Data Setup Time
t_6	4.5	ns min	Data Hold Time
t_7	0	ns min	SCLK Falling edge to $\overline{SYNC}$ Rising edge
t_8	33	ns min	Minimum $\overline{SYNC}$ high time
t_9	20	ns min	SCLK rising edge to DOUT valid

NOTES
[1]See Figure 1.
[2]All input signals are specified with tr =tf = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

Specifications subject to change without notice.

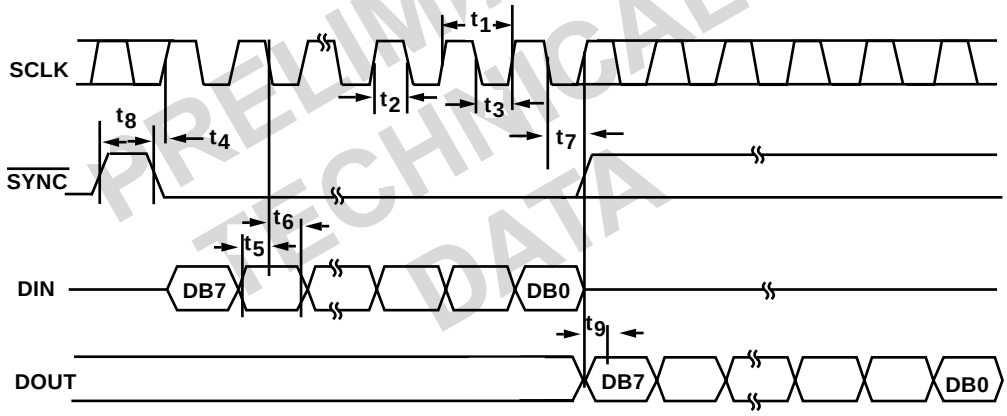


Figure 1. 3-Wire Serial Interface Timing Diagram.

ADG715 TIMING CHARACTERISTICS[1] (V_{DD} = +2.5 V to +5.5 V . All specifications –40°C to +85°Cunless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX}	Units	Conditions/Comments
FSCL	400	kHz max	SCL Clock Frequency
t_1	2.5	µs min	SCL Cycle Time
t_2	0.6	µs min	t_{HIGH}, SCL High Time
t_3	1.3	µs min	t_{LOW}, SCL Low Time
t_4	0.6	µs min	$t_{HD, STA}$, Start/Repeated Start Condition Hold Time
t_5	100	ns min	$t_{SU, DAT}$, Data Setup Time
t_6[2]	0.9	µs max	$t_{HD, DAT}$, Data Hold Time
	0	µs min	
t_7	0.6	µs min	$t_{SU, STA}$, Setup Time for Repeated Start
t_8	0.6	µs min	$t_{SU, STO}$, Stop Condition Setup Time
t_9	1.3	µs min	t_{BUF}, Bus Free Time Between a STOP Condition and a Start Condition
t_{10}	300	ns max	t_R, Rise Time of both SCL and SDA when receiving
	20 + $0.1C_b$[3]	ns min	
t_{11}	250	ns max	t_F, Fall Time of SDA when receiving
t_{11}	300	ns max	t_F, Fall Time of both SCL and SDA when transmitting
	20 + $0.1C_b$[3]	ns min	
C_b	400	pF max	Capacitive Load for Each Bus Line
t_{SP}[4]	50	ns max	Pulse width of spike suppressed

NOTES
[1]See Figure 2.
[2]A master device must provide a hold time of at least 300ns for the SDA signal (referred to the V_{IH} min of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
[3]C_b is the total capacitance of one bus line in pF. t_R and t_F measured between $0.3V_{DD}$ and $0.7V_{DD}$.
[4]Input filtering on both the SCL and SDA inputs suppress noise spikes which are less than 50ns.

Specifications subject to change without notice.

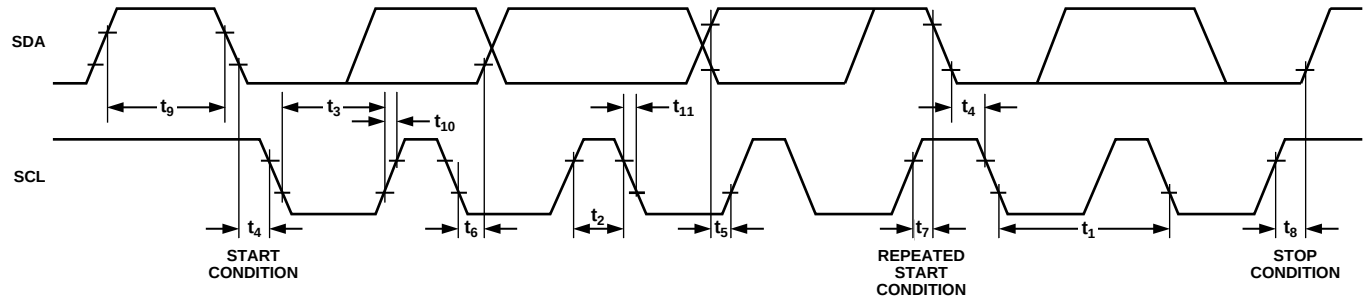


Figure 2. 2-Wire Serial Interface Timing Diagram.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS}	+7 V
V_{DD} to GND	–0.3 V to +7 V
V_{SS} to GND	+0.3 V to -7 V
Analog Inputs[2]	V_{SS} - 0.3 V to V_{DD} +0.3 Vor 30 mA, Whichever Occurs First
Digital Inputs[2]	-0.3V to V_{DD} +0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D	100mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D	30mA
Operating Temperature Range	
Industrial (B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
Package, Power Dissipation	mW
θ_{JA} Thermal Impedance	128°C/W
θ_{JC} Thermal Impedance	42°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C
ESD	2kV

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

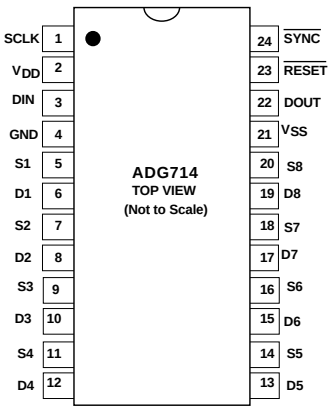
ORDERING GUIDE

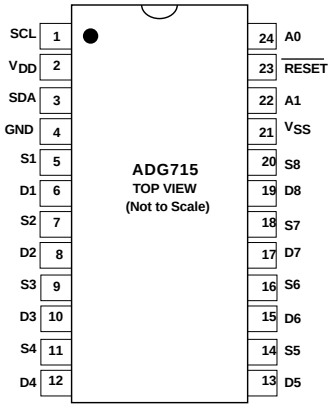
Model	Temperature Range	Interface	Package Description	Package Option
ADG714BRU	-40 °C to +85 °C	SPI/QSPI/Microwire	TSSOP	RU-24
ADG715BRU	-40 °C to +85 °C	I^2C Compatible	TSSOP	RU-24

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG714/ADG715 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION
24 lead TSSOP





ADG714 PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Description
1	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. These devices can accomodate serial input rates of up to 30MHz.
2	V_{DD}	Positive Analog supply voltage.
3	DIN	Serial Data Input. Data is clocked into the 8-bit input register on the falling edge of the serial clock input.
4	GND	Ground reference
5,7,9,11, 14,16,18,20	SX	Source. May be an input or output
6,8,10,12,13 15,17,19	DX	Drain. May be an input or output.
21	V_{SS}	Negative analog supply voltage, for single supply operation this should be tied to GND.
22	DOUT	Serial Data Output. This allows a number a parts to be daisy chained. Data is clocked out of the input shift register on the rising edge of SCLK.
23	$\overline{\text{RESET}}$	Active low control input that clears the input register and turns all switches to the OFF condition.
24	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and the input shift register is enabled. Data is transferred on the falling edges of the following 8 clocks. Taking $\overline{\text{SYNC}}$ high, updates the switches.

ADG715 PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Description
1	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into the 16-bit input shift register. Clock rates of up to 400kbit/s can be accommodated with this 2-wire serial interface.
2	V_{DD}	Positive Analog supply voltage.
3	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into the 8-bit input shift register during the write cycle and used to read back 1 byte of data during the read cyle. It is a bidirectional open-drain data line which should be pulled to the supply with an external pull-up resistor.
4	GND	Ground reference
5,7,9,11, 14,16,18,20	SX	Source. May be an input or output
6,8,10,12,13 15,17,19	DX	Drain. May be an input or output.
21	V_{SS}	Negative analog supply voltage, for single supply operation this should be tied to GND.
22	A1	Address Input. Sets the 2nd Least Significant bit of the 7 bit slave address.
23	$\overline{\text{RESET}}$	Active low control input that clears the input register and turns all switches to the OFF condition.
24	A0	Address Input. Sets the Least Significant bit of the 7 bit slave address.

TERMINOLOGY

R_{ON}	Ohmic resistance between D and S.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	"OFF" switch source capacitance. Measured with reference to ground.
C_D (OFF)	"OFF" switch drain capacitance. Measured with reference to ground.
C_D,C_S(ON)	"ON" switch capacitance. Measured with reference to ground.
C_{IN}	Digital input capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on. See test circuit 4.
t_{OFF}	Delay between applying the digital control input and the output switching off.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Bandwidth	The frequency at which the output is attenuated by -3dBs.
On Response	The Frequency response of the "ON" switch.
On Loss	The voltage drop across the "ON" switch seen on the On Response vs. Frequency plot as how many dBs the signal is away from 0dB.
V_{INL}	Maximum input voltage for logic "0".
V_{INH}	Minimum input voltage for logic "1".
I_{INL}(I_{INH})	Input current of the digital input.
I_{DD}	Positive supply current.

GENERAL DESCRIPTION

The ADG714 and ADG715 are serially controlled, octal SPST switches, controlled by either a 2 or 3 wire interface. Each bit of the 8 bit serial word corresponds to one switch of the part. A logic '1' in the particular bit position turns on the switch, while a logic '0' turns the switch off. Because each switch is independently controlled by an individual bit, this provides the option of having any, all or none of the switches ON.

POWER ON RESET

On power up of the device, all switches will be in the OFF condition and the internal shift register is filled with zeros and will remain so until a valid write takes place.

SERIAL INTERFACE

3-WIRE SERIAL INTERFACE

The ADG714 has a three wire serial interface ($\overline{SYNC}$, SCLK, and DIN), which is compatible with SPI, QSPI, MICROWIRE interface standards and most DSP's. Figure 1 shows the timing diagram of a typical write sequence.

Data is written to the 8-bit shift register via DIN under the control of the $\overline{SYNC}$ and SCLK signals. Data may be written to the shift register in more or less than 8 bits. In each case the shift register retains the last eight bits that were written.

When $\overline{SYNC}$ goes low, the input shift register is enabled. Data from DIN is clocked into the shift register on the falling edge of SCLK. Each bit of the eight bit word corresponds to one of the eight switches. Figure 2 shows the contents of the input shift register. Data appears on the DOUT pin on the rising edge of SCLK suitable for daisy chaining, delayed of course by eight bits. When all eight bits have been written into the shift register, the $\overline{SYNC}$ line is brought high again. The switches are updated with the new configuration and the input shift register is disabled. With $\overline{SYNC}$ held high, any further data or noise on the DIN line will have no effect on the shift register.

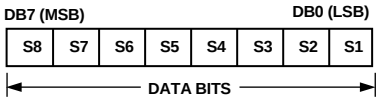


Figure 3. Input Shift Register Contents

SERIAL INTERFACE

2-WIRE SERIAL BUS

The ADG715 is controlled via an I^2C compatible serial bus. This device is connected to the bus as a slave device (no clock is generated by the switch)

The ADG715 has a 7-bit slave addresses. The five MSBs are 10010 and the two LSBs are determined by the state of the A0 and A1 pins.

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition which is when a high to low transition on the SDA line occurs while SCL is high. The following byte is the address byte which consists of the 7-bit slave address followed by a R/W bit (this bit determines whether data will be read from or written to the slave device).

The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the Acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/W bit is high, the master will read from the slave device. However, if the R/W bit is low, the master will write to the slave device.

2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an Acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.

3) When all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low to high transition on the SDA line while SCL is high. In Write mode, the master will pull the SDA line high during the 10th clock pulse to establish a STOP condition. In Read mode, the master will issue a No Acknowledge for the 9th clock pulse (i.e. the SDA line remains high). The master will then bring the SDA line low before the 10th clock pulse and then high during the 10th clock pulse to establish a STOP condition.

See Figure 4 for a graphical explanation of the serial interface.

A repeated write function gives the user flexibility to update the matrix switch a number of times after addressing the part only once. During the write cycle, each data byte will update the configuration of the switches. For example, after the matrix switch has acknowledged its address byte, and receives one data byte, the switches will update after the data byte, if another data byte is written to the matrix switch while it is still the addressed slave device, this data byte will also cause an switch configuration update. Repeat read of the matrix switch is also allowed.

INPUT SHIFT REGISTER

The input shift register is 8-bits wide. Figure 3 illustrates the contents of the input shift register. Data is loaded into the device as an 8-bit word under the control of a serial clock input, SCL. The timing diagram for this operation is shown in Figure 1. The 8-bit word consists of 8 data bits each controlling one switch. MSB (Bit 7) is loaded first.

WRITE OPERATION

When writing to the ADG715, the user must begin with an address byte and R/$\overline{W}$ bit, after which the switch will Acknowledge that it is prepared to receive data by pulling SDA low. This address byte is followed by the 8-bit word. The write operations for the matrix switch is shown in the figure below.

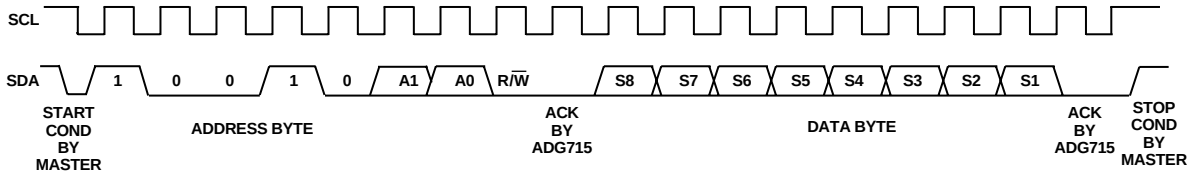


Figure 4. ADG715 Write Sequence

READ OPERATION

When reading data back from the ADG715, the user must begin with an address byte and R/$\overline{W}$ bit, after which the matrix switch will Acknowledge that it is prepared to transmit data by pulling SDA low. The readback operation is a single byte which consists of the 8 data bits in the input register. The read operation for the part is shown in the figure below.

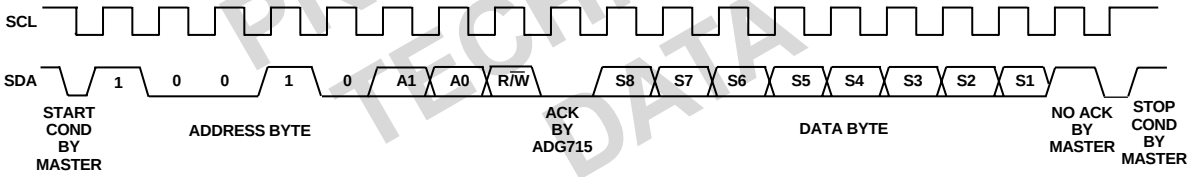


Figure 5. ADG715 Readback Sequence

TEST CIRCUITS

TBD

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24 Lead TSSOP
(RU-24)