Dual Frequency Synthesizer

Preliminary Technical Data ADF4210/ADF4211/ADF4212/ADF4213

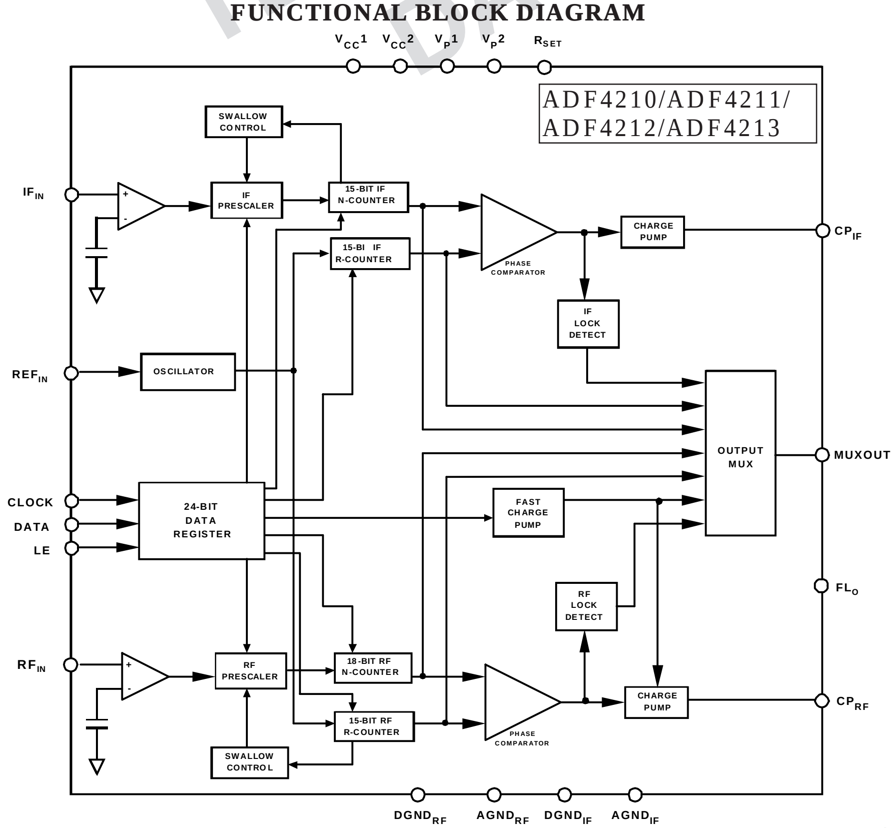
FEATURES
ADF4210: 550MHz/1.2GHz
ADF4211: 550MHz/2.0GHz
ADF4212: 550MHz/3.0GHz
ADF4213: 1.0GHz/2.5GHz
+2.7 V to +5.5 V Power Supply
Programmable Dual Modulus Prescaler
Programmable Charge Pump Currents
3-Wire Serial Interface
Digital Lock Detect
Power Down Mode

APPLICATIONS
Portable Wireless Communications (PCS/PCN,
Cordless) Cordless and Cellular Tele-
phone Systems Wireless Local Area Net-
works (WLANs)

GENERAL DESCRIPTION

The ADF4210/ADF4211/ADF4212/ADF4213 is a dual frequency synthesizer which can be used to implement local oscillators in the up-conversion and down-conversion sections of wireless receivers and transmitters. They can provide the LO for both the RF and IF sections. They consist of a low-noise digital PFD (Phase Frequency Detector), a precision charge pump, a programmable reference divider, programmable A and B counters and a dual-modulus prescaler (P/P+1). The A (6-bit) and B (12-bit) counters, in conjunction with the dual modulus prescaler (P/P+1), implement an N divider (N= BP+A). In addition, the 15-bit reference counter (R Counter), allows selectable REFIN frequencies at the PFD input. A complete PLL (Phase-Locked Loop) can be implemented if the synthesizers are used with an external loop filter and VCO's (Voltage Controlled Oscillators)Control of all the on-chip registers is via a simple 3-wire interface. The devices operate with a 3V (± 10%) or 5V(± 10%) power supply and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM



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ADF4210/11/12/13—SPECIFICATIONS[1]

(V_{DD} = +3 V ± 10%, +5 V ± 10%; V_P = V_{DD}, +5 V ± 10%; GND = 0 V; R_{SET} = 4.7kΩ; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	B Version	BChips	Units	Test Conditions/Comments
RF CHARACTERISTICS				
RF Input Frequency ($RF_{IN}A$, $RF_{IN}B$)				
ADF4210	25/550	25/550	MHz min/max	
ADF4211	0.1/1.2	0.1/1.2	GHz min/max	
ADF4212	0.1/3.0	0.1/3.0	GHz min/max	
ADF4213	0.1/2.5	0.1/2.5	GHz min/max	
IF Input Frequency ($IF_{IN}A$, $IF_{IN}B$)				
ADF4210	25/550	25/550	MHz min/max	
ADF4211	25/550	25/550	GHz min/max	
ADF4212	25/550	25/550	GHz min/max	
ADF4213	0.1/1.0	0.1/1.0	GHz min/max	
Reference Input Frequency	5/40	5/40	MHz min/max	
Phase Detector Frequency	10	10	MHz max	
RF Input Sensitivity	-15/0	-15/0	dBm min/max	3V Power Supply
	-10/0	-10/0	dBm min/max	5V Power Supply
Reference Input Sensitivity	-5	-5	dBm min	
CHARGE PUMP				
I_{CP} sink/source				
High Value	5	5	mA typ	See Table 11
Low Value	625	625	µA typ	
I_{CP} Three State Current	1	1	nA max	
Sink and Source Current Matching	2	2	% typ	0.5V < V_{CP} < V_P - 0.5
I_{CP} vs. V_{CP}	2	2	% typ	0.5V < V_{CP} < V_P - 0.5
I_{CP} vs. Temperature	2	2	% typ	V_{CP} = $V_P/2$
LOGIC INPUTS				
V_{INH}, Input High Voltage	0.8*V_{DD}	0.8*V_{DD}	V min	
V_{INL}, Input Low Voltage	0.2*V_{DD}	0.2*V_{DD}	V max	
I_{INH}/I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
Oscillator Input Current	±100	±100	µA max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	V_{CC} - 0.4	V_{CC} - 0.4	V min	I_{OH} = 1mA
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{OL} = 1mA
POWER SUPPLIES				
AV_{DD}	2.7/5.5	2.7/5.5	V min/V max	
DV_{DD}	AV_{DD}	AV_{DD}		
V_P1,V_P2	AV_{DD}/5.5	AV_{DD}/5.5	V min/V max	
I_{DD}				
(RF + IF)				
ADF4210	3.0	3.0	mA max	
ADF4211	4.0	4.0	mA max	
ADF4212	4.0	4.0	mA max	
ADF4213	5.0	5.0	mA max	
RF Only				
ADF4210	2.0	2.0	mA max	
ADF4211	3.0	3.0	mA max	
ADF4212	4.0	4.0	mA max	
ADF4213	4.0	4.0	mA max	
IF Only				
ADF4213	1.0	1.0	mA max	
Low Power Sleep Mode	1	1	µA typ	

Parameter	B Version	BChips	Units	Test Conditions/Comments
NOISE CHARACTERISTICS				
Phase Noise Floor	-173	-173	dBc/Hz typ	@ 25kHz PFD Frequency
	-165	-165	dBc/Hz typ	@ 200kHz PFD Frequency
Phase Noise Performance[2]				@ VCO Output
ADF4210[3]	-96	-96	dBc/Hz typ	
ADF4211[4]	-92	-92	dBc/Hz typ	
ADF4211[5]	-82	-82	dBc/Hz typ	
ADF4212[6]	-85	-85	dBc/Hz typ	
ADF4212[7]	-66	-66	dBc/Hz typ	
ADF4213[7]	-66	-66	dBc/Hz typ	
ADF4213[8]	-85	-85	dBc/Hz typ	
Spurious Signals				Measured at offset of $f_{PFD}/2f_{PFD}$
ADF4210[3]	tbd/tbd	tbd/tbd	dB typ	
ADF4211[4]	tbd/tbd	tbd/tbd	dB typ	
ADF4211[5]	tbd/tbd	tbd/tbd	dB typ	
ADF4212[6]	tbd/tbd	tbd/tbd	dB typ	
ADF4212[7]	tbd/tbd	tbd/tbd	dB typ	
ADF4212[8]	tbd/tbd	tbd/tbd	dB typ	
ADF4213[8]	tbd/tbd	tbd/tbd	dB typ	
ADF4213[8]	tbd/tbd	tbd/tbd	dB typ	

NOTES

1 Operating temperature range is as follows: B Version: –40°C to +85°C.

2 The phase noise is measured with the EVAL-ADF421XEB Evaluation Board and the HP8562E Spectrum Analyzer. The spectrum analyzer provides the REFIN for the synthesizer. (f_{REFOUT} = 10MHz@ 0dBm)

3. f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{RF} = 540MHz; N = 2700; Loop B/W = 20kHz

4. f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{RF} = 900MHz; N = 4500; Loop B/W = 12kHz

5. f_{REFIN} = 10 MHz; f_{PFD} = 30kHz; Offset frequency = 1 kHz; f_{RF} = 836MHz; N = 27867; Loop B/W = 3kHz

6. f_{REFIN} = 10 MHz; f_{PFD} = 200kHz; Offset frequency = 1 kHz; f_{RF} = 1880MHz; N = 9400; Loop B/W = 20kHz

7. f_{REFIN} = 10 MHz; f_{PFD} = 10kHz; Offset frequency = 250Hz; f_{RF} = 1880MHz; N = 188000; Loop B/W = 1kHz

8. f_{REFIN} = 10 MHz; f_{PFD} = 200kHz; Offset frequency = 1 kHz; f_{RF} = 1960MHz; N = 9800; Loop B/W = 20kHz

Specifications subject to change without notice.

CHIP LAYOUT

TIMING CHARACTERISTICS

(V_{DD} = +5 V 10%, +3 V ± 10%; GND = 0 V, unless otherwise noted)

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Units	Test Conditions/Comments
t_1	50	ns min	DATA to CLOCK Set Up Time
t_2	10	ns min	DATA to CLOCK Hold Time
t_3	50	ns min	CLOCK High Duration
t_4	50	ns min	CLOCK Low Duration
t_5	50	ns min	CLOCK to LE Set Up Time
t_6	50	ns min	LE Pulse Width

NOTE
Guaranteed by Design but not Production Tested.

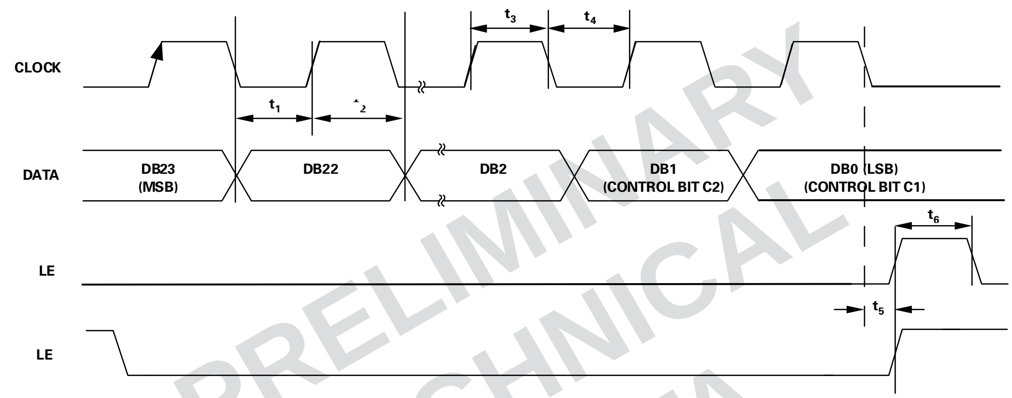


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . –0.3 V to +7 V
V_P to GND . . . . –0.3 V to +7 V
V_P to V_{DD} . . . . –0.3 V to +3.5 V
Digital I/O Voltage to GND . . . . –0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND . . . . –0.3 V to V_P + 0.3 V
Operating Temperature Range
Industrial (B Version) . . . . –40°C to +85°C
Storage Temperature Range . . . . –65°C to +150°C
Maximum Junction Temperature . . . . +150°C
TSSOP θ_{JA} Thermal Impedance . . . . TBD°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . +215°C
Infrared (15 sec) . . . . +220°C

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This device is a high-performance RF integrated circuit with an ESD rating of < 2kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADF4210BRU	–40°C to +85°C	RU-16
ADF4210BCHIPS	–40°C to +85°C	
ADF4211BRU	–40°C to +85°C	RU-16
ADF4211BRCHIPS	–40°C to +85°C	
ADF4212BRU	–40°C to +85°C	RU-16
ADF4212BCHIPS	–40°C to +85°C	
ADF4213BRU	–40°C to +85°C	RU-16
ADF4213BRCHIPS	–40°C to +85°C	

*RU = Thin Shrink Small Outline Package (TSSOP).

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 2. ADF4210 Phase Noise

Figure 3. ADF4210 Reference Spurs

Figure 4. ADF4211 Phase Noise (GSM902)

Figure 5. ADF4211 Reference Spurs (GSM902)

Figure 6. ADF4211 Phase Noise (CDMA836)

Figure 7. ADF4211 Reference Spurs (CDMA836)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Figure 8. ADF4212 Phase Noise (GSM1880)

Figure 9. ADF4212 Reference Spurs (GSM1880)

Figure 10. ADF4212 Phase Noise (CDMA1880)

Figure 11. ADF4212 Reference Spurs (CDMA1880)

Figure 12. ADF4212 Phase Noise (WCDMA1960)

Figure 13. ADF4212 Reference Spurs (WCDMA1960)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Figure 14. ADF4210 Phase Noise Floor vs PFD Frequency

Figure 15. ADF4211 Phase Noise Floor vs PFD Frequency

Figure 16. ADF4212 Phase Noise Floor vs PFD Frequency

Figure 17.ADF4213 Phase Noise Floor vs PFD Frequency

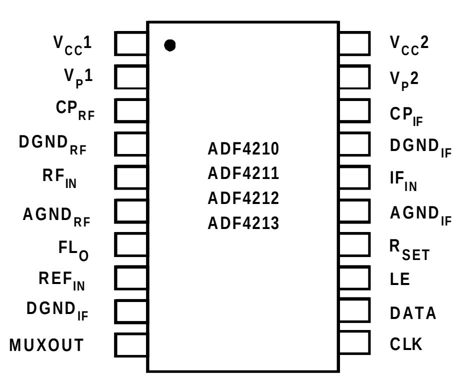
Figure 18.

Figure 19.

PIN DESCRIPTION

Mnemonic	Function
Vcc1	Positive power supply for the RF section. A 0.1uF capacitor should be connected between this pin and GND. Vcc1 has a value +5V 10% or 3V 10%. Vcc1 must have the same potential as Vcc2.
Vp1	RF Charge Pump Power Supply. This should be greater than or equal to $V_{cc}1$.
CP_{RF}	RF Charge Pump Output. This is normally connected to a loop filter which drives the input to an external VCO.
$DGND_{RF}$	Digital Ground for the RF digital circuitry.
RF_{IN}	Input to the RF Prescaler. This small signal input is normally taken from the VCO.
$AGND_{RF}$	Analog Ground for the RF analog circuitry.
FL_o	Multiplexed output of RF/IF programmable or reference dividers, RF/IF fastlock mode. CMOS output.
REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and an equivalent input resistance of 100kΩ. This input can be driven from a TTL or CMOS crystal oscillator.
$DGND_{IF}$	Digital Ground for the IF digital,interface and control circuitry
MUXOUT	This multiplexer output allows either the IF/RF Lock Detect, the scaled RF, scaled IF or the scaled Reference Frequency to be accessed externally.
CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 22-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.
R_{SET}	Connecting a resistor to this pin sets the maximum charge pump output current. With R_{SET} = 4.7kΩ, I_{CPmax} = 5mA.
$AGND_{IF}$	Analog Ground for the IF analog circuitry.
IF_{IN}	Input to the RF Prescaler. This small signal input is normally taken from the VCO.
$DGND_{IF}$	Digital Ground for the IF digital,interface and control circuitry
CP_{IF}	IF Charge Pump Output. This is normally connected to a loop filter which drives the input to an external VCO.
Vp2	IF Charge Pump Power Supply. This should be greater than or equal to $V_{cc}2$.
Vcc2	Positive power supply for the IF section. A 0.1uF capacitor should be connected between this pin and GND. Vcc1 has a value +5V ±10% or 3V ±10%. Vcc1 must have the same potential as Vcc1.

PIN CONFIGURATION



CIRCUIT DESCRIPTION

INPUT SHIFT REGISTER

The functional block diagram for the ADF4210 family is shown on page 1. The main blocks include a 22-bit input shift register, two 15-bit R counters and two N counters (15 bit resloution for the IF and 18 bit resolution for the RF). Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two lsb's DB1, DB0 as shown in the timing diagram of Figure 1. The truth table for these bits is shown in Table 1.

PROGRAMMABLE REFERENCE (R) COUNTER

If control bits C2, C1 are 0,0 then the data is transferred from the input shift register to the 14 Bit IFR counter. If the control bits 1,0 then the data is transferred to the 14 Bit RFR counter Tables 2a and 2b shows the input shift register data format for the IF and RF R conters and Table 3 shows the divide ratios possible.

Table 1. C2, C1 Truth Table

Control Bits C2	C1	Data Latch
0	0	IF R Counter
0	1	IF N Counter (A and B)
1	0	RF R Counter
1	1	RF N Counter

Table 2a. IF R Counter

IF CP Current Setting			IF F_O	IF Lock Detect	3-State CP_{IF}	IF PD Polarity		14-Bit Reference Counter														Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
IF CPI 2	IF CPI 1	IF CPI 0	P4	P3	P2	P1		R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2(0)	C1(0)

Table 2b. RF R Counter

RF CP Current Setting			RF F_O	RF Lock Detect	3-State CP_{RF}	RF PD Polarity		14-Bit Reference Counter														Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RF CPI 2	RF CPI 1	RF CPI 0	P12	P11	P10	P9	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2(1)	C1(0)

Table 3. IF/RF R Counter Divide Ratios

Divide Ratio	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	0	0	0	0	1	0
*	*	*	*	*	*	*	*	*	*	*	*	*	*	
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
16382	1	1	1	1	1	1	1	1	1	1	1	1	1	0
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES
1. Divide ratio: 1 to 16383

PROGRAMMABLE N COUNTER

If control bits C2, C1 are 0, 1 then the data in the input register is used to program the IFN (A + B) counter. If the control bits 1,1 then the data is transferred to the RFN counter. The N counter consists of a 6-bit swallow counter (A counter) and 12-bit programmable counter (B counter). Table 4 shows the input register data format for programming the N counters. Table 5 and 6 show the truth table for the RF and IF A counters. Table 7 is the truth table for the RF/IF B counter.

Pulse Swallow Function

The A and B counters, in conjunction with the dual modulus prescaler make it possible to generate output frequencies which are spaced only by the Reference Frequency divided by R . The equation for the VCO frequency is as follows:

$$f_{VCO} = [(P \times B) + A] \times f_{REFIN}/R$$

f_{VCO}: Ouput Frequency of external voltage controlled oscillator (VCO).

P: Preset modulus of dual modulus prescaler.

B: Preset Divide Ratio of binary 12-bit counter (3

A: Preset Divide Ratio of binary 6-bit swallow counter.

f_{REFIN}: Ouput frequency of the external reference frequency oscillator.

R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16383).

Table 4a. IF N Counter

IF CP Gain	IF Power Down	IF Prescaler	IF Prescaler	12-Bit B Counter												6-Bit A Counter						Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	P8	P7	P6	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2(0)	C1(1)

Table 4b. RF N Counter

RF CP Gain	RF Power Down	RF Prescaler	RF Prescaler	12-Bit B Counter												6-Bit A Counter						Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	P16	P15	P14	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2(1)	C1(1)

Table 5. RF Swallow Counter (A Counter)

Divide Ratio	A6	A5	A4	A3	A2	A1
0	0	0	0	0	0	0
1	0	0	0	0	0	1
*	*	*	*	*	*	*
127	1	1	1	1	1	1

NOTES
1. Divide ratio: 0 to 127.
2. B is greater than or equal to A

Table 6. IF Swallow Counter (A Counter)

Divide Ratio	A6	A5	A4	A3	A2	A1
0	X	X	0	0	0	0
1	X	X	0	0	0	1
*	*	*	*	*	*	*
15	X	X	1	1	1	1

NOTES
1. Divide ratio: 0 to 15
2. B is greater than or equal to A
3. X equals dont care condition.

Table 7. B Counter Divide Ratio

Divide Ratio	N17	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6
3	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	1	0	0
*	*	*	*	*	*	*	*	*	*	*	*	*
*	*	*	*	*	*	*	*	*	*	*	*	*
4095	1	1	1	1	1	1	1	1	1	1	1	1

NOTES
1.Divide ratios less than 3 are prohibited.
2.Divide ratio: 3 to 4095.
3.B is must be greater than or equal to A.

IF Power Down

If P8 has been set to a "1" and P2 has been set to “0” (normal operation), then a synchronous power down is conducted in the IF section. The device will automatically put the IF charge pump into 3-state and then complete the IF power down. See table 8.

If P8 has been set to a "1" and P2 has been set to “1” (normal operation), then an asynchronous power down is conducted in the IF section. The IF stage of the device will go into powerdown on the rising edge of LE which latches the "1" to the IF powerdown bit. See table 8.

Activation of either synchronous or asynchronous powerdown forces the IF loop's R and N dividers to their load state conditions and the IF_{IN} section is debiased to a high impedance state

The REF oscillator circuit is only disabled if both the IF and RF Powerdowns are set.

The IF section of the devicewill return to normal powered-up operation immediately on LE latching a "0" to the IF powerdown bit (P8). See table 8.

RF Power Down

If P16 has been set to a "1" and P10 has been set to “0” (normal operation), then a synchronous power down is conducted in the RF section. The device will automatically put the RF charge pump into 3-state and then complete the RF power down. See table 8.

If P16 has been set to a "1" and P10 has been set to “1” (normal operation), then an asynchronous power down is conducted in the RF section. The RF stage of the device will go into powerdown on the rising edge of LE which latches the "1" to the RF powerdown bit. See table 8.

Activation of either synchronous or asynchronous powerdown forces the RF loop's R and N dividers to their load state conditions and the RF_{IN} section is debiased to a high impedance state

The REF oscillator circuit is only disabled if both the IF and RF Powerdowns are set.

The RF section of the devicewill return to normal powered-up operation immediately on LE latching a "0" to the RF powerdown bit (P16). See table 8.

Table 8. Power-Down Modes

P10 P2	P16 P8	RF Mode IF Mode
X	0	Normal Operation
0	1	Synchronous Power-Down
1	1	Asynchronous Power-Down

MUXOUT Control

The on-chip multiplexer is controlled by P12, P11, P4, P3 on the ADF4210 Family.

Table 9. MUXOUT Control

P12	P11	P4	P3	Muxout
0	0	0	0	Logic low state
0	0	0	1	IF Analog Lock Detect
0	0	1	0	IF Reference Divider Output
0	0	1	1	IF N Divider Output
0	1	0	0	RF Analog Lock Detect
0	1	0	1	RF/IF Analog Lock Detect
0	1	1	0	IF Digital Lock Detect
0	1	1	1	Logic high state
1	0	0	0	RF Reference Divider
1	0	0	1	RF N Divider
1	0	1	0	3-State Output
1	0	1	1	IF Counter Reset
1	1	0	0	RF Digital Lock Detect
1	1	0	1	RF/IF Digital Lock Detect
1	1	1	0	RF Counter Reset
1	1	1	1	IF and RF Counter Reset

IF Phase Detector Polarity

P1 sets the IF Phase Detector Polarity. When the IF VCO characteristics are positive this should be set to “1”. When they are negative it should be set to “0”.

RF Phase Detector Polarity

P9 sets the IF Phase Detector Polarity. When the RF VCO characteristics are positive this should be set to “1”. When they are negative it should be set to “0”.

IF Charge Pump 3-State

P2 puts the IF charge pump into 3-state mode when programmed to a “1”. It should be set to “0” for normal operation.

RF Charge Pump 3-State

P10 puts the RF charge pump into 3-state mode when programmed to a “1”. It should be set to “0” for normal operation.

IF Prescaler Value

P7 and P6 in the IF A,B Counter Latch set the IF prescaler values. See Table 10.

RF Prescaler Value

P15 and P14 in the RF A,B Counter Latch set the RF prescaler values. See Table 10.

NOTES

1. The prescaler value should be chosen so that the prescaler output frequency is always less than or equal to 125MHz. Thus, with an RF frequency of 2GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not valid.

Table 10. Prescaler Values

P15 P7	P14 P6	Prescaler Value[1]
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

IF Charge Pump Currents
IFCP2, IFCP1, IFCP0 program Current Setting for the IF charge pump. See Table 11.

RF Charge Pump Currents
RFCP2, RFCP1, RFCP0 program Current Setting for the RF charge pump. See Table 11.

Table 11. Charge Pump Currents

RFCP2 IFCP2	RFCP1 IFCP1	RFCP0 IFCP0	Output
0	0	0	0.625mA
0	0	1	1.25 mA
0	1	0	1.875 mA
0	1	1	2.5 mA
1	0	0	3.125 mA
1	0	1	3.75 mA
1	1	0	4.375 mA
1	1	1	5.0 mA

IF Fastlock
The IF CP Gain bit of the IF N register in the ADF4210 family is the Fastlock Enable Bit. Only when this is “1” is IF Fastlock enabled. When Fastlock is enabled, the IF CP current is set to it's maximum value. Also an extra loop filter damping resistor to ground is switched in using the FL_O pin. thus compensating for the change in loop characteristics while in Fastlock. Since the IF CP Gain bit is contained in the IF N Counter, only one write is needed to both program a new output frequency and also initiate Fastlock. To come out of fastlock, the IF CP Gain bit on the IF N register must be set to "0".

RF Fastlock
The RF CP Gain bit of the RF N register in the ADF4210 family is the Fastlock Enable Bit. Only when this is “1” is RF Fastlock enabled. When Fastlock is enabled, the RF CP current is set to it's maximum value. Also an extra loop filter damping resistor to ground is switched in using the FL_O pin. thus compensating for the change in loop characteristics while in Fastlock. Since the RF CP Gain bit is contained in the RF N Counter, only one write is needed to both program a new output frequency and also initiate Fastlock. To come out of fastlock, the RF CP Gain bit on the RF N register must be set to "0".

Device Programming After Initial Power-Up.
After initially powering up the device, there are three ways to program the device.