14-Bit, 300 MSPS High Speed TxDAC+® D/A Converter

Preliminary Technical Data

12-17-99

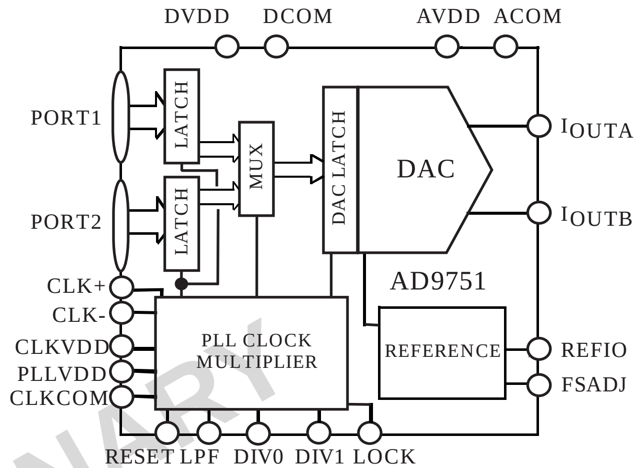
AD9755*

FEATURES

- 14-Bit Dual Muxed Port DAC
- 300 MSPS Output Update Rate
- Excellent SFDR and IMD Performance
- SFDR to Nyquist @25MHz Output: 74dB
- Internal 2x Clock Doubler/PLL
- Differential or Single Ended Clock Input
- On-chip 1.2 V Reference
- Single +3 V Supply Operation
- Power Dissipation: <300 mW @ 3V
- Power Down Mode: 25 mW AVDD @ 3 V
- 48-Lead LQFP

APPLICATIONS

Communications:
LMDS, LMCS, MMDS
Basestations
Digital Synthesis
Quadrature Modulation



BLOCK DIAGRAM

PRODUCT DESCRIPTION

The AD9755 is a dual muxed port, ultra high-speed, single channel,14-bit CMOS DAC. It integrates a high-quality 14-bit TxDAC+® core, a voltage reference, and digital interface circuitry into a small 48-lead LQFP package. The AD9755 offers exceptional ac and dc performance while supporting update rates up to 300MSPS.

The AD9755 has been optimized for ultra high speed applications up to 300MSPS where data rates exceed those possible on a single data interface port DAC. The digital interface consists of two buffered latches as well as control logic. These latches can be time multiplexed to the high speed DAC in several ways. For applications where the duty cycle of the input clock is not 50%, the internal PLL can be used. This PLL drives the DAC latch at twice the speed of the externally applied clock and is able to interleave the data from the two input channels. The resulting output data rate is twice that of the two input channels. For applications where the duty cycle of the input clock is 50%, or may be sensitive to clock jitter, the PLL can be disabled and a separate on-chip internal clock doubler may be used. With the PLL disabled, this clock doubler may be used, or another mode is available in which an external 2× clock is supplied and divided by two internally.

The CLK inputs (CLK+/CLK-) can be driven either differentially or single ended, with a signal swing as low as 1V p-p.

The DAC utilizes a segmented current source architecture combined with a proprietary switching technique to reduce glitch energy and to maximize dynamic accuracy. Differential current outputs support single-ended or differential applications. The differential outputs each provide a nominal full-scale current from 2 to 20mA.

The AD9755 is manufactured on an advanced low cost 0.35µm CMOS process. It operates from a single supply of 2.7V to 3.6V and consumes <300 mW of power.

PRODUCT HIGHLIGHTS

1. The AD9755 is a member of a pin-compatible family of high speed TxDAC+s providing 10, 12, and 14 bit resolution.

2. Ultra high speed 300MSPS conversion rate.

3. Dual 14-Bit Latched, Multiplexed Input Ports: The AD9755 features a flexible dual-port interface allowing high speed data interfacing.

4. Internal Clock Doubler, differential and single ended clock inputs.

5. Low Power: Complete CMOS DAC function operates on <300 mW from a 2.7 V to 3.6 V single supply. The DAC full-scale current can be reduced for lower power operation.

6. On-chip Voltage Reference: The AD9755 includes a 1.20 V temperature-compensated bandgap voltage reference.

TxDAC+ is a registered trademark of Analog Devices, Inc.
*Patent pending

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DC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +3 V, DVDD = +3 V, PLLVDD=3 V, CLKVDD=3 V, I_{OUTFS} = 20 mA, unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	14			Bits
DC ACCURACY [1]				
Integral Linearity Error (INL)	TBD	0.5	TBD	LSB
Differential Nonlinearity (DNL)	TBD	0.25	TBD	LSB
ANALOG OUTPUT				
Offset Error	–0.025		+0.025	% of FSR
Gain Error (Without Internal Reference)	–5	±2	+5	% of FSR
Gain Error (With Internal Reference)	–7	±1	+7	% of FSR
Full-Scale Output Current [2]	2.0		20.0	mA
Output Compliance Range	–1.0		1.25	V
Output Resistance		100		KΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage	1.08	1.20	1.32	V
Reference Output Current [3]		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance		1		MΩ
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±50		ppm of FSR/°C
Gain Drift (With Internal Reference)		±100		ppm of FSR/°C
Reference Voltage Drift		±50		ppm/°C
POWER SUPPLY				
Supply Voltages				
AVDD	2.7	3.0	3.3	V
DVDD	2.7	3.0	3.3	V
PLLVDD	2.7	3.0	3.3	V
CLKVDD	2.7	3.0	3.3	V
Analog Supply Current (I_{AVDD})		33		mA
Digital Supply Current (I_{DVDD})		65		mA
PLL Supply Current (I_{PLLVDD})		4.5		mA
Clock Supply Current (I_{CLKVDD})		5.5		mA
Power Dissipation (3 V, I_{OUTFS} = 20 mA)		300		mW
Power Supply Rejection Ratio [4] —AVDD	–0.4		+0.4	% of FSR/V
Power Supply Rejection Ratio [4] —DVDD	–0.05		+0.05	% of FSR/V
OPERATING RANGE	–40		+85	°C

NOTES

1 Measured at I_{OUTA}, driving a virtual ground.

2 Nominal full-scale current, I_{OUTFS}, is 32× the I_{REF} current.

3 An external buffer amplifier is recommended to drive any external load.

4 ±5% Power supply variation.

Specifications subject to change without notice.

DYNAMIC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +3 V, DVDD = +3 V, CLKVDD = 3 V, PLLVDD = 0 V, I_{OUTFS} = 20 mA, Differential Transformer Coupled Output, 50Ω Doubly Terminated, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (F_{DAC})	300			MSPS
Output Settling Time (t_{ST}) (to 0.1%)[1]		11		ns
Output Propagation Delay (t_{PD})[1]		1		ns
Glitch Impulse[1]		5		pV-s
Output Rise Time (10% to 90%)[1]		2.5		ns
Output Fall Time (10% to 90%)[1]		2.5		ns
Output Noise (I_{OUTFS} = 20 mA)		50		pA/√Hz
Output Noise (I_{OUTFS} = 2 mA)		30		pA/√Hz
AC LINEARITY				
Spurious-Free Dynamic Range to Nyquist				
f_{DATA} = 100 MSPS; f_{OUT} = 1.00 MHz				
0 dBFS Output				
T_A = +25°C	78	85		dBc
T_{MIN} to T_{MAX}	74			dBc
–6 dBFS Output		79		dBc
–12 dBFS Output		77		dBc
–18 dBFS Output		75		dBc
f_{DATA} = 65 MSPS; f_{OUT} = 1.01 MHz		84		dBc
f_{DATA} = 65 MSPS; f_{OUT} = 2.51 MHz		84		dBc
f_{DATA} = 65 MSPS; f_{OUT} = 5.02 MHz		80		dBc
f_{DATA} = 65 MSPS; f_{OUT} = 15.2 MHz		77		dBc
f_{DATA} = 65 MSPS; f_{OUT} = 25.2 MHz		74		dBc
f_{DATA} = 150 MSPS; f_{OUT} = 5.02 MHz		80		dBc
f_{DATA} = 150 MSPS; f_{OUT} = 15.2 MHz		78		dBc
f_{DATA} = 150 MSPS; f_{OUT} = 25.2 MHz		76		dBc
f_{DATA} = 150 MSPS; f_{OUT} = 40.2 MHz		74		dBc
f_{DATA} = 150 MSPS; f_{OUT} = 50.2 MHz		73		dBc
Spurious-Free Dynamic Range within a Window				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1 MHz; 2 MHz Span				
T_A = +25°C	78	88		dBc
T_{MIN} to T_{MAX}	76			dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 5.02 MHz; 2 MHz Span		85		dBc
f_{CLOCK} = 150 MSPS; f_{OUT} = 5.04 MHz; 4 MHz Span		85		dBc
Total Harmonic Distortion				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz				
T_A = +25°C		–84	–76	dBc
T_{MIN} to T_{MAX}			–74	dBc
f_{CLOCK} = 50 MHz; f_{OUT} = 2.00 MHz		–80		dBc
f_{CLOCK} = 150 MHz; f_{OUT} = 2.00 MHz		–80		dBc
Multitone Power Ratio (Eight Tones at 110kHz Spacing)				
f_{CLOCK} = 65MSPS; f_{OUT} = 2.00MHz to 2.77MHz				
0dBFS Output		80		dBc
-6dBFS Output		78		dBc
-12dBFS Output		75		dBc
-18dBFS Output		71		dBc

NOTES
1 Measured single-ended into 50 Ω load.
Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +3 V, DVDD = +3 V, CLKVDD = 3 V, PLLVDD = 3 V, I_{OUTFS} = 20 mA, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DIGITAL INPUTS[1]				
Logic "1"	2.1	3		V
Logic "0"		0	0.9	V
Logic "1" Current	–10		+10	µA
Logic "0" Current	–10		+10	µA
Input Capacitance		5		pF
Input Setup Time (t_S)		2.0		ns
Input Hold Time (t_H)	TBD			ns
Min CLK freq[2]		6.25		MHz

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AVDD	ACOM	–0.3	+3.9	V
DVDD	DCOM	–0.3	+3.9	V
PLVDD	DCOM	–0.3	+3.9	V
CLKVDD	DCOM	–0.3	+3.9	V
ACOM	DCOM	–0.3	+0.3	V
CLK+/CLK-	DCOM	–0.3	DVDD + 0.3	V
Digital Inputs (DB11 to DB0)	DCOM	–0.3	DVDD + 0.3	V
I_{OUTA}, I_{OUTB}	ACOM	–1.0	AVDD + 0.3	V
REFIO, FSADJ	ACOM	–0.3	AVDD + 0.3	V
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
AD9755AST	–40°C to +85°C	48-Lead LQFP	ST-48
AD9755-EB			Evaluation Board

Thermal Characteristics
Thermal Resistance
48-Lead LQFP
θ_{JA} = 91°C/W

NOTES
1DIV0,DIV1=(1,1).
2Min CLK freq only applies when using internal PLL. When PLL is disabled, there is no minimum CLK frequency.

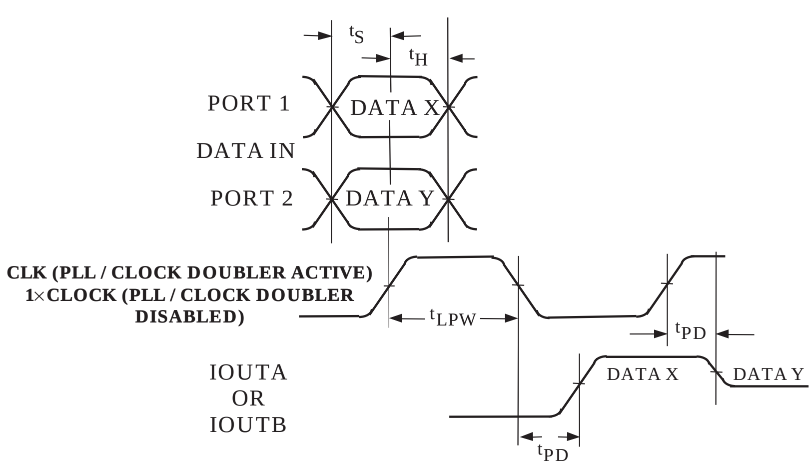
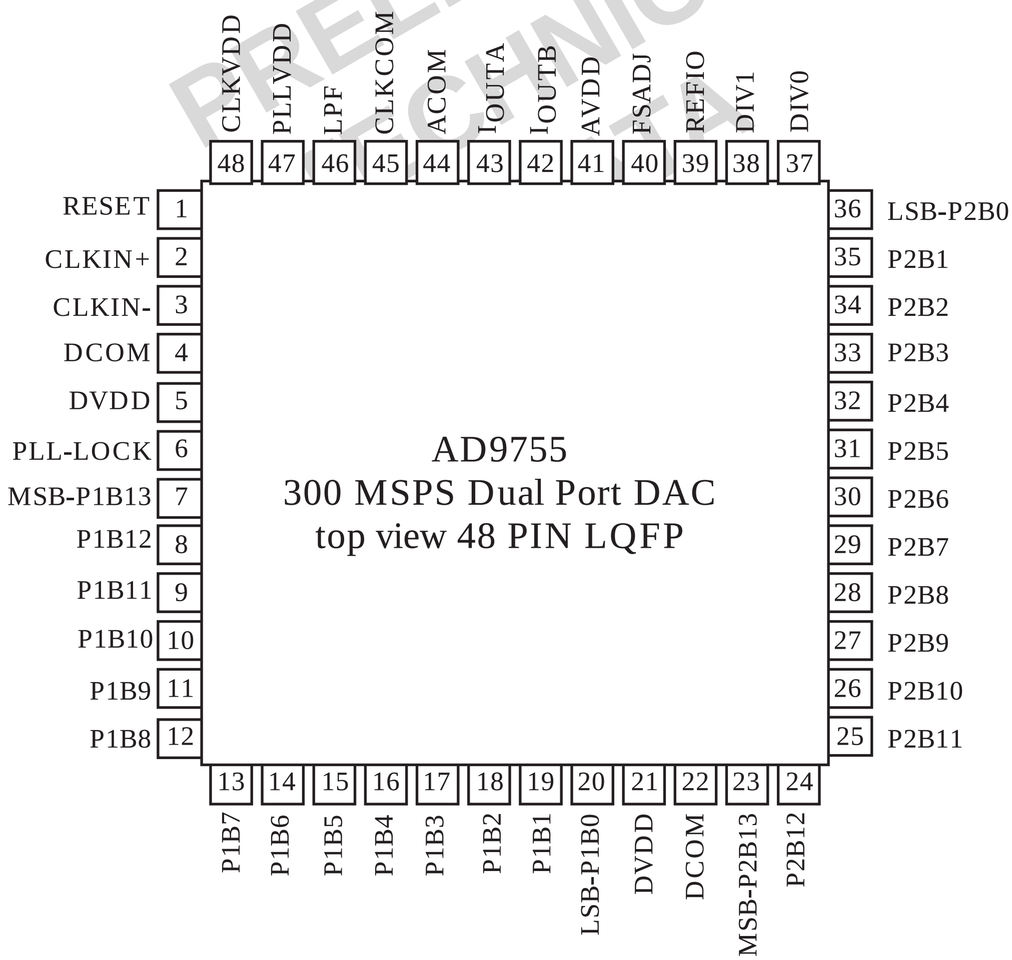


Figure 1. AD9755 I/O Timing

PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Description
43	I_{OUTA}	Differential DAC current output
42	I_{OUTB}	Differential DAC current output
39	REFIO	Reference input/output
37,38	DIV0,DIV1	Control inputs for PLL and input port selector mode, see tables I and II for details
40	FSADJ	Full-scale current output adjust
41	AVDD	Analog Supply Voltage
44	ACOM	Analog Common
5,21	DVDD	Digital Supply Voltage
4,22	DCOM	Digital Common
47	PLLVDD	Phase Locked Loop Supply Voltage
48	CLKVDD	Clock Supply Voltage
45	CLKCOM	Clock and Phase Locked Loop Common
2	CLK+	Differential Clock input
3	CLK-	Differential Clock input
46	LPF	PLL Low Pass Filter
1	RESET	Internal Clock Divider Reset
6	PLL-LOCK	PLL Lock Indicator Output
7-20	DB13-P1/DB0-P1	Data bits DB13 to DB0, port 1
23-36	DB13-P2/DB0-P2	Data bits DB13 to DB0, port 2



FUNCTIONAL DESCRIPTION

Figure 2 shows a simplified block diagram of the AD9755. The AD9755 consists of a PMOS current source array capable of providing up to 20ma of full-scale current, I_{OUTFS}. The array is divided into 31 equal sources that make up the five most significant bits (MSB's). The next four bits, or middle bits, consist of 15 equal current sources whose value is 1/16th of an MSB current source. The remaining LSBs are a binary weighted fraction of the middle bit current sources. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances dynamic performance for multitone or low amplitude signals and helps maintain the DAC's high output impedance (i.e., >100KΩ).

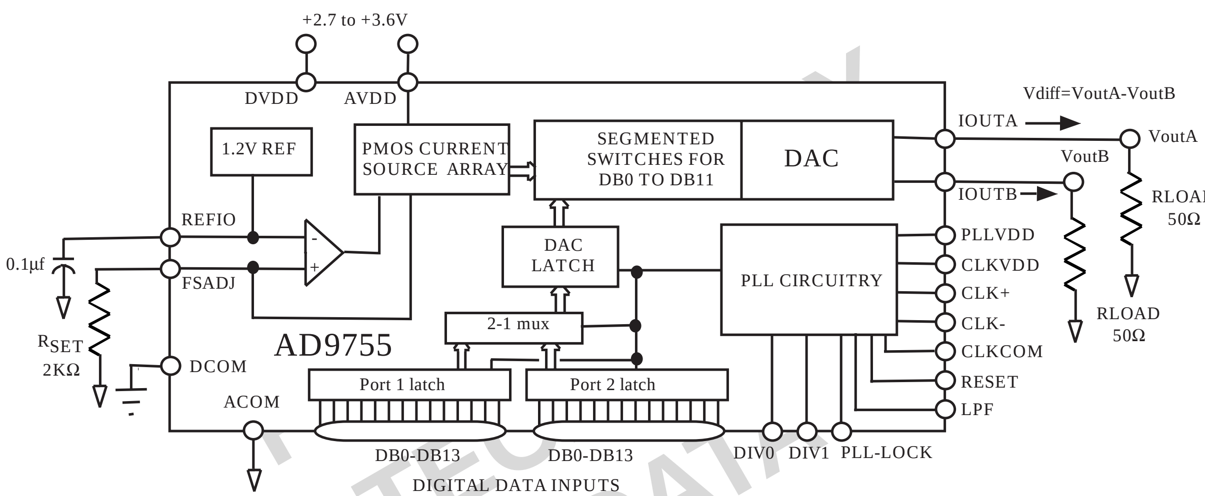


Figure 2. Simplified Block Diagram

All of the current sources are switched to one or the other of the two outputs (i.e., IOUTA or IOUTB) via PMOS differential current switches. The switches are based on a new architecture that drastically improves distortion performance. This new switch architecture reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The analog and digital sections of the AD9755 have separate power supply inputs (i.e., AVDD and DVDD) that can operate independently over a 2.7 volt to 3.6 Volt range. The digital section, which is capable of operating at a 300 MSPS clock rate, consists of edge-triggered latches and segment decoding logic circuitry. The analog section includes the PMOS current sources, the associated differential switches, a 1.20 V bandgap voltage reference and a reference control amplifier.

The full-scale output current is regulated by the reference control amplifier and can be set from 2 mA to 20 mA via an external resistor, R_{SET}. The external resistor, in combination with both the reference control amplifier and voltage reference V_{REFIO}, sets the reference current I_{REF}, which is replicated to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is thirty-two times the value of I_{REF}.

REFERENCE OPERATION

The AD9755 contains an internal 1.20 V bandgap reference. This can be easily overdriven by an external reference with no effect on performance. REFIO serves as either an *input* or *output* depending on whether the internal or an external reference is used. To use the internal reference, simply decouple the REFIO pin to ACOM with a 0.1µF capacitor. The internal reference voltage will be present at REFIO. If the voltage at REFIO is to be used elsewhere in the circuit, an external buffer amplifier with an input bias current less than 100nA should be used. An example of the use of the internal reference is given in Figure 3.

An external reference can be applied to REFIO as shown in Figure 4. The external reference may provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. Note that the 0.1 µF compensation capacitor is not required since the internal reference is overdriven, and the relatively high input impedance of REFIO minimizes any loading of the external reference.

REFERENCE CONTROL AMPLIFIER

The AD9755 also contains an internal control amplifier that is used to regulate the DAC's full-scale output current, I_{OUTFS}. The control amplifier is configured as a voltage to current converter as shown in Figure 3, so that its current output, I_{REF}, is determined by the ratio of V_{REFIO} and an external resistor, R_{SET}, as stated in Equation 4. I_{REF} is applied to the segmented current sources with the proper scaling factor to set I_{OUTFS} as stated in Equation 3.

The control amplifier allows a wide (10:1) adjustment span of I_{OUTFS} over a 2 mA to 20 mA range by setting IREF between 62.5 µA and 625 µA. The wide adjustment span of I_{OUTFS} provides several application benefits. The first benefit relates directly to the power dissipation of the AD9755, which is proportional to I_{OUTFS} (refer to the POWER DISSIPATION section). The second benefit relates to the 20 dB adjustment, which is useful for system gain control purposes.

The small signal bandwidth of the reference control amplifier is approximately 500KHz and can be used for low frequency small signal multiplying applications.

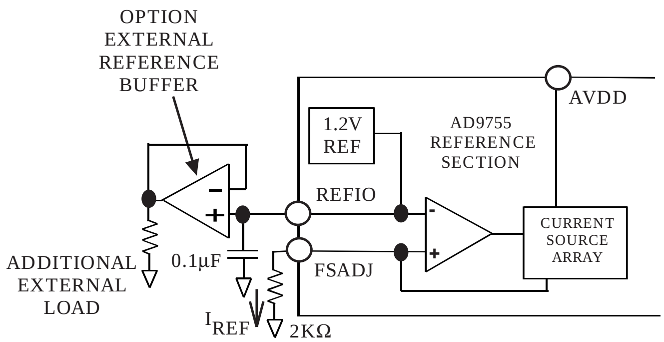


Figure 3. Internal Reference Configuration

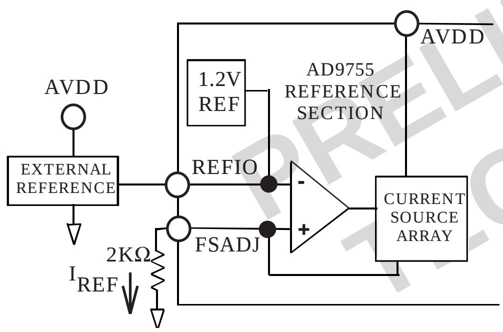


Figure 4. External Reference Configuration

PLL CLOCK MULTIPLIER OPERATION

The Phase Locked Loop (PLL) is intrinsic to the operation of the AD9755 in that it produces the necessary internally synchronized 2× clock for the edge triggered latches, multiplexer and DAC.

With PLLVDD connected to its supply voltage, the AD9755 is in PLL ACTIVE mode. Fig 5 shows a functional block diagram of the AD9755 clock control circuitry with PLL active. The circuitry consists of a phase detector, charge pump, voltage controlled oscillator (VCO), input data rate range control, clock logic circuitry and control input/outputs. The ÷2 logic in the feedback loop allows the PLL to generate the 2× clock needed for the DAC output latch.

Figure 6 defines the input and output timing for the AD9755 with the PLL active. CLK in Figure 6 represents the clock which is generated external to the AD9755 which also updates the input data at ports 1 and 2. CLK may be applied as a single ended signal by tying CLK- to mid supply and applying CLK to CLK+, or as a differential signal applied to CLK+ and CLK-.

RESET has no purpose when using the internal PLL and should be grounded. When the AD9755 is in PLL ACTIVE mode, LOCK is the output of the internal phase detector. When locked, the lock output in this mode will be a logic “1”.

Typically, the VCO can generate outputs of 100 to 400 MHz. The range control is used to keep the VCO operating within its designed range, while allowing input clocks as low as 6.25 MHz. With the PLL active, logic levels at DIV0 and DIV1 determine the divide ratio of the range controller. Table I gives the frequency range of the input clock for the different states of DIV0 and DIV1.

A 392Ω resistor and 1.0µf capacitor connected in series from LPF to PLLVDD are required to optimize the phase noise vs. settling/acquisition time characteristics of the PLL. To obtain optimum noise and distortion performance, PLLVDD should be set to a voltage level similar to DVDD.

SNR is partly a function of the jitter generated by the clock circuitry. As a result, any noise on PLLVDD or CLKVDD may decrease the SNR at the output of the DAC. To minimize this potential problem, PLLVDD and CLKVDD can be connected to DVDD using an LC filter network similar to that shown in Figure 7.

DAC TIMING WITH PLL ACTIVE

In PLL ACTIVE mode, port 1 and port 2 input latches are updated on the rising edge of CLK. On the same rising edge, data previously present in the input port 2 latch is written to the DAC output latch. The DAC output will update accordingly after a short propagation delay.

Following the rising edge of CLK, at a time equal to half of its period, the data in the port 1 latch will be written to the DAC output latch, again with a corresponding change in the DAC output. Due to the internal PLL, the time at which the data in the port 1

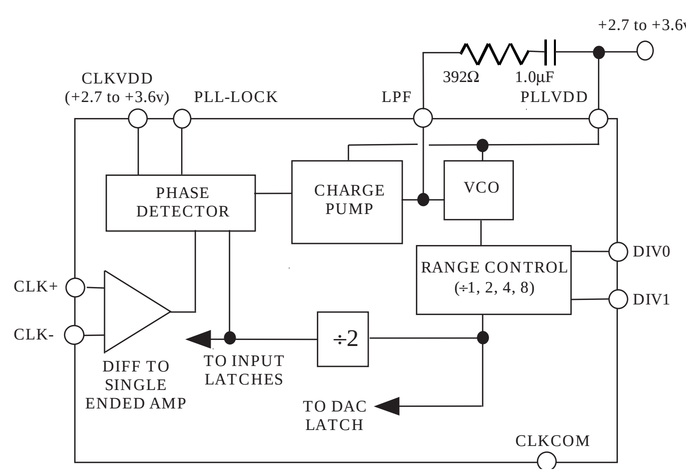


Figure 5. AD9755 Clock Circuitry with PLL Active

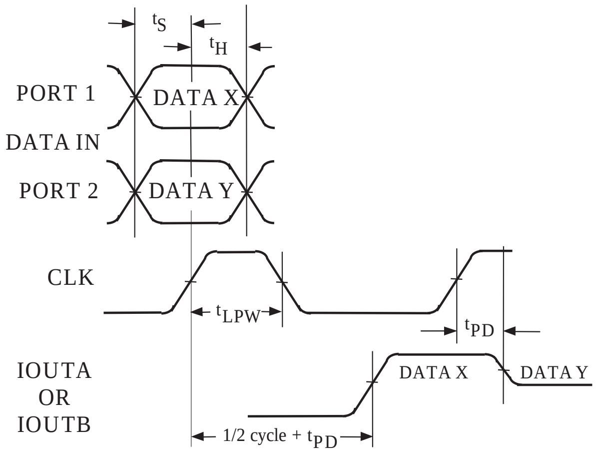


Figure 6a.

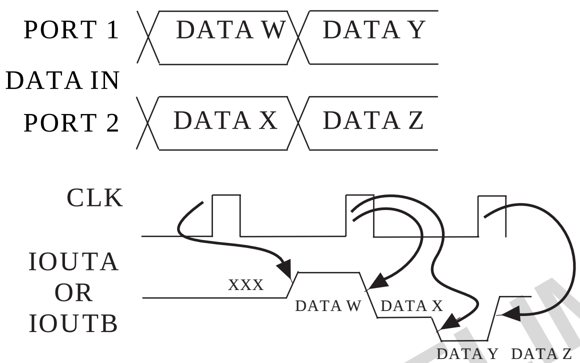


Figure 6b.

Figure 6. DAC Input Timing Requirements with PLL Active

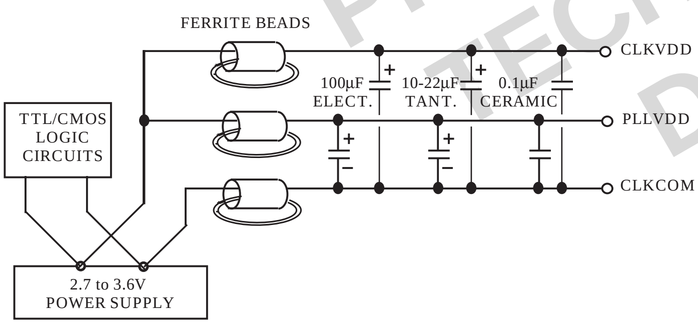


Figure 7. LC Network for Power Filtering

Table I, CLK rates for DIV0, DIV1 levels with PLL active

CLK freq	DIV1	DIV0	Range Controller
50-150 MHz	0	0	÷1
25-100 MHz	0	1	÷2
12.5-50 MHz	1	0	÷4
6.25-25 MHz	1	1	÷8

and port 2 input latches is written to the DAC latch is independent of the duty cycle of CLK. When using the PLL, the external clock can be operated at any duty cycle that meets the specified latch pulse width.

On the next rising edge of CLK, the cycle begins again with the two input port latches being updated, and the DAC output latch being updated with the current data in the port 2 input latch.

PLL DISABLED MODE

When PLLVDD is grounded, the PLL is disabled. An external clock must now drive the CLK inputs at the desired DAC output update data rate. The speed and timing of the data present at input ports 1 and 2 is now dependent on whether or not the AD9755 is interleaving the digital input data, or only responding to data on a single port. Figure 8 is a functional block diagram of the AD9755 clock control circuitry with the PLL disabled.

DIV0 and DIV1 no longer control the PLL, but are used to set the control on the input mux for either interleaving or non-interleaving the input data. The different modes for states of DIV0 and DIV1 are given in Table II.

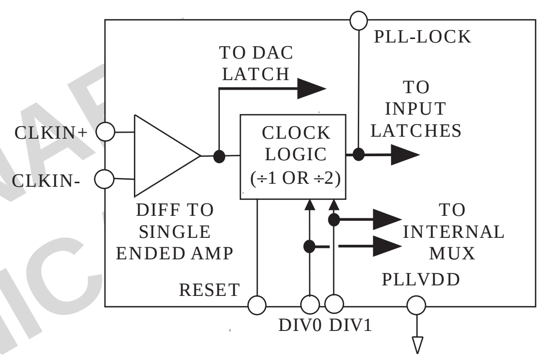


Figure 8. AD9755 Clock Circuitry with PLL Disabled

Table II, Input Mode for DIV0, DIV1 Levels with PLL Disabled

Input Mode	DIV1	DIV0
Interleaved (2×)	0	0
Non-Interleaved		
Port 1 selected	0	1
Port 2 selected	1	0
Interleaved (Clock Doubler Active)	1	1

INTERLEAVED (2×) MODE WITH PLL DISABLED

The relationship between the internal and external clocks in this mode is shown in Figure 9. A clock at the output update data rate (2× the input data rate) must be applied to the CLK inputs. Internal dividers then create the internal 1× clock necessary for the input latches. With the PLL disabled, a delayed version of the 1× clock is present at the PLL-LOCK pin. The DAC latch is updated by the external 2× clock. Updates to the data at input ports 1 and 2 should be synchronized to the specific rising edge of the external 2× clock which corresponds to the rising edge of the 1× internal clock as shown in Figure 9. To ensure this synchronization, a logic "1" should be momentarily applied to the RESET pin on power up, before CLK is applied. Applying a momentary logic "1" to RESET

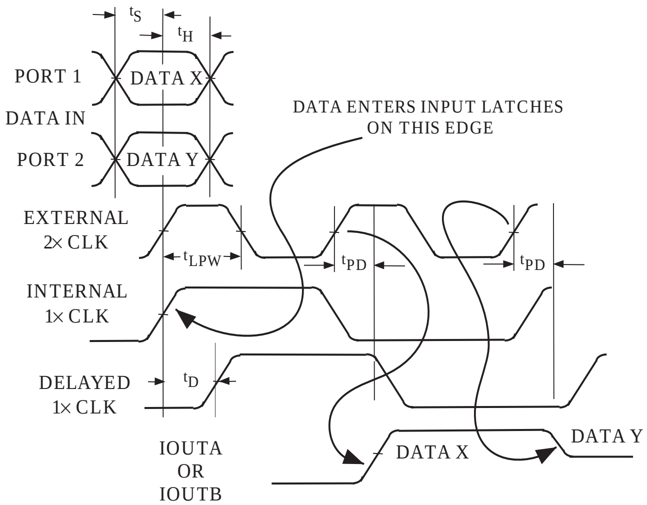


Figure 9. AD9755 Timing Requirements, Interleaved (2×) *Mode with PLL Disabled*

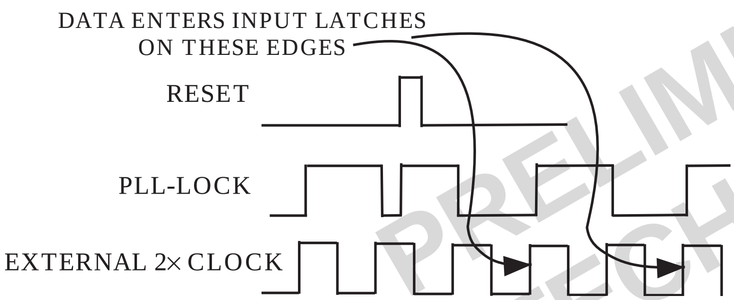


Figure 10. AD9755 Reset Function Timing with PLL Disabled

brings the 1× clock at PLL-LOCK to a logic "1". On the next rising edge of the 2× clock, the 1× clock will go to logic "0". The following rising edge of the 2× clock will cause the 1× clock to to logic "1" again, as well as update the data in both of the input latches. The details of this are given in figure 10.

NON-INTERLEAVED MODE WITH PLL DISABLED

If the data at only one port is required, the AD9755 interface can operate as a simple double buffered latch with no interleaving. On the rising edge of the 1× clock, input latch 1 or 2 is updated with the present input data. On the next rising edge, the DAC latch is updated and a propagation time later the DAC output reflects this change. Figure 11 represents the AD9755 timing in this mode.

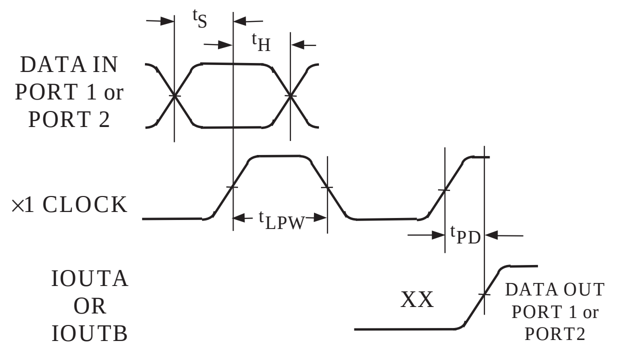


Figure 11. AD9755 Timing Requirements, Non-Interleaved Mode with PLL Disabled

INTERLEAVED MODE WITH PLL DISABLED, CLOCK DOUBLER ACTIVE

This mode is nearly identical to operation with the PLL active. However, in this mode an internal clock doubler logic circuit (not the PLL) is used to generate the internal 2× clock signals when an external 1× clock is applied. The significant difference is that the externally applied 1× clock must have a 50% duty cycle. The relationship between the internal and external clocks in this mode is shown in Figure 12.

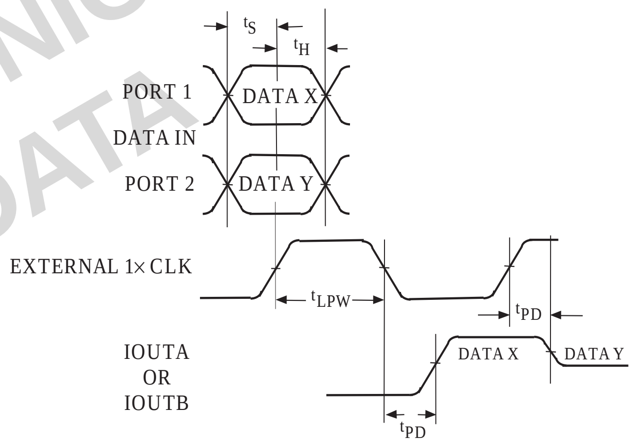


Figure 12. AD9755 Timing Requirements, Interleaved Mode with PLL Disabled, Clock Doubler Active

DAC TRANSFER FUNCTION

The AD9755 provides complementary current outputs, I_{OUTA} and I_{OUTB}. I_{OUTA} will provide a near full-scale current output, I_{OUTFS}, when all bits are high (i.e., DAC CODE = 1023) while I_{OUTB}, the complementary output, provides no current. The current output appearing at I_{OUTA} and I_{OUTB} is a function of both the input code and I_{OUTFS} and can be expressed as:

$$I_{OUTA} = (DAC\ CODE/1024) \times I_{OUTFS} \quad (1)$$

$$I_{OUTB} = (16383 - DAC\ CODE)/16384 \times I_{OUTFS} \quad (2)$$

where *DAC CODE* = 0 to 1023 (i.e., Decimal Representation).

As mentioned previously, I_{OUTFS} is a function of the reference current I_{REF}, which is nominally set by a reference voltage, V_{REFIO} and external resistor R_{SET}. It can be expressed as:

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

where $I_{REF} = V_{REFIO}/R_{SET}$ (4)

The two current outputs will typically drive a resistive load directly or via a transformer. If dc coupling is required, I_{OUTA} and I_{OUTB} should be directly connected to matching resistive loads, R_{LOAD}, that are tied to analog common, ACOM. Note, R_{LOAD} may represent the equivalent load resistance seen by I_{OUTA} or I_{OUTB} as would be the case in a doubly terminated 50Ωor 75Ω cable. The single-ended voltage output appearing at the I_{OUTA} and I_{OUTB} nodes is simply :

$$V_{OUTA} = I_{OUTA} \times R_{LOAD} \quad (5)$$

$$V_{OUTB} = I_{OUTB} \times R_{LOAD} \quad (6)$$

Note the full-scale value of V_{OUTA} and V_{OUTB} should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

$$V_{DIFF} = (I_{OUTA} - I_{OUTB}) \times R_{LOAD} \quad (7)$$

Substituting the values of I_{OUTA}, I_{OUTB} and I_{REF}; V_{DIFF} can be expressed as:

$$V_{DIFF} = \{(2\ DAC\ CODE - 1023)/1024\} \times (32\ R_{LOAD}/R_{SET}) \times V_{REFIO} \quad (8)$$

These last two equations highlight some of the advantages of operating the AD9755 differentially. First, the differential operation will help cancel common-mode error sources associated with I_{OUTA} and I_{OUTB} such as noise, distortion and dc offsets. Second, the differential code dependent current and subsequent voltage, V_{DIFF}, is twice the value of the single-ended voltage output (i.e., V_{OUTA} or V_{OUTB}), thus providing twice the signal power to the load.

Note, that the gain drift temperature performance for a single-ended (V_{OUTA} and V_{OUTB}) or differential output (V_{DIFF}) of the AD9755 can be enhanced by selecting temperature tracking resistors for R_{LOAD} and R_{SET} due to their ratiometric relationship as shown in Equation 8.

ANALOG OUTPUTS

The AD9755 produces two complementary current outputs, I_{OUTA} and I_{OUTB}, which may be configured for single-ended or differential operation. I_{OUTA} and I_{OUTB} can be converted into complementary single-ended voltage outputs, V_{OUTA} and V_{OUTB}, via a load resistor, R_{LOAD}, as described in the DAC TRANSFER FUNCTION section by Equations 5 through 8. The differential voltage, V_{DIFF}, existing between V_{OUTA} and V_{OUTB} can also be converted to a single-ended voltage via a transformer or differential amplifier configuration. The ac performance of the AD9755 is optimum and specified using a differential transformer coupled output in which the voltage swing at I_{OUTA} and I_{OUTB} is limited to ±0.5 V. If a single-ended unipolar output is desirable, I_{OUTA} should be selected as the output, with I_{OUTB} grounded.

The distortion and noise performance of the AD9755 can be enhanced when it is configured for differential operation. The common-mode error sources of both I_{OUTA} and I_{OUTB} can be significantly reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the frequency content of the reconstructed waveform increases. This is due to the first order cancellation of various dynamic common-mode distortion mechanisms, digital feedthrough and noise.

Performing a differential-to-single-ended conversion via a transformer also provides the ability to deliver twice the reconstructed signal power to the load (i.e., assuming no source termination). Since the output currents of I_{OUTA} and I_{OUTB} are complementary, they become additive when processed differentially. A properly selected transformer will allow the AD9755 to provide the required power and voltage levels to different loads. Refer to APPLYING THE AD9755 section for examples of various output configurations.

The output impedance of I_{OUTA} and I_{OUTB} is determined by the equivalent parallel combination of the PMOS switches associated with the current sources and is typically 100 KΩ in parallel with 5 pF. It is also slightly dependent on the output voltage (i.e., V_{OUTA} and V_{OUTB}) due to the nature of a PMOS device. As a result, maintaining I_{OUTA} and/or I_{OUTB} at a virtual ground via an I-V op amp configuration will result in the optimum dc linearity. Note the INL/DNL specifications for the AD9755 are measured with I_{OUTA} and I_{OUTB} maintained at virtual ground via an op amp.

I_{OUTA} and I_{OUTB} also have a negative and positive voltage compliance range that must be adhered to in order to achieve optimum performance. The negative output compliance range of –1.0 V is set by the breakdown limits of the CMOS process. Operation beyond this maximum limit may result in a breakdown of the output stage and affect the reliability of the AD9755.

The positive output compliance range is slightly dependent on the full-scale output current, I_{OUTFS}. It degrades slightly from its nominal 1.25 V for an I_{OUTFS} = 20 mA to 1.00 V for an I_{OUTFS} = 2 mA. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at I_{OUTA} and I_{OUTB} does not exceed 0.5 V. Applications requiring the AD9755's output (i.e., V_{OUTA} and/or V_{OUTB}) to extend its output compliance range should size R_{LOAD} accordingly. Operation beyond this compliance range will adversely affect the AD9755's linearity performance and subsequently degrade its distortion performance.

DIGITAL INPUTS

The AD9755's digital input consists of two channels of 14 data input pins each and a pair of differential clock input pins. The 14-bit parallel data inputs follow standard straight binary coding where DB11 is the most significant bit (MSB) and DB0 is the least significant bit (LSB). I_{OUTA} produces a full-scale output current when all data bits are at logic 1. I_{OUTB} produces a complementary output with the full-scale current split between the two outputs as a function of the input code.

The digital interface is implemented using an edge-triggered master slave latch. With the PLL active, or when using the internal clock doubler, the DAC output is updated twice for every input clock period, as shown in Figure 6, 9 and 11, and is designed to support a clock input rate as high as 150 MSPS. This gives a DAC output update rate of 300MSPS. The setup and hold times can also be varied within the clock cycle as long as the specified minimum times are met, although the location of these transition edges may affect digital feedthrough and distortion performance. Best performance is typically achieved when the input data transitions on the falling edge of a 50% duty cycle clock.

The digital inputs are CMOS-compatible with logic thresholds, VTHRESHOLD, set to approximately half the digital positive supply (DVDD) or

$$VTHRESHOLD = DVDD/2\ (\pm 20\%)$$

The internal digital circuitry of the AD9755 is capable of operating over a digital supply range of 2.7V to 3.6 V. As a result, the digital inputs can also accommodate TTL levels when DVDD is set to accommodate the maximum high level voltage of the TTL drivers V_{OH}(MAX). A DVDD of 3V to 3.3V will typically ensure proper compatibility with most TTL logic families. Figure 13 shows the equivalent digital input circuit for the data and clock inputs.

The AD9755 features a flexible differential clock input operatingfrom separate supplies (i.e., CLKVDD, CLKCOM) to achieve optimum jitter performance. The two clock inputs, CLK+ and CLK-, can be driven from a single-ended or differential clock source. For single ended operation, CLK+ should be driven by a logic source while CLK- should be set to the threshold voltage of the logic source. This can be done via a resistor divider/capacitor network as shown in Figure 14a. For differential operation, both CLK+ and CLK- should be biased to CLKVDD/2 via a resistor divider network as shown in Figure 14b.

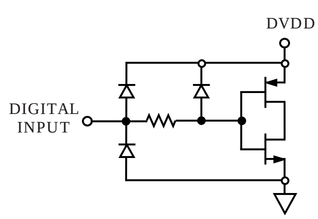


Figure 13. Equivalent Digital Input

Because the output of the AD9755 is capable of being updated at up to 300 MSPS, the quality of the clock and data input signals are important in achieving the optimum performance. Operating the AD9755 with reduced logic swings and a corresponding digital supply (DVDD) will result in the lowest data feedthrough and on-chip digital noise. The drivers of the digital data interface circuitry should be specified to meet the minimum setup and hold times of the AD9755 as well as its required min/max input logic level thresholds.

Digital signal paths should be kept short and run lengths matched to avoid propagation delay mismatch. The insertion of a low value resistor network (i.e., 20 Ω to 100 Ω) between the AD9755 digital inputs and driver outputs may be helpful in reducing any over-shooting and ringing at the digital inputs that contribute to data feedthrough. For longer run lengths and high data update rates, strip line techniques with proper termination resistors should be considered to maintain "clean" digital inputs.

The external clock driver circuitry should provide the AD9755 with a low jitter clock input meeting the min/max logic levels while providing fast edges. Fast clock

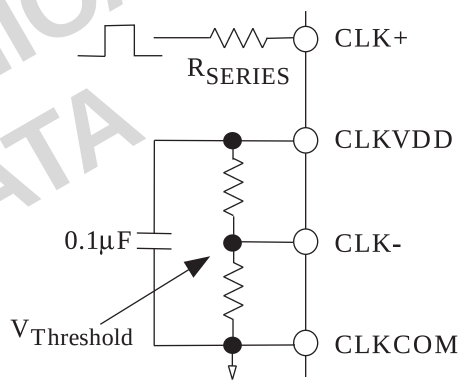


Figure 14a. Single Ended Clock Interface

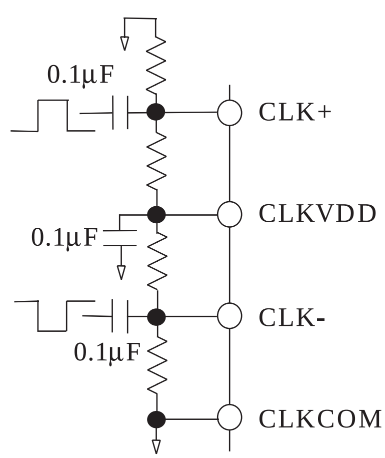


Figure 14b. Differential Clock Interface

edges will help minimize any jitter that will manifest itself as phase noise on a reconstructed waveform. Thus, the clock input should be driven by the fastest logic family suitable for the application.

Note that the clock input could also be driven via a sine wave, which is centered around the digital threshold (i.e., DVDD/2) and meets the min/max logic threshold. This will typically result in a slight degradation in the phase noise, which becomes more noticeable at higher sampling rates and output frequencies. Also, at higher sampling rates, the 20% tolerance of the digital logic threshold should be considered since it will affect the effective clock duty cycle and, subsequently, cut into the required data setup and hold times.

48 pin LQFP package
(ST-48)