Dual 600 MHz, 50 mW Current Feedback Amplifier

AD8002

FEATURES

Excellent Video Specifications (R_L = 150 Ω, G = +2)
- **Gain Flatness 0.1 dB to 60 MHz**
- **0.01% Differential Gain Error**
- **0.02° Differential Phase Error**

Low Power
- **5.5 mA/Amp Max Power Supply Current (55 mW)**

High Speed and Fast Settling
- **600 MHz, –3 dB Bandwidth (G = +1)**
- **500 MHz, –3 dB Bandwidth (G = +2)**
- **1200 V/μs Slew Rate**
- **16 ns Settling Time to 0.1%**

Low Distortion
- **–65 dBc THD, f_C = 5 MHz**
- **33 dBm 3rd Order Intercept, F_1 = 10 MHz**
- **–66 dB SFDR, f = 5 MHz**
- **–60 dB Crosstalk, f = 5 MHz**

High Output Drive
- **Over 70 mA Output Current**
- **Drives Up to Eight Back-Terminated 75 Ω Loads (Four Loads/Side) While Maintaining Good Differential Gain/Phase Performance (0.01%/0.17°)**

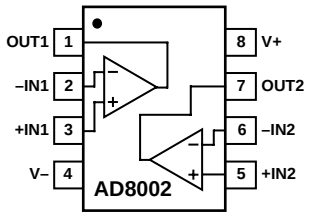
Available in 8-Lead Plastic DIP, SOIC and μSOIC Packages

APPLICATIONS

A-to-D Driver
Video Line Driver
Differential Line Driver
Professional Cameras
Video Switchers
Special Effects
RF Receivers

FUNCTIONAL BLOCK DIAGRAM

8-Lead Plastic DIP, SOIC and μSOIC



PRODUCT DESCRIPTION

The AD8002 is a dual, low power, high speed amplifier designed to operate on ±5 V supplies. The AD8002 features unique transimpedance linearization circuitry. This allows it to drive video loads with excellent differential gain and phase performance on only 50 mW of power per amplifier. The AD8002 is a current feedback amplifier and features gain flatness of 0.1 dB to 60 MHz while offering differential gain and phase error of 0.01% and 0.02°. This makes the AD8002 ideal for professional video electronics such as cameras and video switchers. Additionally, the AD8002's low distortion and fast settling make it ideal for buffer high speed A-to-D converters.

The AD8002 offers low power of 5.5 mA/amplifier max (V_S = ±5 V) and can run on a single +12 V power supply, while capable of delivering over 70 mA of load current. It is offered in an 8-lead plastic DIP, SOIC and μSOIC package. These features make this amplifier ideal for portable and battery powered applications where size and power is critical.

The outstanding bandwidth of 600 MHz along with 1200 V/μs of slew rate make the AD8002 useful in many general purpose high speed applications where dual power supplies of up to ±6 V and single supplies from 6 V to 12 V are needed. The AD8002 is available in the industrial temperature range of –40°C to +85°C.

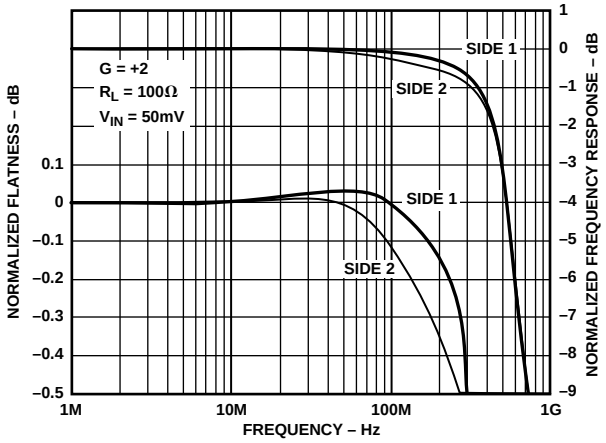


Figure 1. Frequency Response and Flatness, G = +2

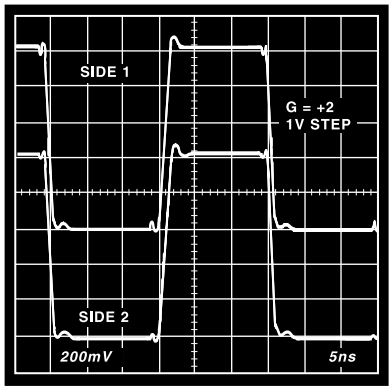


Figure 2. 1 V Step Response, G = +1

REV. C

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AD8002–SPECIFICATIONS (@ T_A = + 25°C, V_S = ±5 V, R_L = 100 Ω, R_C[1] = 75 Ω, unless otherwise noted)

Model		Conditions	AD8002A Min	Typ	Max	Units
DYNAMIC PERFORMANCE						
–3 dB Small Signal Bandwidth,	N Package	G = +2, R_F = 750 Ω		500		MHz
		G = +1, R_F = 1.21 kΩ		600		MHz
	R Package	G = +2, R_F = 681 Ω		500		MHz
		G = +1, R_F = 953 Ω		600		MHz
	RM Package	G = +2, R_F = 681 Ω		500		MHz
		G = +1, R_F = 1 kΩ		600		MHz
Bandwidth for 0.1 dB Flatness						
	N Package	G = +2, R_F = 750 Ω		60		MHz
	R Package	G = +2, R_F = 681 Ω		90		MHz
	RM Package	G = +2, R_F = 681 Ω		60		MHz
Slew Rate		G = +2, V_O = 2 V Step		700		V/µs
		G = –1, V_O = 2 V Step		1200		V/µs
Settling Time to 0.1%		G = +2, V_O = 2 V Step		16		ns
Rise & Fall Time		G = +2, V_O = 2 V Step, R_F = 750 Ω		2.4		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion		f_C = 5 MHz, V_O = 2 V p-p		–65		dBc
		G = +2, R_L = 100 Ω				
Crosstalk, Output to Output		f = 5 MHz, G = +2		–60		dB
Input Voltage Noise		f = 10 kHz, R_C = 0 Ω		2.0		nV/√Hz
Input Current Noise		f = 10 kHz, +In		2.0		pA/√Hz
		–In		18		pA/√Hz
Differential Gain Error		NTSC, G = +2, R_L = 150 Ω		0.01		%
Differential Phase Error		NTSC, G = +2, R_L = 150 Ω		0.02		Degree
Third Order Intercept		f = 10 MHz		33		dBm
1 dB Gain Compression		f = 10 MHz		14		dBm
SFDR		f = 5 MHz		–66		dB
DC PERFORMANCE						
Input Offset Voltage				2.0	6	mV
		T_{MIN}–T_{MAX}		2.0	9	mV
Offset Drift				10		µV/°C
–Input Bias Current				5.0	25	±µA
		T_{MIN}–T_{MAX}			35	±µA
+Input Bias Current				3.0	6.0	±µA
		T_{MIN}–T_{MAX}			10	±µA
Open Loop Transresistance		V_O = ±2.5 V	250	900		kΩ
		T_{MIN}–T_{MAX}	175			kΩ
INPUT CHARACTERISTICS						
Input Resistance		+Input		10		MΩ
		–Input		50		Ω
Input Capacitance		+Input		1.5		pF
Input Common-Mode Voltage Range				3.2		±V
Common-Mode Rejection Ratio						
Offset Voltage		V_{CM} = ±2.5 V	49	54		dB
–Input Current		V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}		0.3	1.0	µA/V
+Input Current		V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}		0.2	0.9	µA/V
OUTPUT CHARACTERISTICS						
Output Voltage Swing		R_L = 150 Ω	2.7	3.1		±V
Output Current[2]				70		mA
Short Circuit Current[2]			85	110		mA
POWER SUPPLY						
Operating Range			±3.0		±6.0	V
Quiescent Current/Both Amplifiers		T_{MIN}–T_{MAX}		10.0	11.5	mA
Power Supply Rejection Ratio		$+V_S$ = +4 V to +6 V, $–V_S$ = –5 V	60	75		dB
		$–V_S$ = – 4 V to –6 V, $+V_S$ = +5 V	49	56		dB
–Input Current		T_{MIN}–T_{MAX}		0.5	2.5	µA/V
+Input Current		T_{MIN}–T_{MAX}		0.1	0.5	µA/V

NOTES

[1]R_C is recommended to reduce peaking and minimize input reflections at frequencies above 300 MHz. However, R_C is not required.

[2]Output current is limited by the maximum power dissipation in the package. See the power derating curves.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 12.6 V
Internal Power Dissipation[2]
  Plastic DIP Package (N) . . . . . 1.3 W
  Small Outline Package (R) . . . . . 0.9 W
  µSOIC Package (RM) . . . . . 0.6 W
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±1.2 V
Output Short Circuit Duration
  . . . . . Observe Power Derating Curves
Storage Temperature Range N, R, RM . . . . . –65°C to +125°C
Operating Temperature Range (A Grade) . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:
8-Lead Plastic DIP Package: θ_{JA} = 90°C/W
8-Lead SOIC Package: θ_{JA} = 155°C/W
8-Lead µSOIC Package: θ_{JA} = 200°C/W

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8002 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

While the AD8002 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

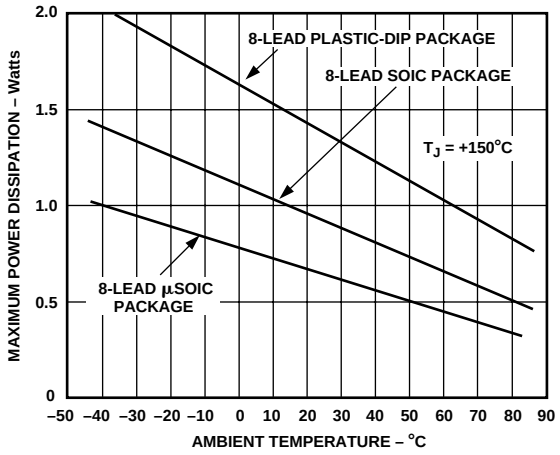


Figure 3. Plot of Maximum Power Dissipation vs. Temperature

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Brand Code
AD8002AN	–40°C to +85°C	8-Lead PDIP	N-8	Standard
AD8002AR	–40°C to +85°C	8-Lead SOIC	SO-8	Standard
AD8002AR-REEL	–40°C to +85°C	8-Lead SOIC 13" REEL	SO-8	Standard
AD8002AR-REEL7	–40°C to +85°C	8-Lead SOIC 7" REEL	SO-8	Standard
AD8002ARM	–40°C to +85°C	8-Lead µSOIC	RM-8	HFA
AD8002ARM-REEL	–40°C to +85°C	8-Lead µSOIC 13" REEL	RM-8	HFA
AD8002ARM-REEL7	–40°C to +85°C	8-Lead µSOIC 7" REEL	RM-8	HFA

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8002 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

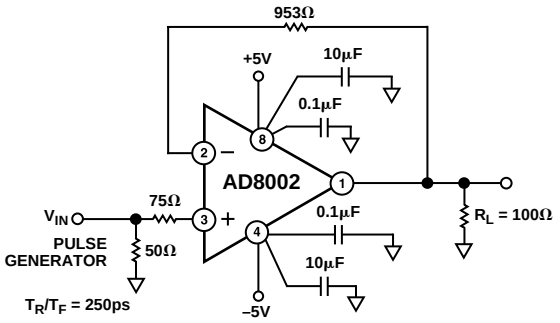


Figure 4. Test Circuit , Gain = +1

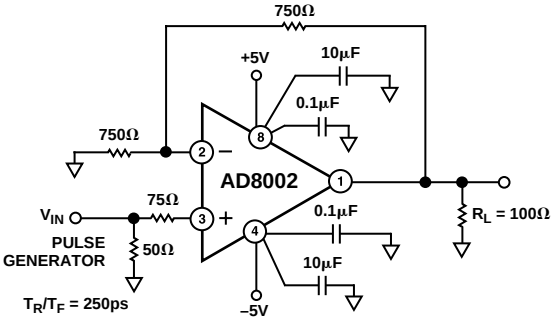


Figure 7. Test Circuit, Gain = +2

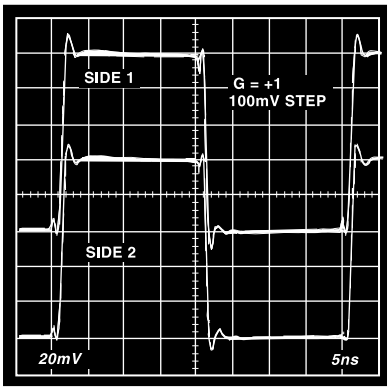


Figure 5. 100 mV Step Response, G = +1

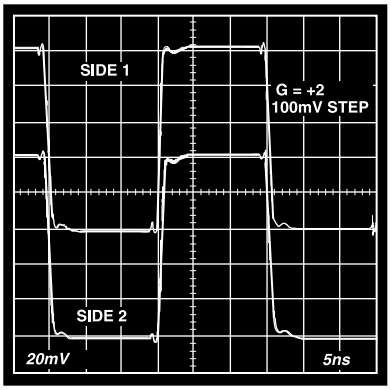


Figure 8. 100 mV Step Response, G = +2

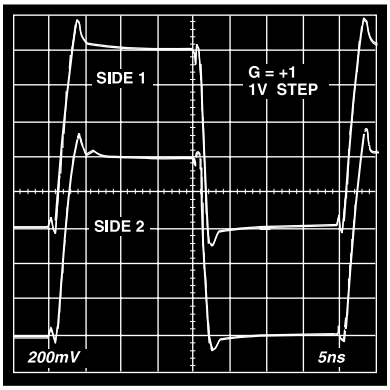


Figure 6. 1 V Step Response, G = +1

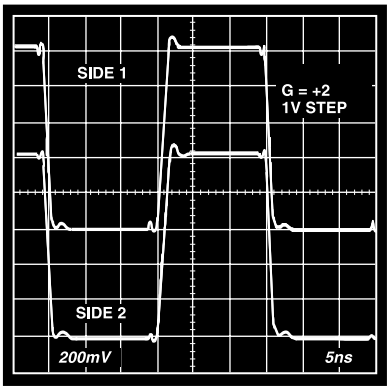


Figure 9. 1 V Step Response, G = +2

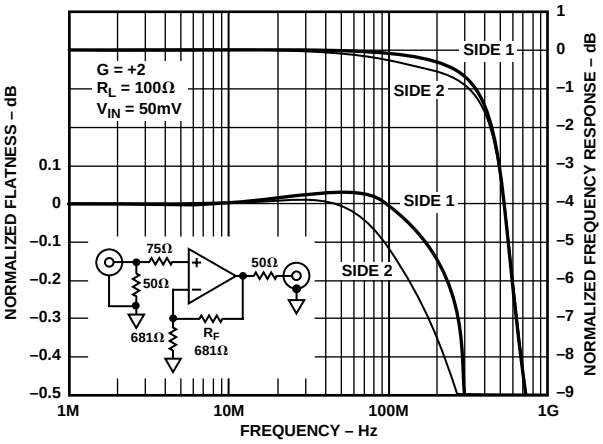


Figure 10. Frequency Response and Flatness, G = +2

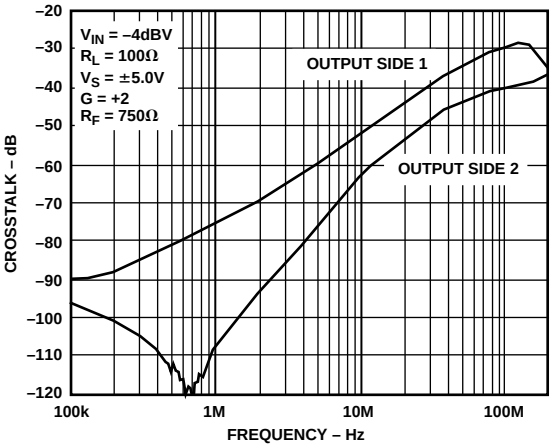


Figure 13. Crosstalk (Output-to-Output) vs. Frequency

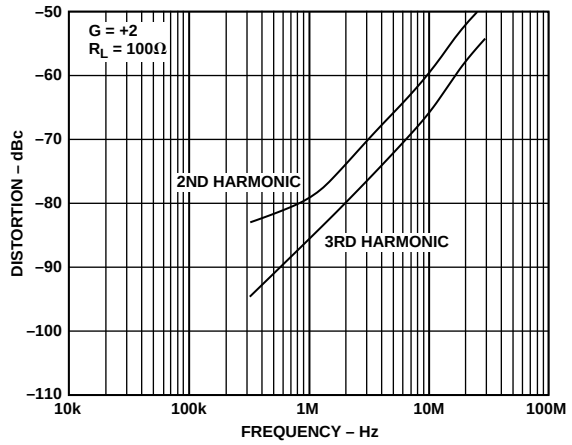
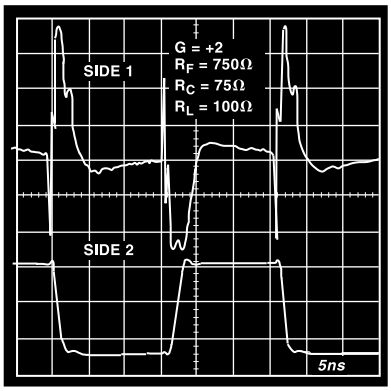


Figure 11. Distortion vs. Frequency, G = +2, R_L = 100 Ω



NOTES: SIDE 1: V_{IN} = 0V; 8mV/div RTO
SIDE 2: 1V STEP RTO; 400mV/div

Figure 14. Pulse Crosstalk, Worst Case, 1 V Step

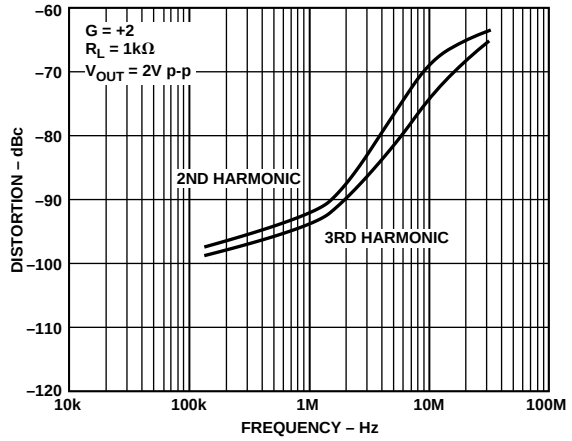


Figure 12. Distortion vs. Frequency, G = +2, R_L = 1 kΩ

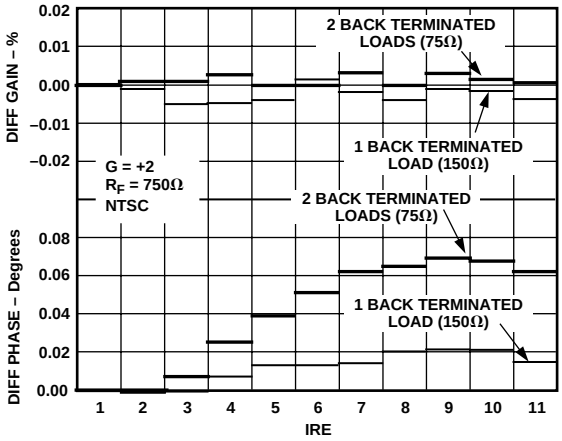


Figure 15. Differential Gain and Differential Phase (per Amplifier)

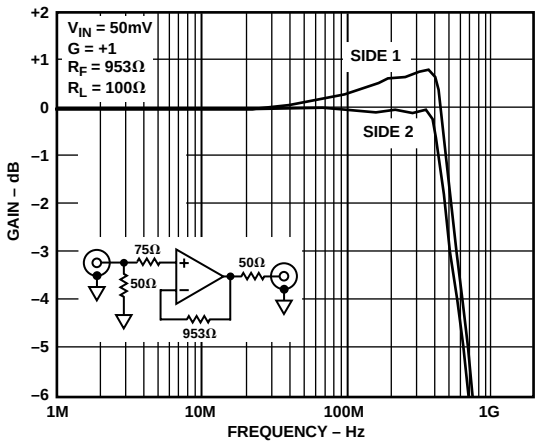


Figure 16. Frequency Response, G = +1

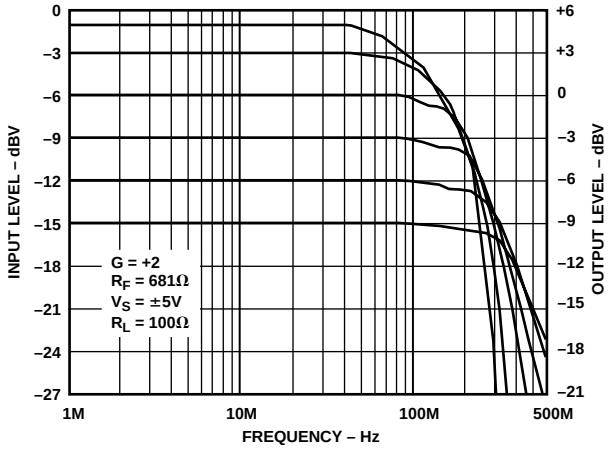


Figure 19. Large Signal Frequency Response, G = +2

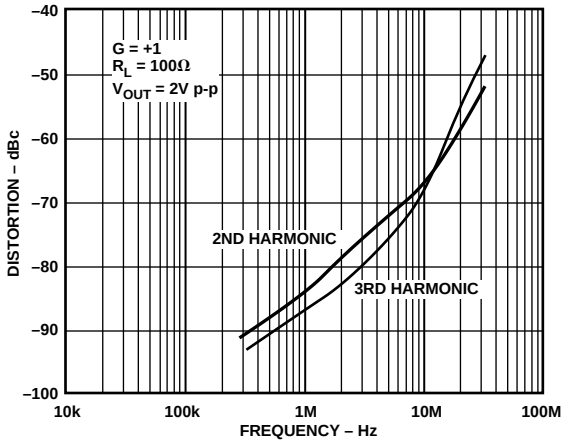


Figure 17. Distortion vs. Frequency, G = +1, R_L = 100 Ω

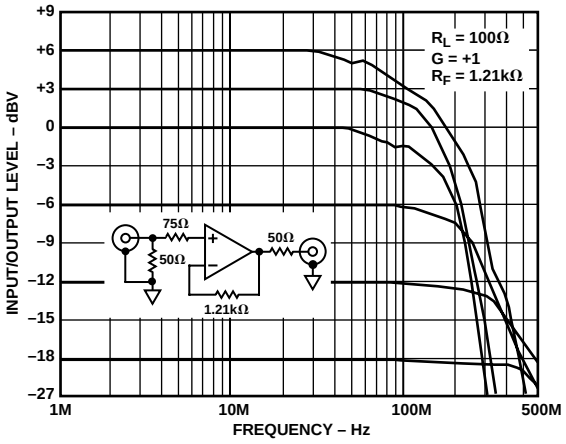


Figure 20. Large Signal Frequency Response, G = +1

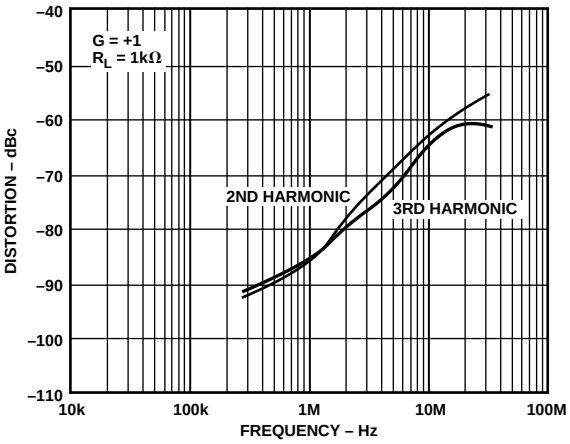


Figure 18. Distortion vs. Frequency, G = +1, R_L = 1 kΩ

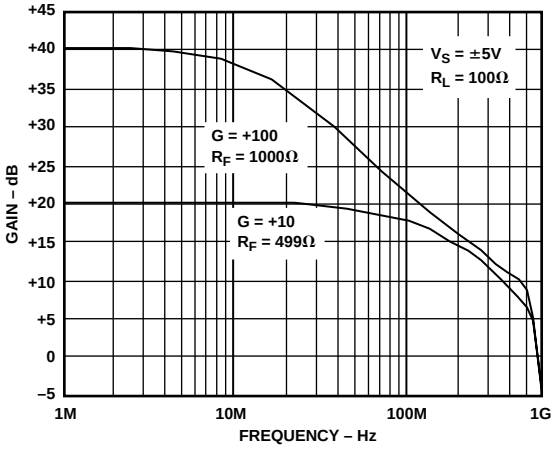


Figure 21. Frequency Response, G = +10, G = +100

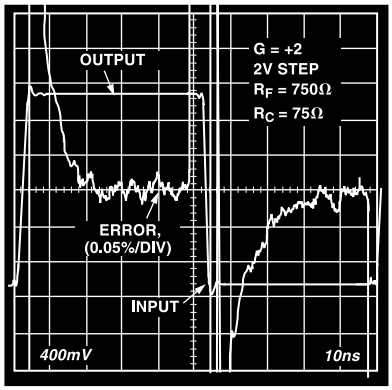


Figure 22. Short-Term Settling Time

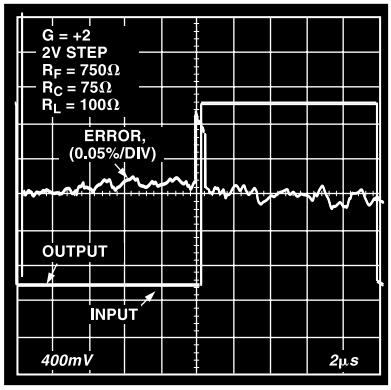


Figure 25. Long-Term Settling Time

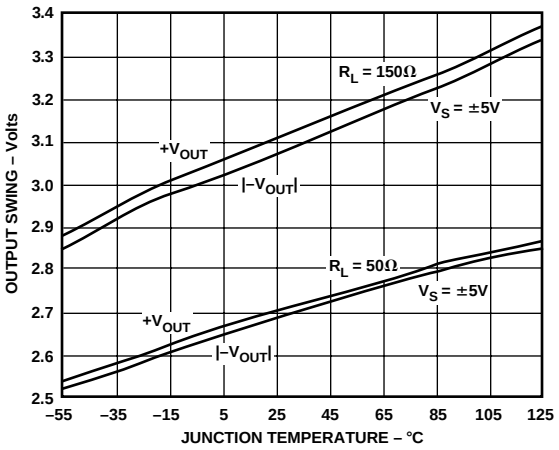


Figure 23. Output Swing vs. Temperature

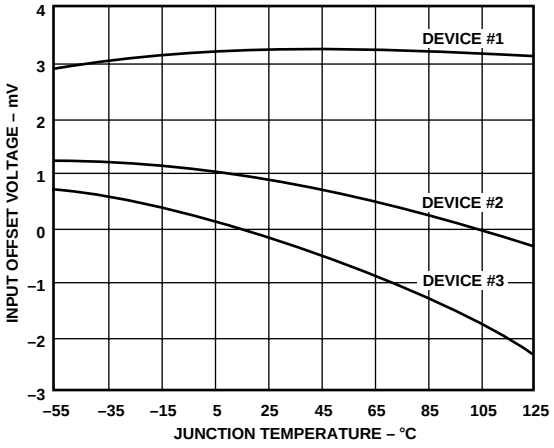


Figure 26. Input Offset Voltage vs. Temperature

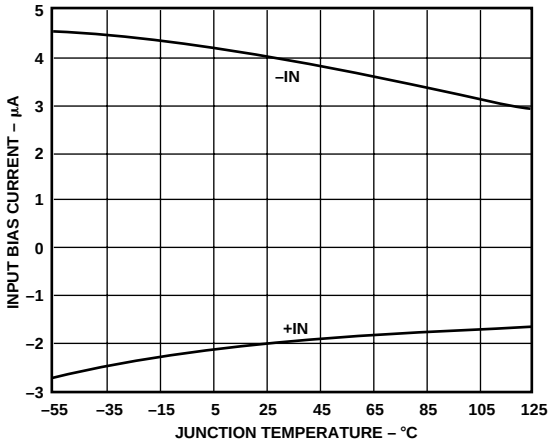


Figure 24. Input Bias Current vs. Temperature

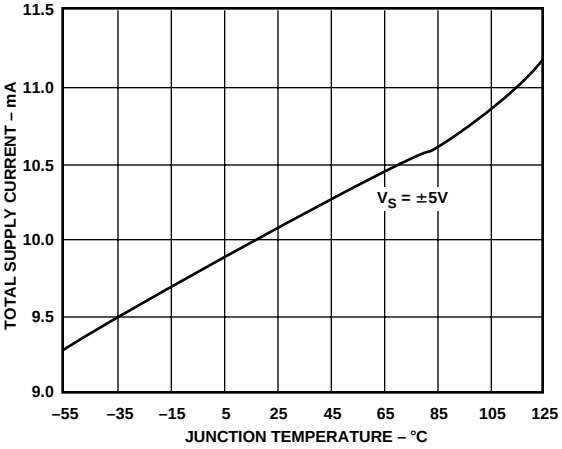


Figure 27. Total Supply Current vs. Temperature

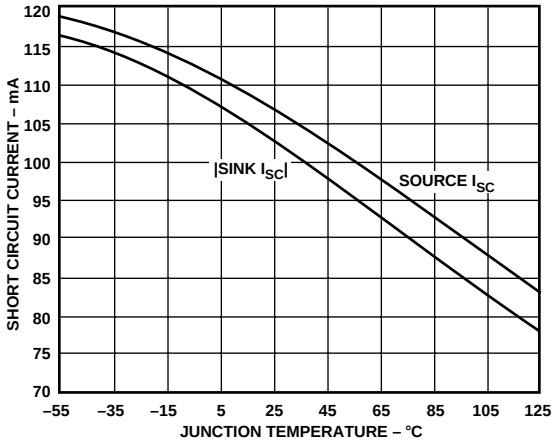


Figure 28. Short Circuit Current vs. Temperature

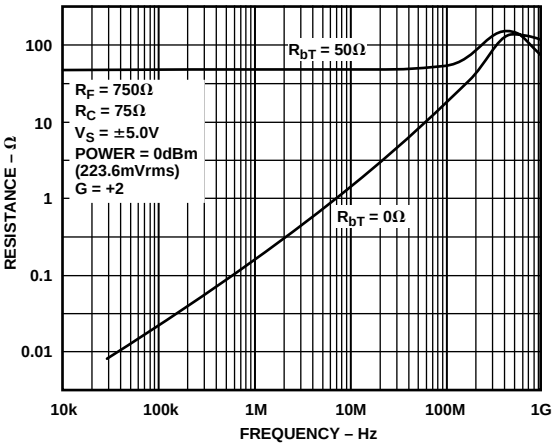


Figure 31. Output Resistance vs. Frequency

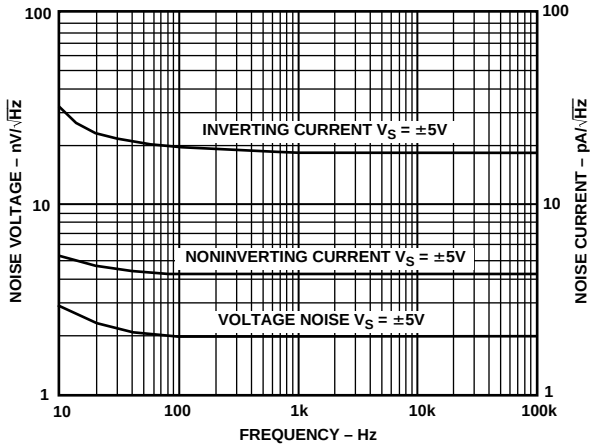


Figure 29. Noise vs. Frequency

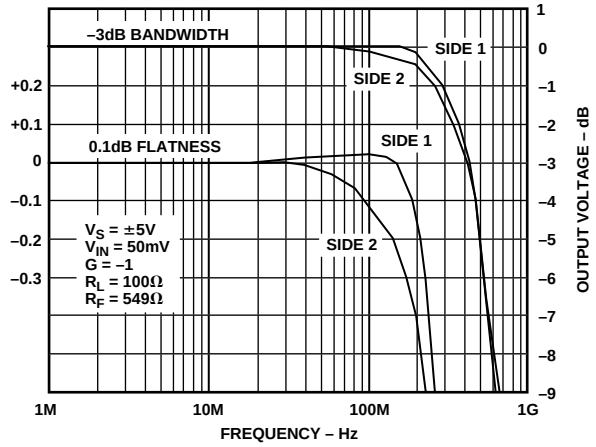


Figure 32. –3 dB Bandwidth vs. Frequency, G = –1

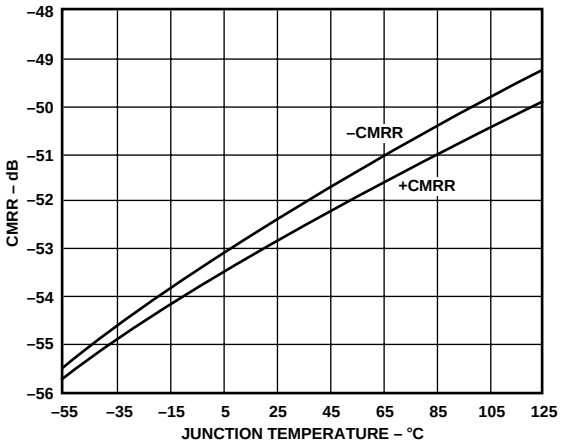


Figure 30. CMRR vs. Temperature

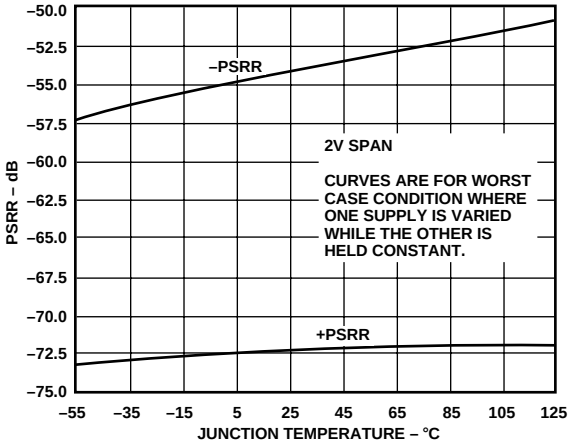


Figure 33. PSRR vs. Temperature

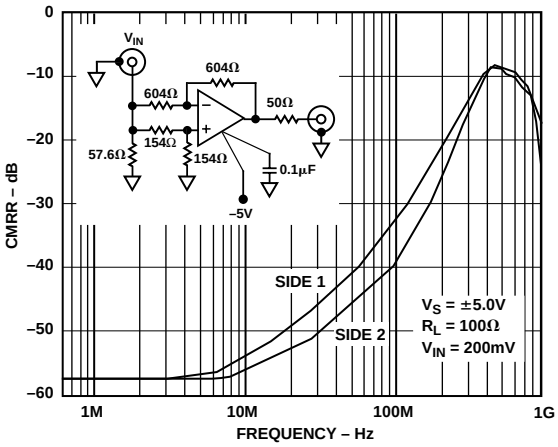


Figure 34. CMRR vs. Frequency

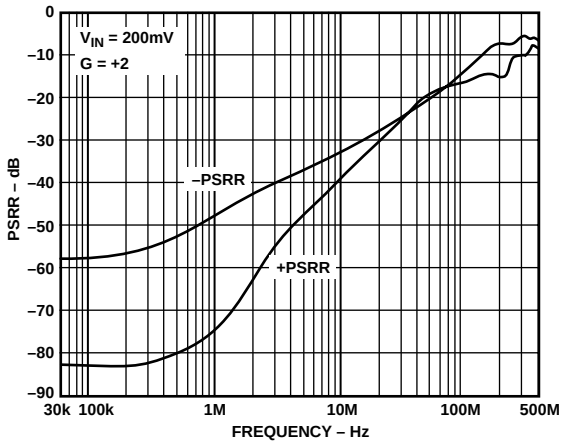


Figure 37. PSRR vs. Frequency

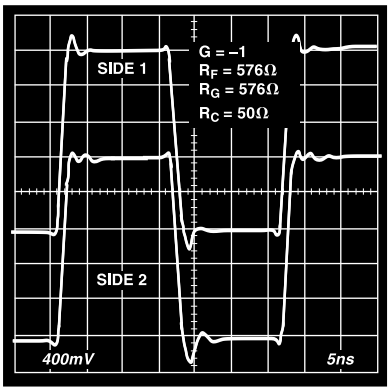


Figure 35. 2 V Step Response, G = –1

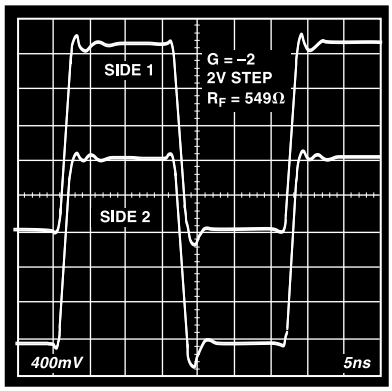


Figure 38. 2 V Step Response, G = –2

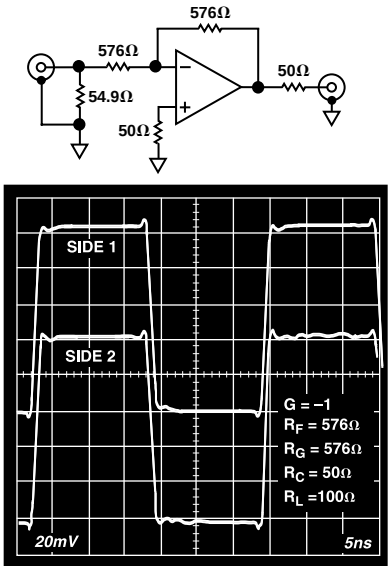


Figure 36. 100 mV Step Response, G = –1

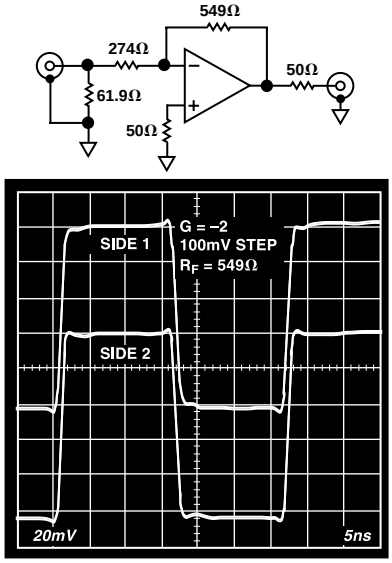


Figure 39. 100 mV Step Response, G = –2

THEORY OF OPERATION

A very simple analysis can put the operation of the AD8002, a current feedback amplifier, in familiar terms. Being a current feedback amplifier, the AD8002's open-loop behavior is expressed as transimpedance, $\Delta V_O/\Delta I_{-IN}$, or T_Z. The open-loop transimpedance behaves just as the open-loop voltage gain of a voltage feedback amplifier, that is, it has a large dc value and decreases at roughly 6 dB/octave in frequency.

Since the R_{IN} is proportional to $1/g_M$, the equivalent voltage gain is just $T_Z \times g_M$, where the g_M in question is the transconductance of the input stage. This results in a low open-loop input impedance at the inverting input, a now familiar result. Using this amplifier as a follower with gain, Figure 40, basic analysis yields the following result.

$$\frac{V_O}{V_{IN}} = G \times \frac{T_Z\ (S)}{T_Z\ (S) + G \times R_{IN} + R1}$$

$$G = 1 + \frac{R1}{R2} \quad R_{IN} = 1/g_M \approx 50\ \Omega$$

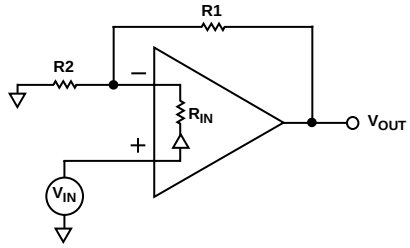


Figure 40.

Recognizing that $G \times R_{IN} << R1$ for low gains, it can be seen to the first order that bandwidth for this amplifier is independent of gain (G).

Considering that additional poles contribute excess phase at high frequencies, there is a minimum feedback resistance below which peaking or oscillation may result. This fact is used to determine the optimum feedback resistance, R_F. In practice parasitic capacitance at the inverting input terminal will also add phase in the feedback loop, so picking an optimum value for R_F can be difficult.

Achieving and maintaining gain flatness of better than 0.1 dB at frequencies above 10 MHz requires careful consideration of several issues.

Choice of Feedback and Gain Resistors

The fine scale gain flatness will, to some extent, vary with feedback resistance. It, therefore, is recommended that once optimum resistor values have been determined, 1% tolerance values should be used if it is desired to maintain flatness over a wide range of production lots. In addition, resistors of different construction have different associated parasitic capacitance and inductance. Surface mount resistors were used for the bulk of the characterization for this data sheet. It is not recommended that leaded components be used with the AD8002.

Printed Circuit Board Layout Considerations

As to be expected for a wideband amplifier, PC board parasitics can affect the overall closed-loop performance. Of concern are stray capacitances at the output and the inverting input nodes. If a ground plane is to be used on the same side of the board as the signal traces, a space (5 mm min) should be left around the signal lines to minimize coupling. Additionally, signal lines connecting the feedback and gain resistors should be short enough so that their associated inductance does not cause high frequency gain errors. Line lengths on the order of less than 5 mm are recommended. If long runs of coaxial cable are being driven, dispersion and loss must be considered.

Power Supply Bypassing

Adequate power supply bypassing can be critical when optimizing the performance of a high frequency circuit. Inductance in the power supply leads can form resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to the load, then bypass capacitors (typically greater than 1 µF) will be required to provide the best settling time and lowest distortion. A parallel combination of 4.7 µF and 0.1 µF is recommended. Some brands of electrolytic capacitors will require a small series damping resistor ≈4.7 Ω for optimum results.

DC Errors and Noise

There are three major noise and offset terms to consider in a current feedback amplifier. For offset errors refer to the equation below. For noise error the terms are root-sum-squared to give a net output error. In the circuit below (Figure 41) they are input offset (V_{IO}) which appears at the output multiplied by the noise gain of the circuit ($1 + R_F/R_I$), noninverting input current ($I_{BN} \times R_N$) also multiplied by the noise gain, and the inverting input current, which when divided between R_F and R_I and subsequently multiplied by the noise gain always appears at the output as $I_{BN} \times R_F$. The input voltage noise of the AD8002 is a low 2 nV/$\sqrt{\text{Hz}}$. At low gains though the inverting input current noise times R_F is the dominant noise source. Careful layout and device matching contribute to better offset and drift specifications for the AD8002 compared to many other current feedback amplifiers. The typical performance curves in conjunction with the equations below can be used to predict the performance of the AD8002 in any application.

$$V_{OUT} = V_{IO} \times \left(1 + \frac{R_F}{R_I}\right) \pm I_{BN} \times R_N \times \left(1 + \frac{R_F}{R_I}\right) \pm I_{BI} \times R_F$$

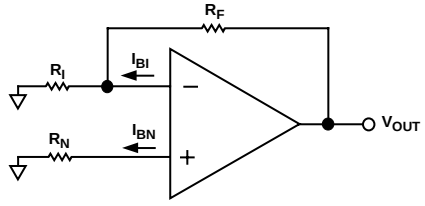


Figure 41. Output Offset Voltage

Driving Capacitive Loads

The AD8002 was designed primarily to drive nonreactive loads. If driving loads with a capacitive component is desired, best frequency response is obtained by the addition of a small series resistance as shown in Figure 42. The accompanying graph

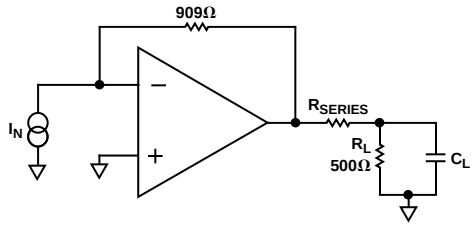


Figure 42. Driving Capacitive Loads

shows the optimum value for R_{SERIES} vs. capacitive load. It is worth noting that the frequency response of the circuit when driving large capacitive loads will be dominated by the passive roll-off of R_{SERIES} and C_L.

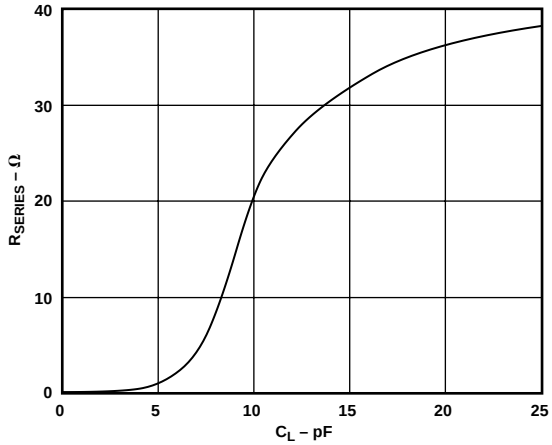


Figure 43. Recommended R_{SERIES} vs. Capacitive Load

Communications

Distortion is a key specification in communications applications. Intermodulation distortion (IMD) is a measure of the ability of an amplifier to pass complex signals without the generation of spurious harmonics. The third order products are usually the most problematic since several of them fall near the fundamentals and do not lend themselves to filtering. Theory predicts that the third order harmonic distortion components increase in power at three times the rate of the fundamental tones. The specification of third order intercept as the virtual point where fundamental and harmonic power are equal is one standard measure of distortion performance. Op amps used in closed-loop applications do not always obey this simple theory. At a gain of two, the AD8002 has performance summarized in Figure 44. Here the worst third order products are plotted vs. input power. The third order intercept of the AD8002 is +33 dBm at 10 MHz.

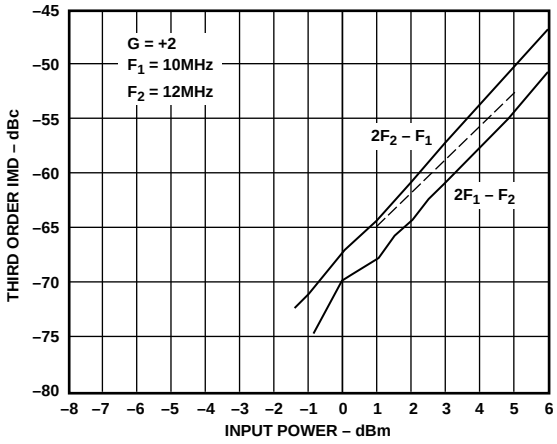


Figure 44. Third Order IMD; F_1 = 10 MHz, F_2 = 12 MHz

Operation as a Video Line Driver

The AD8002 has been designed to offer outstanding performance as a video line driver. The important specifications of differential gain (0.01%) and differential phase (0.02°) meet the most exacting HDTV demands for driving one video load with each amplifier. The AD8002 also drives four back terminated loads (two each), as shown in Figure 45, with equally impressive performance (0.01%, 0.07°). Another important consideration is isolation between loads in a multiple load application. The AD8002 has more than 40 dB of isolation at 5 MHz when driving two 75 Ω back terminated loads.

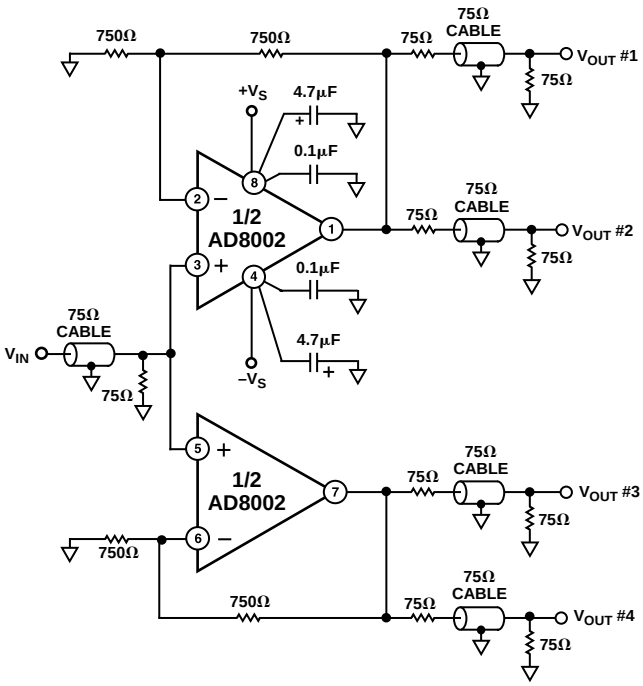


Figure 45. Video Line Driver

Driving A-to-D Converters

The AD8002 is well suited for driving high speed analog-to-digital converters such as the AD9058. The AD9058 is a dual 8-bit 50 MSPS ADC. In the circuit below the AD8002 is shown driving the inputs of the AD9058 which are configured for 0 V to +2 V ranges. Bipolar input signals are buffered, amplified (–2×), and offset (by +1.0 V) into the proper input range of the ADC. Using the AD9058's internal +2 V reference connected to both ADCs as shown in Figure 46 reduces the number of external components required to create a complete data acquisition system. The 20 Ω resistors in series with ADC inputs are used to help the AD8002s drive the 10 pF ADC input capacitance. The AD8002 only adds 100 mW to the power consumption while not limiting the performance of the circuit.

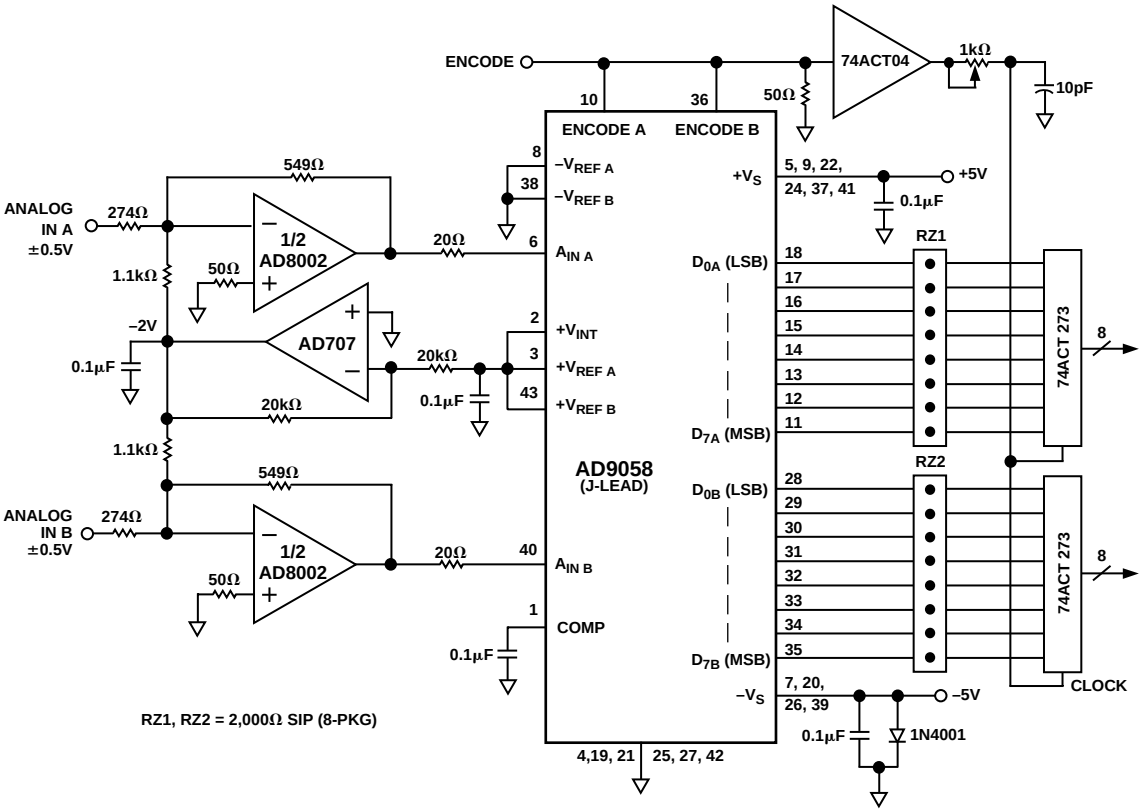


Figure 46. AD8002 Driving a Dual A-to-D Converter

Single-Ended to Differential Driver Using an AD8002

The two halves of an AD8002 can be configured to create a single-ended to differential high speed driver with a –3 dB bandwidth in excess of 200 MHz as shown in Figure 47. Although the individual op amps are each current feedback, the overall architecture yields a circuit with attributes normally associated with voltage feedback amplifiers, while offering the speed advantages inherent in current feedback amplifiers. In addition, the gain of the circuit can be changed by varying a single resistor, R_F, which is often not possible in a dual op amp differential driver.

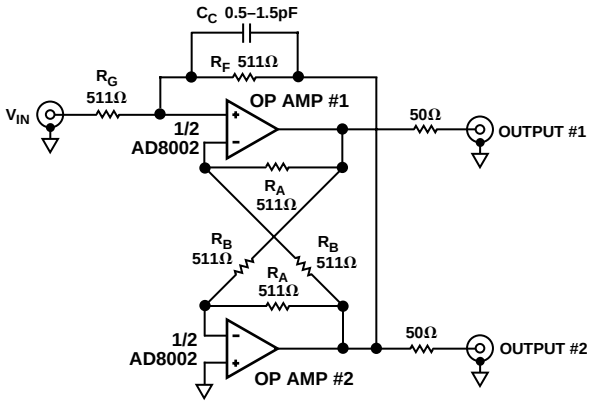


Figure 47. Differential Line Driver

The current feedback nature of the op amps, in addition to enabling the wide bandwidth, provides an output drive of more than 3 V p-p into a 20 Ω load for each output at 20 MHz. On the other hand, the voltage feedback nature provides symmetrical high impedance inputs and allows the use of reactive components in the feedback network.

The circuit consists of the two op amps each configured as a unity gain follower by the 511 Ω R_A feedback resistors between each op amp's output and inverting input. The output of each op amp has a 511 Ω R_B resistor to the inverting input of the other op amp. Thus, each output drives the other op amp through a unity gain inverter configuration. By connecting the two amplifiers as cross-coupled inverters, their outputs are freed to be equal and opposite, assuring zero-output common-mode voltage.

With this circuit configuration, the common-mode signal of the outputs is reduced. If one output moves slightly higher, the negative input to the other op amp drives its output to go slightly lower and thus preserves the symmetry of the complementary outputs which reduces the common-mode signal. The common-mode output signal was measured to be –50 dB at 1 MHz.

Looking at this configuration overall, there are two high impedance inputs (the + inputs of each op amp), two low impedance outputs and high open loop gain. If we consider the two noninverting inputs and just the output of Op Amp #2, the structure looks like a voltage feedback op amp having two symmetrical, high impedance inputs and one output. The +input to Op Amp #2 is the noninverting input (it has the same polarity as Output #2) and the +input to Amplifier #1 is the inverting input (opposite polarity of Output #2).

With a feedback resistor R_F, an input resistor R_G, and grounding of the +input of Op Amp #2, a feedback amplifier is formed. This configuration is just like a voltage feedback amplifier in an inverting configuration if only Output #2 is considered. The addition of Output #1 makes the amplifier differential output.

The differential gain of this circuit is:

$$G = \frac{R_F}{R_G} \times \left(1 + \frac{R_A}{R_B}\right)$$

The R_F/R_G term is the gain of the overall op amp configuration and is the same as for an inverting op amp except for the polarity. If Output #1 is used as the output reference, then the gain is positive. The $1+R_A/R_B$ term is the noise gain of each individual op amp in its noninverting configuration.

The resulting architecture offers several advantages. First, the gain can be changed by changing a single resistor. Changing either R_F or R_G will change the gain as in an inverting op amp circuit. For most types of differential circuits, more than one resistor must be changed to change gain and still maintain good CMR.

Reactive elements can be used in the feedback network. This is in contrast to current feedback amplifiers that restrict the use of reactive elements in the feedback. The circuit described requires about 0.9 pF of capacitance in shunt across R_F in order to optimize peaking and realize a –3 dB bandwidth of more than 200 MHz.

The peaking exhibited by the circuit is very sensitive to the value of this capacitor. Parasitics in the board layout on the order of tenths of picofarads will influence the frequency response and the value required for the feedback capacitor, so a good layout is essential.

The shunt capacitor type selection is also critical. A good microwave type chip capacitor with high Q was found to yield best performance. The part selected for this circuit was a muRata Erie part no. MA280R9B.

The distortion was measured at 20 MHz with a 3 V p-p input and a 100 Ω load on each output. For Output #1 the distortion is –37 dBc and –41 dBc for the second and third harmonics respectively. For Output #2 the second harmonic is –35 dBc and the third harmonic is –43 dBc.

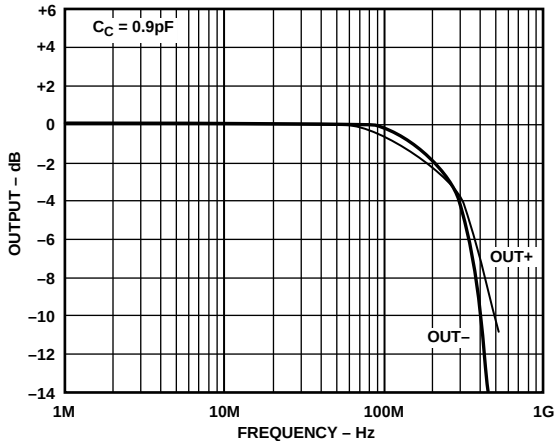


Figure 48. Differential Driver Frequency Response

Layout Considerations

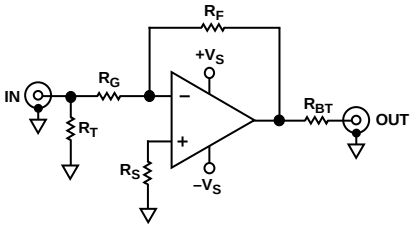
The specified high speed performance of the AD8002 requires careful attention to board layout and component selection. Proper R_F design techniques and low parasitic component selection are mandatory.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance ground path. The ground plane should be removed from the area near the input pins to reduce stray capacitance.

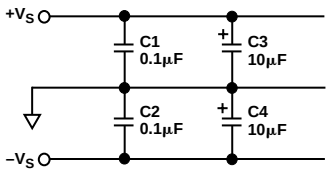
Chip capacitors should be used for supply bypassing (see Figure 49). One end should be connected to the ground plane and the other within 1/8 in. of each power pin. An additional large (4.7 μF–10 μF) tantalum electrolytic capacitor should be connected in parallel, but not necessarily so close, to supply current for fast, large-signal changes at the output.

The feedback resistor should be located close to the inverting input pin in order to keep the stray capacitance at this node to a minimum. Capacitance variations of less than 1 pF at the inverting input will significantly affect high speed performance.

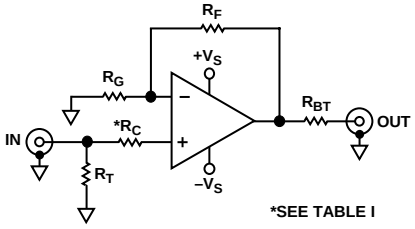
Stripline design techniques should be used for long signal traces (greater than about 1 in.). These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end.



Inverting Configuration



Supply Bypassing



Noninverting Configuration

Figure 49. Inverting and Noninverting Configurations

Table I. Recommended Component Values

	AD8002AN (DIP) Gain							AD8002AR (SOIC) Gain						
Component	**–10**	**–2**	**–1**	**+1**	**+2**	**+10**	**+100**	**–10**	**–2**	**–1**	**+1**	**+2**	**+10**	**+100**
R_F (Ω)	499	549	576	1210	750	499	1000	499	499	549	953	681	499	1000
R_G (Ω)	49.9	274	576	–	750	54.9	10	49.9	249	549	–	681	54.9	10
R_{BT} (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_C (Ω)*				75	75	0	0				75	75	0	0
R_S(Ω)	49.9	49.9	49.9					49.9	49.9	49.9				
R_T (Nominal) (Ω)	–	61.9	54.9	49.9	49.9	49.9	49.9	–	61.9	54.9	49.9	49.9	49.9	49.9
Small Signal BW (MHz)	270	380	410	600	500	170	17	250	410	410	600	500	170	17
0.1 dB Flatness (MHz)	45	80	130	35	60	24	3	50	100	100	35	90	24	3

	AD8002ARM (μSOIC) Gain						
Component	**–10**	**–2**	**–1**	**+1**	**+2**	**+10**	**+100**
R_F (Ω)	499	499	590	1000	681	499	1000
R_G (Ω)	49.9	249	590	–	681	54.9	10
R_{BT} (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_C (Ω)*				75	75	0	0
R_S(Ω)	49.9	49.9	49.9				
R_T (Nominal) (Ω)	–	61.9	49.9	49.9	49.9	49.9	49.9
Small Signal BW (MHz)	270	400	410	600	450	170	19
0.1 dB Flatness (MHz)	60	100	100	35	70	35	3

*R_C is recommended to reduce peaking and minimizes input reflections at frequencies above 300 MHz. However, R_C is not required.

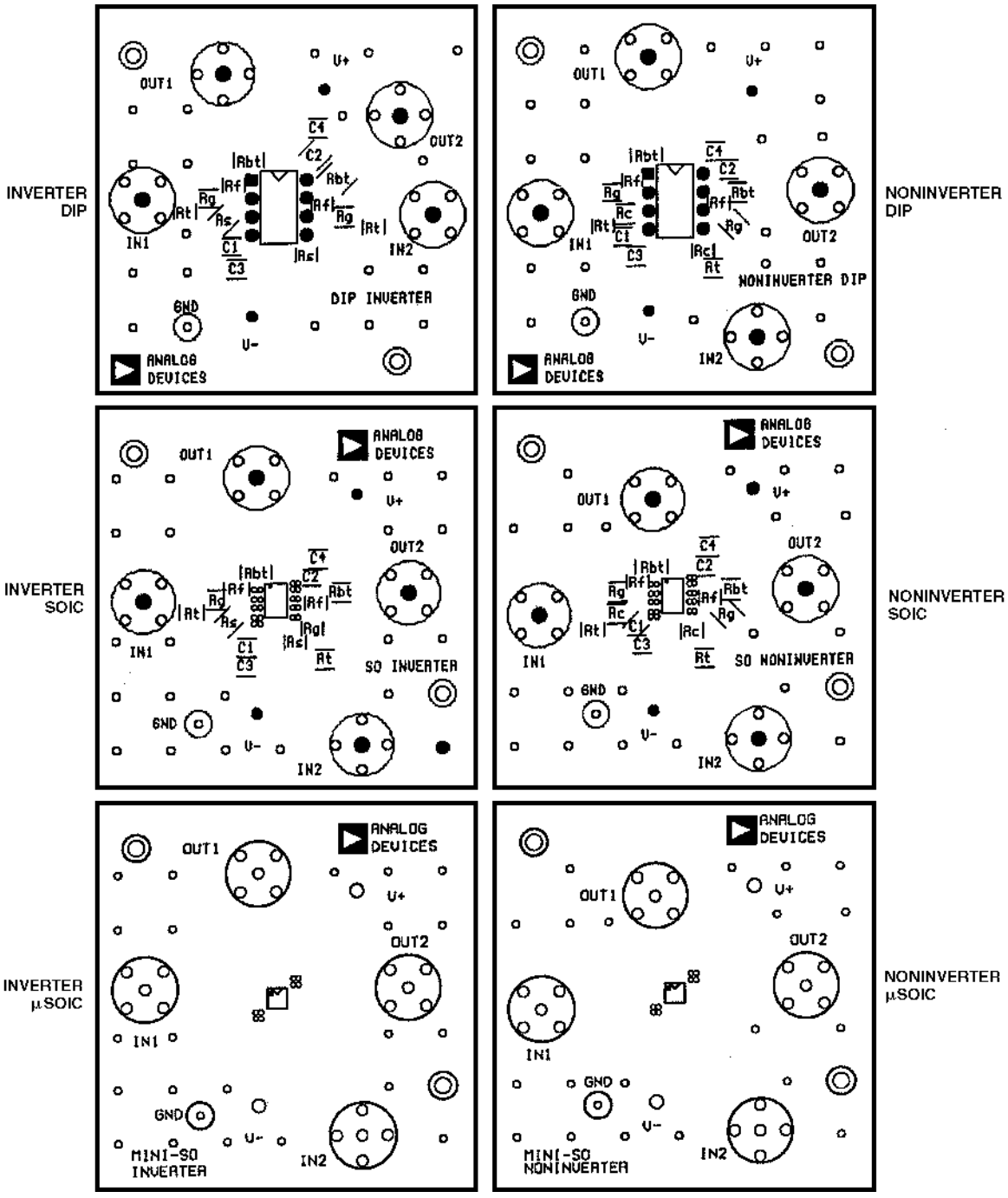


Figure 50. Board Layout (Silkscreen)

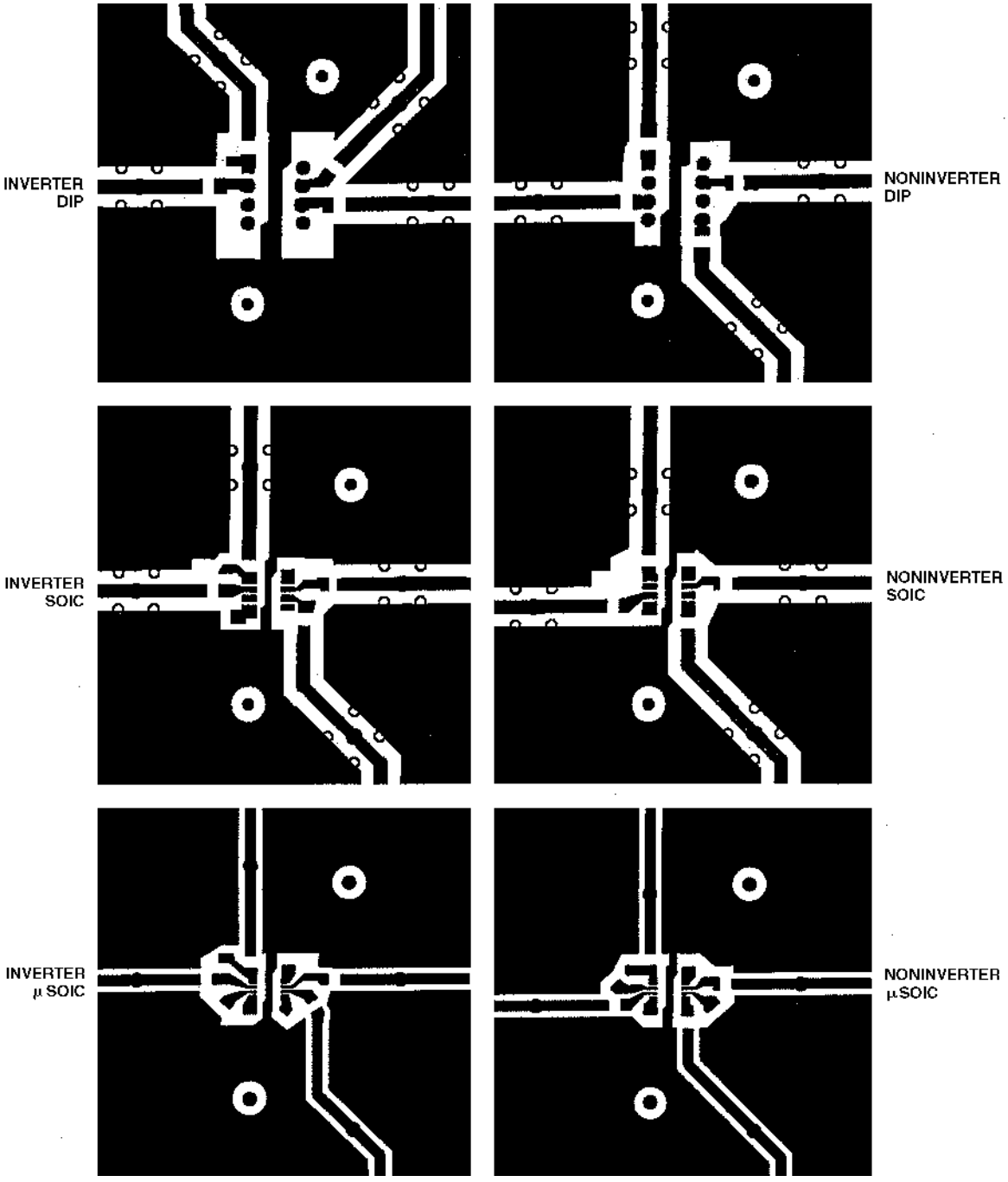


Figure 51. Board Layout (Component Layer)

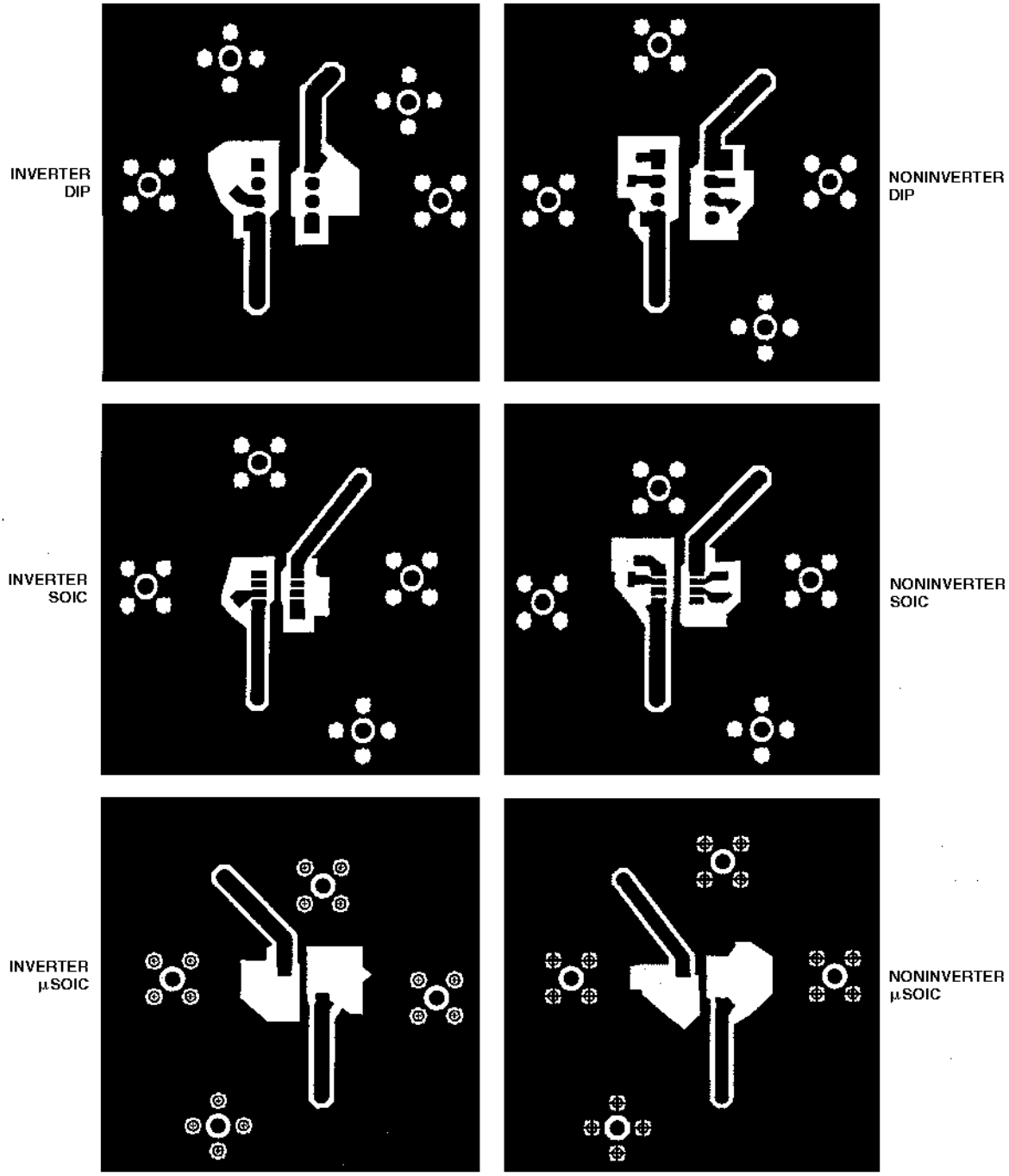
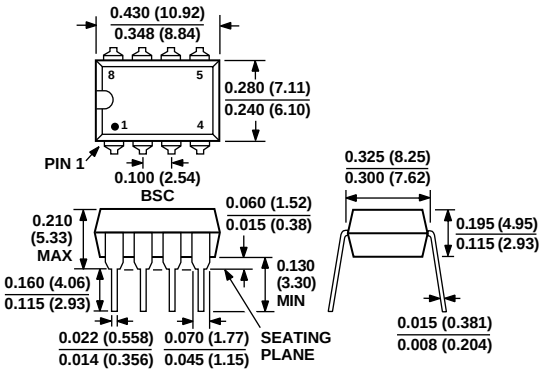


Figure 52. Board Layout (Solder Side) (Looking Through the Board)

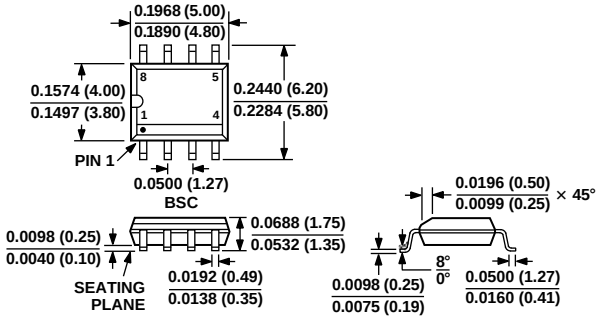
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

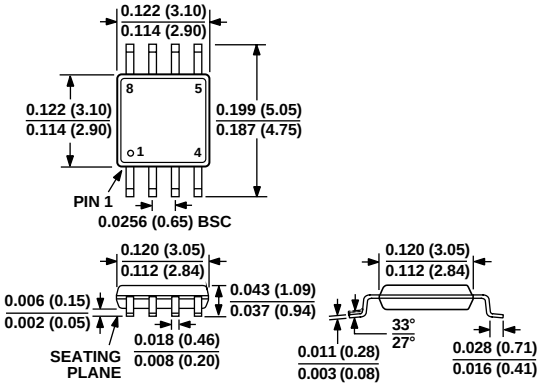
8-Lead Plastic DIP (N-8)



8-Lead SOIC (SO-8)



8-Lead μSOIC (RM-8)



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