16-Bit Sigma-Delta ADC with Programmable Post Processor

Preliminary Technical Data — AD7725

FEATURES

Programmable Signal Conditioning
- **LowPass**
- **HighPass**
- **BandStop**
- **BandPass**

Programmable Decimation, Interpolation and Output Word Rate

Flexible Programming Modes
- **Boot ROM**
- **External EEPROM**
- **Parallel/Serial Interface**

19.2 MHz Master Clock Frequency

0 to +4V or ±2V Input Range

Power Supplies: AVDD, DVDD: +5V ± 5%

On-Chip 2.5V Voltage Reference

44-Pin PQFP

GENERAL DESCRIPTION

The AD7725 is a complete 16-bit, sigma delta converter with on chip user-programmable signal conditioning. The output of the modulator is processed by three cascaded finite impulse response (FIR) filters. This is followed by a user-programmable post processor. The user has complete control over the filter response (lowpass, highpass, bandpass, stopband), the filter coefficients, the decimation ratio. The post processor accepts up to 108 coefficients.

The AD7725 provides 16-bit performance for input bandwidths up to 460 kHz and an output word rate of 1.2 MHz maximum. The input sample rate is set either by the crystal oscillator or an external clock. The output is available via a serial or parallel interface.

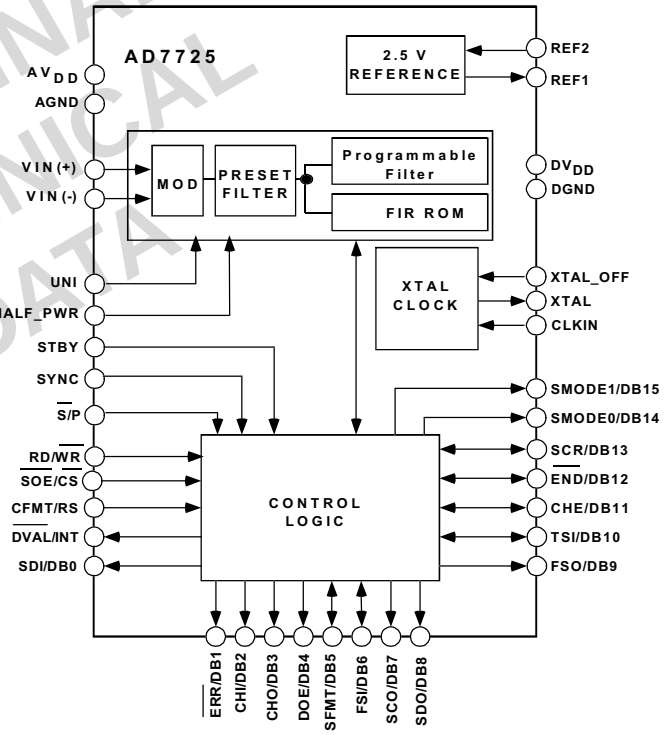
The device contains Systolix's PulseDSP* post processor which permits the signal conditioning characteristics to be programmed through the parallel microprocessor interface, through a serial interface or, it may boot at power-on-reset from its internal ROM or from an external serial EPROM.

The post processor is a fully programmable core which provides processing power of up to 130 million accumulates (MAC) per second. To program the post processor, the user must produce a configuration file which contains the programming data for the intended function. This file is generated by a compiler which is available from Analog Devices. The AD7725 compiler accepts filter coefficient data as an input and automatically generate the required device programming data.

The part provides an accurate on-chip 2.5V reference for the modulator. A reference input/output function is provided to allow either the internal reference or an external system reference to be used as the reference source for the modulator.

The device is offered in a 44-pin PQFP package and is designed to operate from -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



*PulseDSP is a Trademark of Systolix

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

Prelim E1 2/00

SPECIFICATIONS[1]

(AV_{DD} = +5V ± 5%; AGND = AGND1= AGND2 = DGND = 0V;
F_{CLKIN} = 19.2 MHz; REF2 = 2.5 V; T_A = T_{MIN} to T_{MAX}; unless otherwise noted)

Parameter	Test Conditions/Comments	Min	B Version Typ	Max	Units
DYNAMIC SPECIFICATIONS[2]	HALF_PWR = 0 or 1 f_{CLKIN} = 10MHz when HALF_PWR = 1				
ROM FIR					
Bipolar Mode					
Signal to Noise[3]	Measurement Bandwidth = 0.383*F_O				
	2.5V Reference	82	86		dB
	3V Reference	83	87		-90
Signal to Noise[3]	Measurement Bandwidth = 0.5*F_O	78	81.5		dB
Total Harmonic Distortion[3]	2.5V Reference			-88	dB
	3V Reference			-86	dB
Spurious Free Dynamic Range	2.5V Reference			-90	dB
	3V Reference			-88	dB
Unipolar Mode					
Signal to Noise[3]	Measurement Bandwidth = 0.383*F_O		84		dB
Signal to Noise[3]	Measurement Bandwidth = 0.5*F_O		81		dB
Total Harmonic Distortion[3]			-89		dB
DIGITAL FILTER RESPONSE					
PRESET FIR					
Data Output Rate				MCLK/8	
StopBand Attenuation		70			dB
LowPass Corner Frequency			MCLK/16		
Group Delay			133/2F_{CLKIN}		
Settling Time			133/F_{CLKIN}		
ROM FIR					
0 kHz to F_{CLKIN}/83.5				± 0.001	dB
F_{CLKIN}/66.9		-3			dB
F_{CLKIN}/64		-6			dB
F_{CLKIN}/51.9 to F_{CLKIN}/2				-90	dB
Group Delay			1293/2F_{CLKIN}		
Settling Time			1293/F_{CLKIN}		
Output Data Rate, F_O			F_{CLKIN}/32		
POST PROCESSOR CHARACTERISTICS					
Input Data Rate				MCLK/8	
Coefficient Precision			24		Bits
Arithmetic Precision			30		Bits
No. of Taps Permitted				108	
Decimation Factor		2		256	
No. of Decimation Stages		1		5	
Output data Rate				MCLK/16	

AD7725–SPECIFICATIONS[1]

(AV_{DD} = +5V ± 5%; AGND = AGND1= AGND2 = DGND = 0V; F_{CLKIN} = 19.2 MHz; REF2 = 2.5 V; T_A = T_{MIN} to T_{MAX}; unless otherwise noted)

Parameter	Test Conditions/Comments	Min	Typ	Max	Units
ANALOG INPUTS					
Full Scale Input Span	VIN(+) - VIN(-)				
Bipolar Mode		±4/5*V_{REF2}	V		
Unipolar Mode		0		8/5*V_{REF2}	V
Absolute Input Voltage	VIN (+) and/or VIN (-)	AGND		AVDD	V
Input Sampling Capacitance			2		pF
Input Sampling Rate,F_{CLKIN}				19.2	MHz
CLOCK					
CLKIN Duty Ratio		45		55	%
REFERENCE					
REF1 Output Resistance			3		kW
Reference Buffer					
Offset Voltage	Offset between REF1 and REF2		± 10		mV
Using Internal Reference					
REF2 Output Voltage		2.39	2.54	2.69	V
REF2 Output Voltage Drift			60		ppm/°C
Using External Reference					
REF2 Input Impedance	REF1 = AGND				kW
REF2 External Voltage Range		1.2	2.5	3.15	V
STATIC PERFORMANCE					
Resolution		16			Bits
Differential NonLinearity	Guaranteed Monotonic		±0.5	±1	LSB
Integral NonLinearity			±2		LSB
DC CMRR		80			dB
Offset Error					
Bipolar Mode			±5		mV
Unipolar Mode			±25		mV
Gain Error[3,4]			± 0.5		%FSR
LOGIC INPUTS (Excluding CLKIN)					
V_{INH}, Input High Voltage		2.0			V
V_{INL}, Input Low Voltage				0.8	V
CLOCK INPUT (CLKIN)					
V_{INH}, Input High Voltage		3.8			V
V_{INL}, Input Low Voltage				0.4	V
ALL LOGIC INPUTS					
I_{IN}, Input Current	V_{IN} = 0 V to DV_{DD}			± 10	mA
C_{IN}, Input Capacitance				10	pF
LOGIC OUTPUTS					
V_{OH}, Output High Voltage	$\|I_{OUT}\|$ = 200 mA	4.0			V
V_{OL}, Output Low Voltage	$\|I_{OUT}\|$ = 1.6 mA			0.4	V
POWER SUPPLIES					
AV_{DD}		4.75		5.25	V
I_{AVDD}	HALF_PWR = Logic Low		50	65	mA
	HALF_PWR = Logic High		25	33	mA
DV_{DD}		4.75		5.25	V
I_{DVDD}	HALF_PWR = Logic Low		20	35	mA
	HALF_PWR = Logic High		15	20	mA
Power Consumption	Standby Mode			200	mW

NOTES

[1]Operating Temperature Range is as follows: B Version: -40°C to +85°C

[2]Measurement Bandwidth = 0.5*F_O

[3]When using the internal reference, THD and Signal to (Noise + Distortion) specifications apply only to input signals above 10kHz with a 10mF decoupling capacitor between REF2 and AGND2. At frequencies below 10kHz, THD degrades to 84 dB.

Specifications subject to change without notice.

TIMING SPECIFICATIONS

(AVDD = +5 V ± 5%; DVDD = +5 V ± 5%; AGND = DGND = 0 V, REF2 = +2.5 V unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units
CLKIN Frequency	f_{CLK}	1		20	MHz
CLKIN Period (t_{CLK} = 1/f_{CLK})	t_1	0.05		1	ms
CLKIN Low Pulsewidth	t_2	0.45 x t_1		0.55 x t_1	
CLKIN High Pulsewidth	t_3	0.45 x t_1		0.55 x t_1	
CLKIN Rise Time	t_4	5			ns
CLKIN Fall Time	t_5	5			ns
CLKIN to SCO Delay	t_6		25	40	ns
SCO Period[2]: SCR = 1	t_7		2		t_{CLK}
SCR = 0	t_7		1		t_{CLK}
Serial Interface (DSP and ROM Modes)					
FSI Setup Time Before SCO Transition	t_8	20			ns
FSI Hold Time After SCO Transition	t_9	0			ns
SDI Setup Time	t_{10}	20			ns
SDI Hold Time	t_{11}	0			ns
Serial Interface (DSP Mode Only)					
SCO Transition to FSO High Delay	t_{12}	5		10	ns
SCO Transition to FSO Low Delay	t_{13}	5		10	ns
SDO Setup Before SCO Transition	t_{14}	5		10	ns
SDO Holf After SCO Transition	t_{15}	5		10	ns
Serial Interface (EPROM Mode)					
SCO High Time	t_{16}			8	t_{CLK}
SCO Low Time	t_{17}			8	t_{CLK}
SOE Low to First SCO Rising Edge	t_{18}			20	t_{CLK}
Data Setup Before SCO Rising Edge	t_{19}	10			ns
Parallel Interface					
Data Write					
RS High to $\overline{CS}$ Low	t_{20}	5			ns
$\overline{WR}$ Setup Before $\overline{CS}$ Low	t_{21}	5			ns
RS Hold After $\overline{CS}$ Rising Edge	t_{22}	5			ns
$\overline{CS}$ Pulse Width	t_{23}	10			ns
$\overline{WR}$ Hold After $\overline{CS}$ Rising Edge	t_{24}	5			ns
Data Setup time	t_{25}	15			ns
Data Hold Time	t_{26}	0			ns
Data Read					
RS High to $\overline{CS}$ Low	t_{27}	5			ns
RS Setup Before $\overline{CS}$ Low	t_{28}	5			ns
RS Hold After $\overline{CS}$ Rising Edge	t_{29}	5			ns
RD Hold After $\overline{CS}$ Rising Edge	t_{30}	5			ns
Data Valid After INT High	t_{31}			0	ns
Data Hold After $\overline{CS}$ Rising Edge	t_{32}	5			ns
Status Read/Instruction Write					
$\overline{CS}$ Duty Cycle	t_{33}	1			t_{CLK}
Interrupt Clear After $\overline{CS}$ Low	t_{34}			5	ns
RD Setup to $\overline{CS}$ Low	t_{35}	0			ns
RD Hold After $\overline{CS}$ Rising Edge	t_{36}			5	ns
Read Data Access Time	t_{37}			5	ns
Read Data Hold After $\overline{CS}$ Rising Edge	t_{38}	5			ns
Write Data Setup Before $\overline{CS}$ Rising Edge	t_{39}	10			ns
Write Data Hold After $\overline{CS}$ Rising Edge	t_{40}	5			ns

NOTE
Guaranteed by design.

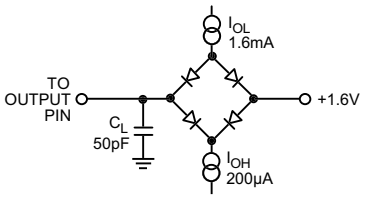


Figure 1. Load Circuit for Timing Specifications

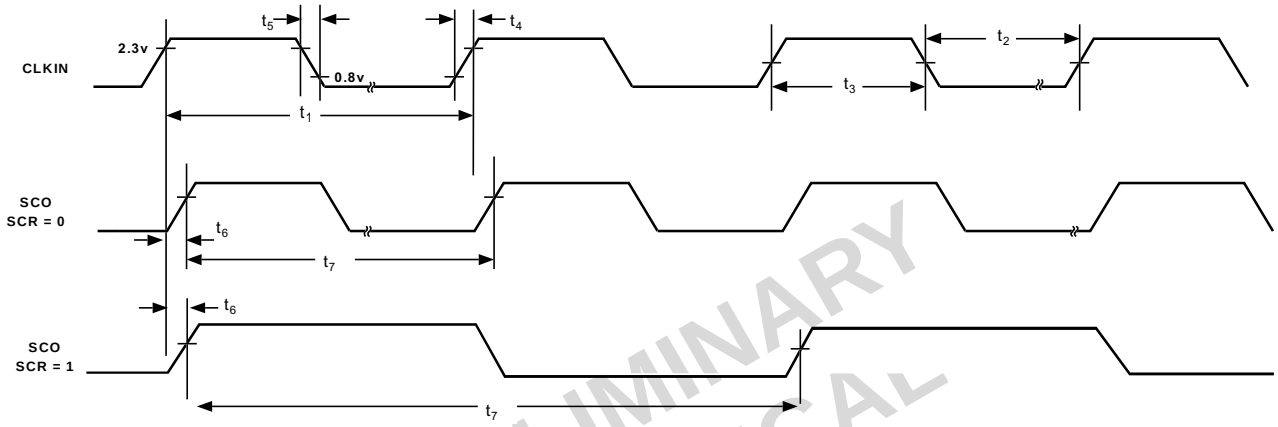


Figure 2. CLKIN to SCO Relationship

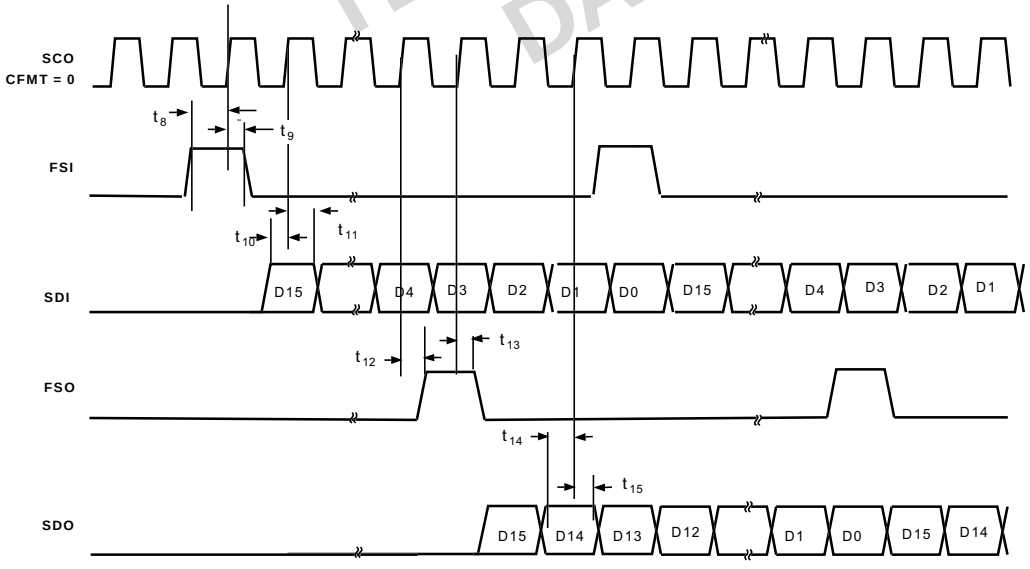
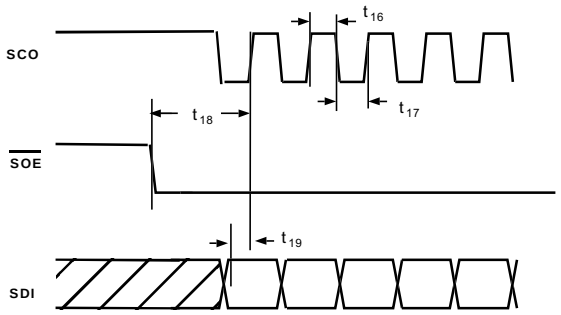


Figure 3. Serial Mode (DSP Mode and ROM Mode). In ROM Mode, Data is not written to the AD7725.



b)

Figure 4. Serial Mode (EPROM Mode)

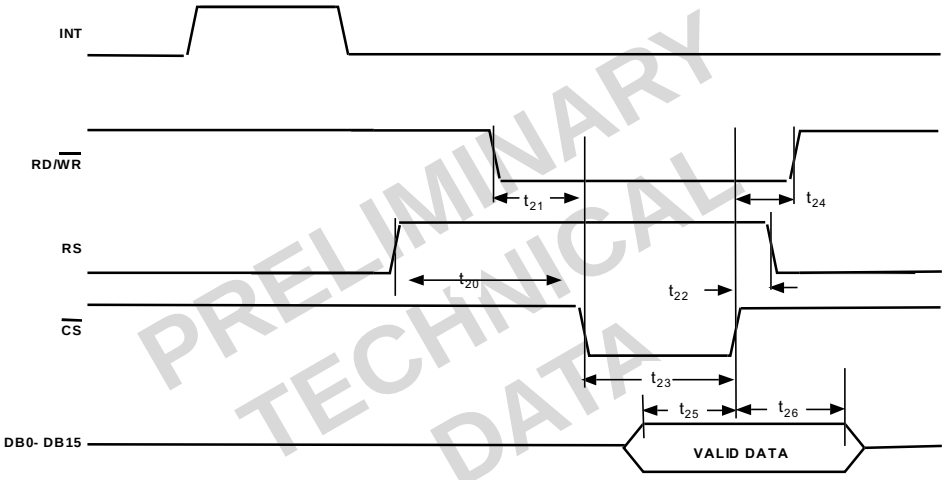


Figure 5. Parallel Mode (Writing Data to the AD7725).

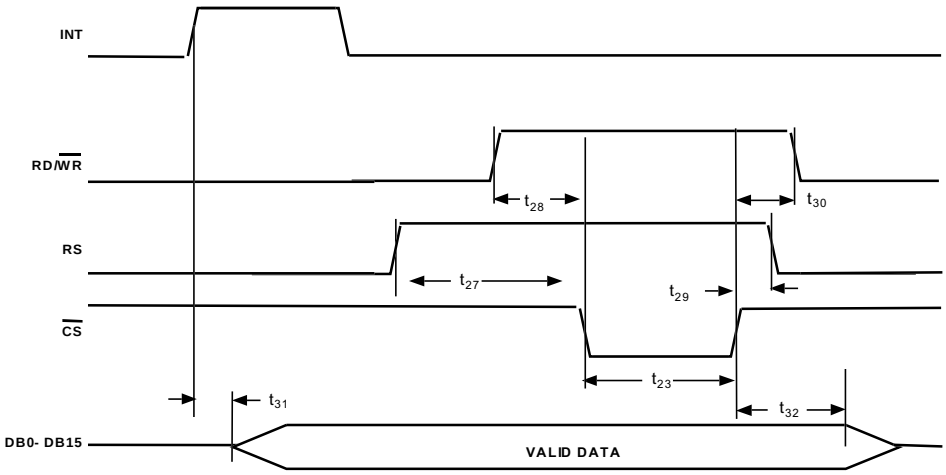


Figure 6. Parallel Mode (Reading Data from the Device).

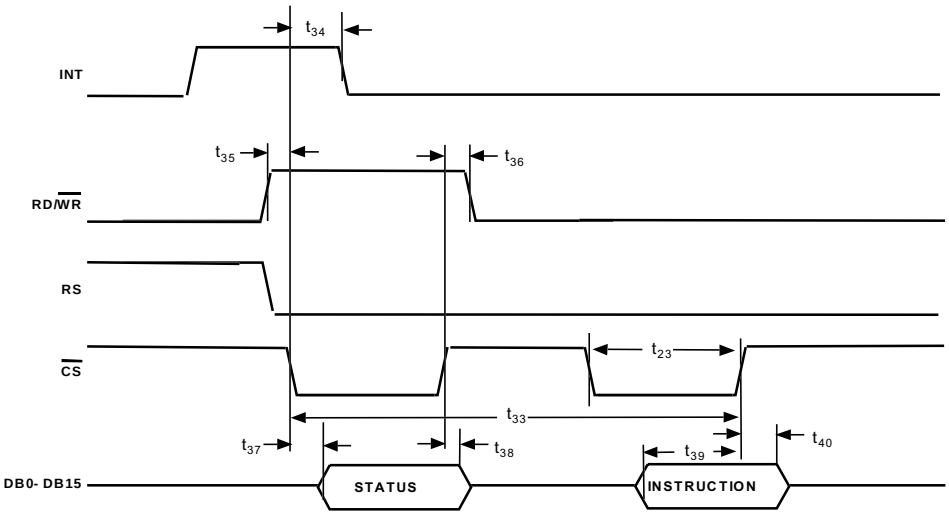


Figure 7. Parallel Mode (Reading the Status Register and Writing Instructions).

TABLE 1: PROGRAMMING MODES

S/$\overline{P}$	SMODE[1, 0]	Configuration Mode	Description
0	xx	MICRO	Parallel Interface. The 16-bit Bi-Directional Microprocessor Interface is used for Read/Write Operations.
1	01	DSP	Serial Interface. Bi-Directional Serial Synchronous Interface Suitable for Interfacing to a DSP.
1	00	ROM	Boot from internal ROM at power on reset (POR)
1	10	EEPROM	Boot from external serial EEPROM on POR
1	11	EEPROM-SLAVE	Boot multiple devices from one external EEPROM. Conversion data is multiplexed onto a common data bus

ABSOLUTE MAXIMUM RATINGS[1]
(T_A = +25°C Unless Otherwise Noted)

DVDD to DGND ..... -0.3 V to 7 V
AVDD to AGND ..... -0.3 V to 7 V
AVDD to DVDD.....-1 V to +1 V
AGND to DGND ..... -0.3 V to +0.3 V
Digital Inputs to DGND ..... -0.3 V to DV_{DD} + 0.3 V
Digital Outputs to DGND ..... -0.3 V to DV_{DD} + 0.3 V
VIN(+), VIN(-) toAGND ..... -0.3 V to AV_{DD} + 0.3V
REF1 to AGND ..... -0.3 V to AV_{DD} + 0.3V
REF2 to AGND ..... -0.3 V to AV_{DD} + 0.3V
REFIN to AGND ..... -0.3 V to AV_{DD} + 0.3V
DGND, AGND ..... ±0.3 V
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
q_{JA} Thermal Impedance ..... 75°C/W
Lead Temperature, Soldering
Vapor Phase(60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7725 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION
44-Pin PQFP Package

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7724BS	-40°C to +85°C	S-44

* S = Plastic Quad Flatpack (PQFP).

PIN FUNCTION DESCRIPTION

Mnemonic	Description
AVDD	Positive power supply voltage for the analog modulator.
AGND	Power supply ground for the analog modulator.
AVDD1	Digital logic power supply for the analog modulator.
AGND1	Digital logic power supply ground for the analog modulator.
AGND2	Power supply ground return to the reference circuitry, REF2, of the analog modulator.
DVDD	Digital power supply voltage.
DGND	Ground reference for digital circuitry.
REF1	Reference output. REF1 connects through 3kW to the output of the internal 2.5 V reference and to a buffer amplifier that drives the S-D modulator.
REF2	Reference Input. REF2 connects to the output of an external buffer amplifier used to drive the S-D modulator. When REF2 is used as an input, REF1 must be connected to AGND to disable the internal buffer amplifier.
VIN(+)	Positive terminal of the differential analog input.
VIN(-)	Negative terminal of the differential analog input.
UNI	Analog Input Range Select Input. The UNI pin selects the analog input range for either bipolar or unipolar operation. A logic high input selects unipolar operation and a logic low selects bipolar operation.
CLKIN	Clock Input. An external clock source can be applied directly to this pin with XTAL_OFF tied high. Alternatively, a parallel resonant fundamental frequency crystal, in parallel with a 1 MW resistor can be connected between the XTAL pin and the CLKIN pin with XTAL_OFF tied low. External capacitors are then required from the CLKIN and XTAL pins to ground. Consult the crystal manufacturer's recommendation for the load capacitors.
XTAL	Input to Crystal Oscillator Amplifier. If an external clock is used, XTAL should be tied to AGND.
XTAL_OFF	Oscillator Enable Input. A logic high disables the crystal oscillator amplifier to allow use of an external clock source. Set low when using an external crystal between the CLKIN and XTAL pins.
HALF_PWR	When set high, the power dissipation is reduced by approximately one half and a maximum CLKIN frequency of 10 MHz applies.
S/$\overline{P}$	Serial/Parallel Interface Select. When S/$\overline{P}$ is tied low, parallel mode is selected. Serial mode is selected when S/$\overline{P}$ is tied high.
SYNC	Synchronization Logic Input. When using more than one AD7725, operated from a common master clock, SYNC allows each ADC to simultaneously sample its analog input and update its output register. A rising edge resets the AD7725 digital filter sequencer counter to zero and resets the post processor core. When the rising edge of CLKIN senses a logic low on SYNC, the reset state is released. Because the digital filter and sequencer are completely reset during this action, SYNC pulses cannot be applied continuously.
STBY	Standby, Logic Input. When STBY is high, the device is placed in a low power mode. When During powerdown, the control logic is held in a reset state, therefore, the current status will be lost. The post processor will retain its configuration data but, signal data will be lost. When STBY is low, the AD7725 is powered up. The device will await its next instruction in DSP mode or, it will reboot from its ROM or EPROM in other serial modes.

SERIAL MODE PIN FUNCTION DESCRIPTION

Mnemonic	Description
$\overline{\text{ERR}}$/DB1	Configuration Error Flag. If an error occurs during programming, this open collector output goes low. This pin can be reset using the Clear Flag instruction (ClrFlags).
SDI/DB0	Serial Data Input. The serial data is shifted in MSB first, synchronous with SCO.
CFMT/RS	Serial Clock Format, Logic Input. The clock format pin selects whether the serial data, SDO, is valid on the rising or falling edge of the serial clock, SCO. When CFMT is logic low, serial data is valid on the rising edge of the serial clock, SCO. If CFMT is logic high, SDO is valid on the falling edge of SCO.
SMODE1/DB15	Serial Mode Select, Logic Input. This pin, in conjunction with SMODE0, selects the serial mode to be used.
SMODE0/DB14	Serial Mode Select, Logic Input. This pin, in conjunction with SMODE1, selects the serial mode to be used.
SCR/DB13	Serial Clock Rate Select Input. With SCR set to a logic low, the serial clock output frequency, SCO, is equal to the CLKIN frequency. A logic high sets the frequency of SCO to one half the CLKIN frequency.
END/DB12	Configuration End Logic Output. A logic high on END indicates that device programming is complete and no programming errors occured.
FSO/DB9	Frame Sync Output. FSO indicates the beginning of a word transmission on the SDO pin. Depending on the logic level of the SFMT pin, the FSO signal is either a positive pulse approximately one SCO period wide, or a frame pulse which is active low for the duration of the 16 bit transmission.
SDO/DB8	Serial Data Output. The serial data is shifted out MSB first, synchronous with SCO.
SCO/DB7	Serial Clock Output.
FSI/DB6	Frame Synchronization Logic Input. FSI indicates the beginning of a word on the SDI pin.
$\overline{\text{DVAL}}$/INT	Data Valid Logic Output. This open-collector output is low when there are no overflows or underflows in the post processor. $\overline{\text{DVAL}}$ goes high when an overflow/underflow occurs in the post processor.
$\overline{\text{SOE}}$/$\overline{\text{CS}}$	Serial Output Enable. $\overline{\text{SOE}}$ enables the external EEPROM and is used to reset the EEPROM's address counter.
CHI/DB2	Chain In Logic Input. A logic high on CHI initiates a configuration unless the $\overline{\text{END}}$ signal indicates that configuration is complete. If configuration is complete, CHI initiates a shift sequence, transferring the contents of the converter's result register to the serial interface. When the device has output its digital word, it awaits a pulse to its CHE pin before it outputs its next digital word.
CHE/DB11	Chain End Logic Input. Following a configuration, CHI is ignored unless CHE is pulsed high. By connecting CHO from the last device in the chain to all CHE inputs, the CHI signals are ignored until all chain events are complete.
CHO/DB3	Chain Out Logic Output. CHO is set high following a CHI triggered configuration or result register output sequence.
BFESTART	Boot from internal ROM/external EPROM Start, Logic Input. A logic high on BFESTART begins the configuration process - the configuration information is loaded into the device from ROM or external EPROM.
BFEDONE	Boot Complete Flag Input. When several devices are cascaded together, BFEDONE informs the AD7725 devices when all the devices have been configured. Conversion data can be output to the common serial bus when all the devices have been configured.
CHSYNC	Device Chain Synchronisation, Logic Input. CHSYNC is a positive edge triggered input which enables a conversion data sample to be read and the device's output register to be updated. It may be used to synchronise conversion data from multiple AD7725 devices.

MODE 2 PARALLEL MODE PIN FUNCTION DESCRIPTION

Mnemonic	Description
$\overline{SOE}/\overline{CS}$	Chip Select Logic Input.
RD/$\overline{WR}$	Read/Write Logic Input. Read cycles are initiated when RD/$\overline{WR}$ is high and the internal clock detects that $\overline{CS}$ has gone low and remains low for one cycle. A write cycle is initiated by taking RD/$\overline{WR}$ low and taking $\overline{CS}$ low for one clock cycle.
CFMT/RS	Register Select. RS selects between the data register, used to read conversion data or write configuration data, and the instruction register. A logic high on RS selects the data register while a logic low selects the instruction register.
$\overline{DVAL}$/INT	Interrupt Logic Output. INT is a programmable output pin which can be programmed to go high when a conversion result is ready to be read from the device, to operate as a busy pin when the part is being configured or while the part is performing instructions or as an error pin to indicate when there are ID, CRC or data errors. INT is normally low.
SMODE1/DB15	Data Output Bit (MSB).
SMODE0/DB14	Data Output Bit.
SCR/DB13	Data Output Bit.
$\overline{END}$/DB12	Data Output Bit.
CHE/DB11	Data Output Bit.
TSI/DB10	Data Output Bit.
FSO/DB9	Data Output Bit.
SDO/DB8	Data Output Bit.
SCO/DB7	Data Output Bit.
FSI/DB6	Data Output Bit.
SFMT/DB5	Data Output Bit.
DOE/DB4	Data Output Bit.
CHO/DB3	Data Output Bit.
CHI/DB2	Data Output Bit.
ERR/DB1	Data Output Bit.
SDI/DB0	Data Output Bit (LSB).

CIRCUIT DESCRIPTION

The AD7725 employs a sigma-delta conversion technique to convert the analog input into an equivalent digital word. The modulator samples the input waveform and outputs an equivalent digital word at the input clock frequency, f_{CLKIN}.

Due to the high oversampling rate, which spreads the quantization noise from 0 to $f_{CLKIN}/2$, the noise energy contained in the band of interest is reduced (Figure 8a). To further reduce the quantization noise, a high order modulator is employed to shape the noise spectrum, so that most of the noise energy is shifted out of the band of interest (Figure 8b).

The digital filter which follows the modulator removes the large out-of-band quantization noise (Figure 8c) while also reducing the data rate from f_{CLKIN} at the input of the filter to $f_{CLKIN}/16$ or less at the output of the filter, depending on the filter type used.

Digital filtering has certain advantages over analog filtering. Since digital filtering occurs after the A/D conversion, it can remove noise injected during the conversion process. Analog filtering cannot do this. The digital filter also has a linear phase response.

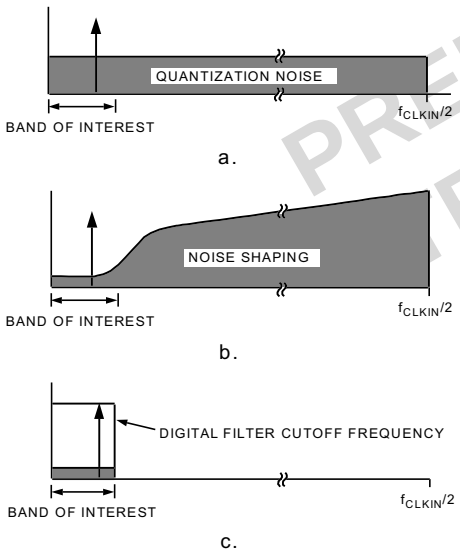


Figure 8. Sigma-Delta ADC

The AD7725 employs three fixed Finite Impulse Response (FIR) filters in series. Each individual filter's output data rate is half that of the filter's input data rate. The fourth stage is programmable, the user being able to select a lowpass, bandpass, stopband or highpass filter response. Both the filter response and the decimation are user programmable. Alternatively, the user can use the default fourth stage which is contained in ROM on the AD7725. This fourth stage decimates by four which leads to an output word rate of $f_{CLKIN}/32$.

APPLYING THE AD7725

Analog Input Range

The AD7725 has differential inputs to provide common-mode noise rejection. In unipolar mode, the analog input range is 0 to 8/5 x VREF2, while in bipolar mode, the analog input range is +4/5 x VREF2. The output code is twos complement binary in both modes with 1 LSB = 61 mV. The ideal input/output transfer characteristics for the two modes are shown in Figure 9 below. In both modes, the absolute voltage on each input must remain within the supply range AGND to AVDD. The bipolar mode allows either single-ended or complementary input signals.

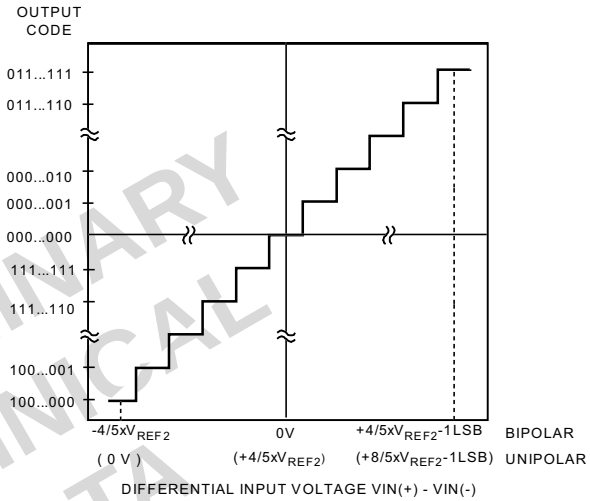


Figure 9. Bipolar (Unipolar) Mode Transfer Function

The AD7725 will accept fullscale inband signals. However, large scale out-of-band signals can overload the modulator inputs. A minimal single-pole RC antialias filter set to $f_{CLKIN}/24$ will allow fullscale input signals over the entire frequency spectrum.

Analog Input

The analog input of the AD7725 uses a switched capacitor technique to sample the input signal. For the purpose of driving the AD7725, an equivalent circuit of the analog inputs is shown in Figure 10. For each half clock cycle, two highly linear sampling capacitors are switched to both inputs, converting the input signal into an equivalent sampled charge. A signal source driving the analog inputs must be able to source this charge, while also settling to the required accuracy by the end of each half-clock phase.

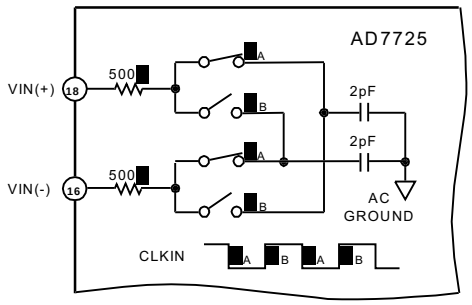


Figure 10. Analog Input Equivalent Circuit

Driving the Analog Inputs

To interface the signal source to the AD7725, at least one op amp will generally be required. The choice of op amp will be critical to achieving the full performance of the AD7725. The op amp not only has to recover from the transient loads that the ADC imposes on it but, must also have good distortion characteristics and very low input noise. Resistors in the signal path will also add to the overall thermal noise floor, necessitating the choice of low value resistors.

Placing an RC filter between the drive source and the ADC inputs, as shown in Figure 11, has a number of beneficial affects: transients on the op amp outputs are significantly reduced since the external capacitor now supplies the instantaneous charge required when the sampling capacitors are switched to the ADC input pins and, input circuit noise at the sample images is now significantly attenuated resulting in improved overall SNR. The external resistor serves to isolate the external capacitor from the ADC output, thus improving op amp stability while also isolating the op amp output from any remaining transients on the capacitor. By experimenting with different filter values, the optimum performance can be achieved for each application. As a guideline, the RC time constant (R x C) should be less than a quarter of the clock period to avoid nonlinear currents from the ADC inputs being stored on the external capacitor and degrading distortion. This restriction means that this filter cannot form the main antialias filter for the ADC.

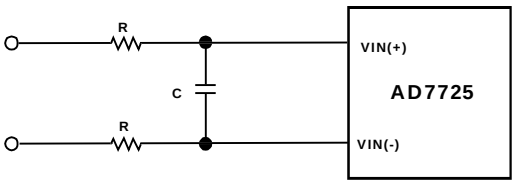


Figure 11. Input RC Network

With the unipolar input mode selected, just one op amp is required to buffer single-ended input signals. However, driving the AD7725 with complementary signals and with the bipolar input range selected has some distinct advantages: even order harmonics in both the drive circuits and the AD7725 front end are attenuated; and the peak to peak input signal range on both inputs is halved. Halving the input signal range allows some op amps to be powered from the same supplies as the AD7725. Although a complementary driver will require the use of two op amps per ADC, it may avoid the need to generate additional supplies just for these op amps.

Figure 12 and 13 show two such circuits for driving the AD7725. Figure 12 is intended for use when the input signal is biased about 2.5 V while Figure 13 is used when the input signal is biased about ground. While both circuits convert the input signal into a complementary signal, the circuit in Figure 13 also level shifts the signal so that both outputs are biased about 2.5 V.

Suitable op amps include the AD8047, AD8044, AD8041 and its dual equivalent the AD8042. The AD8047 has lower input noise than the AD8041/42 but has to be supplied from a +7.5 V/-2.5 V supply. The AD8041/ AD8042 will typically degrade the SNR from 90 dB to 80 dB but can be powered from the same single +5 V supply as the AD7725.

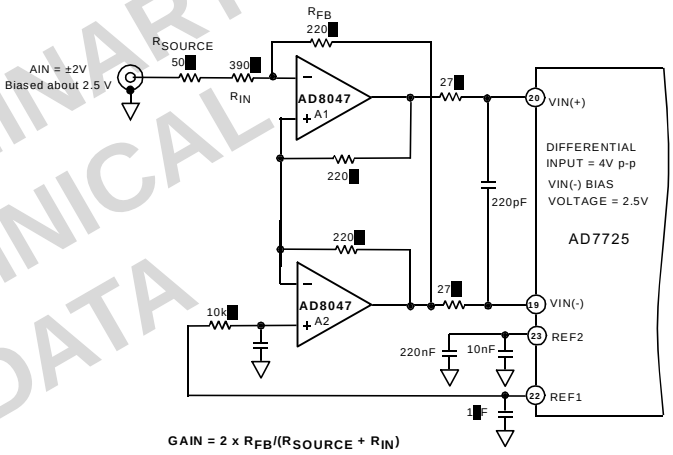


Figure 12. Single-Ended to Differential Input Circuit for Bipolar Mode Operation (Analog Input Biased About +2.5V)

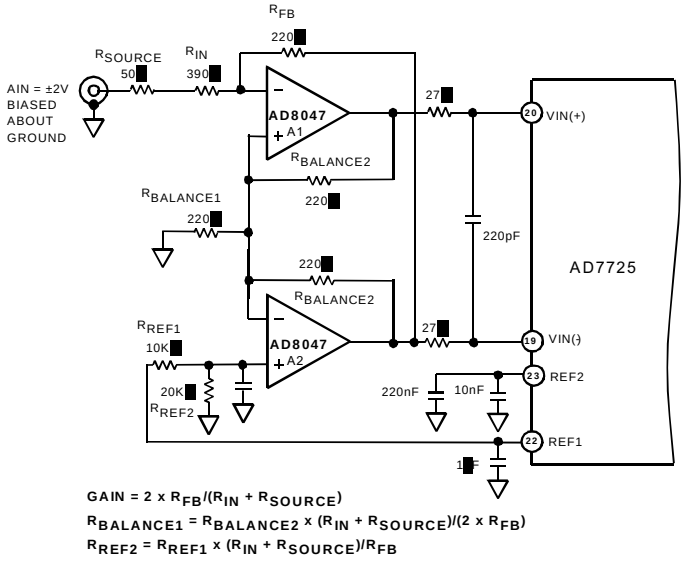


Figure 13. Single-Ended to Differential Input Circuit for Bipolar Mode Operation (Analog Input Biased About Ground)

Applying the Reference

The reference circuitry used in the AD7725 includes an on chip 2.5 V bandgap reference and a reference buffer circuit. The block diagram of the reference circuit is shown in Figure 14. The internal reference voltage is connected to REF1 through a 3 kW resistor and is internally buffered to drive the analog modulator's switched cap DAC (REF2). When using the internal reference, a 1 mF capacitor is required between REF1 and AGND to decouple the bandgap noise. If the internal reference is required to bias external circuits, use an external precision op amp to buffer REF1.

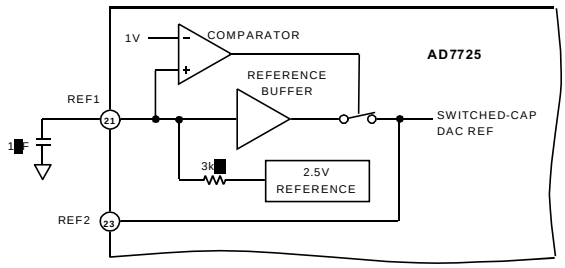


Figure 14. Reference Circuit Block Diagram

Where gain error or gain drift requires the use of an external reference, the reference buffer in Figure 14 can be turned off by grounding the REF1 pin and the external reference can be applied directly to pin REF2. The AD7725 will accept an external reference voltage between 1.2 V and 3.15 V. By applying a 3 V rather than a 2.5 V reference, SNR is typically improved by about 1 dB. Where the output common-mode range of the amplifier driving the inputs is restricted, the fullscale input signal span can be reduced by applying a lower than 2.5 V reference. For example, a 1.25 V reference would make the bipolar input range ±1 V but would degrade SNR.

In all cases, since the REF2 voltage connects to the analog modulator, a 220 nF and 10 nF capacitor must connect directly from REF2 to AGND. The external capacitor provides the charge required for the dynamic load presented at the REF2 pin (see Figure 15).

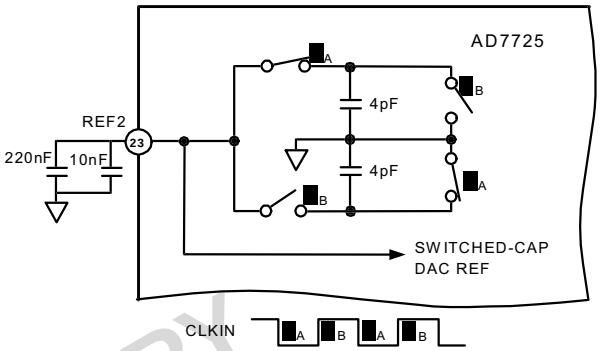


Figure 15. REF2 Equivalent Input Circuit

The AD780 is ideal to use as an external reference with the AD7725. Figure 16 shows a suggested connection diagram. Grounding pin 8 on the AD780 selects the 3 V output mode.

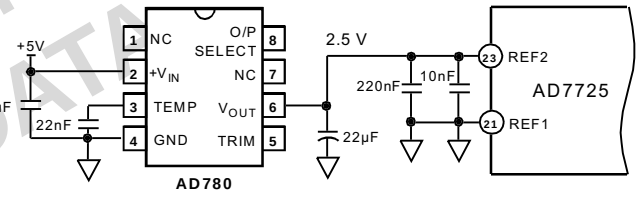


Figure 16. External Reference Circuit Connection

Clock Generation

The AD7725 contains an oscillator circuit to allow a crystal or an external clock signal to generate the master clock for the ADC. The connection diagram for use with a crystal is shown in Figure 17. Consult the manufacturer's recommendation for the load capacitors. To enable the oscillator circuit on board the AD7725, XTAL_OFF should be tied low.

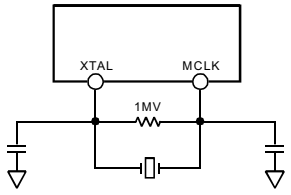


Figure 17. Crystal Oscillator Connection

When an external clock source is being used, the internal oscillator circuit can be disabled by tying XTAL_OFF high. A low phase noise clock should be used to generate

the ADC sampling clock because sampling clock jitter effectively modulates the input signal and raises the noise floor. The sampling clock generator should be isolated from noisy digital circuits, grounded and heavily decoupled to the analog ground plane.

The sampling clock generator should be referenced to the analog ground in a split ground system. However, this is not always possible because of system constraints. In many applications, the sampling clock must be derived from a higher frequency multipurpose system clock that is generated on the digital ground plane. If the clock signal is passed between its origin on a digital ground plane to the AD7725 on the analog ground plane, the ground noise between the two planes adds directly to the clock and will produce excess jitter. The jitter can cause degradation in the signal-to-noise ratio and also produce unwanted harmonics. This can be remedied somewhat by transmitting the sampling signal as a differential one, using either a small RF transformer or a high speed differential driver and a receiver such as PECL. In either case, the original master system clock should be generated from a low phase noise crystal oscillator.

SYSTEM SYNCHRONIZATION

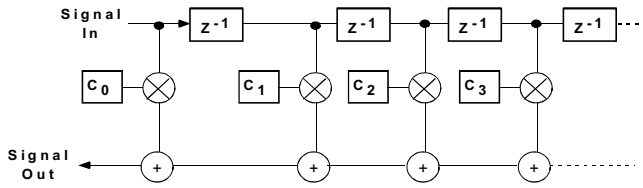
The $\overline{\text{SYNC}}$ input provides a synchronization function for use in parallel or serial mode. SYNC allows the user to begin gathering samples of the analog input from a known point in time. This allows a system using multiple AD7725s, operated from a common master clock, to be synchronized so that each ADC simultaneously updates its output register.

In a system using multiple AD7725s, a common signal to their SYNC inputs will synchronize their operation. On the rising edge of SYNC, the digital filter sequencer is reset to zero. A SYNC pulse, one CLKIN cycle long, can be applied. This way, SYNC is sensed low on the next rising edge of CLKIN.

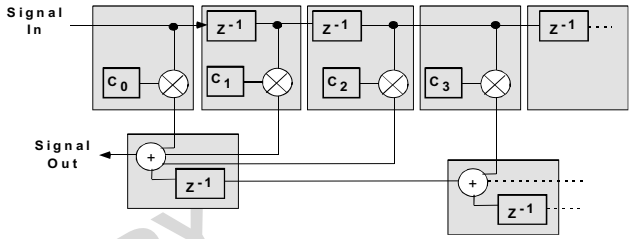
Following a SYNC, the modulator and filter need time to settle before data can be read from the AD7725. In serial mode, $\overline{\text{DVAL}}$/INT goes high following a synchronization and it remains high until valid data is available at the interface. In parallel mode, $\overline{\text{DVAL}}$/INT will stay low during the synchronizaion procedure and will go high when vald data is available at the interface.

POST PROCESSOR

The AD7725's post processor core is a systolic array of simple high performance processors. There are 108 of these in the AD7725. In a systolic array, data is pumped between processors. Each of these processors is allocated to a dedicated function and will only perform that single function. The data is passed between processors and, in this manner, complex operations are performed on the signal. Figure 18 shows an example of a filtering function implemented on the post processor. Figure 18a shows the data path representation of an FIR filter while Figure 18b shows how this algorithm would be implemented on the AD7725. It can be seen from this example that a single FIR tap requires 1.3 processors for implementation. This is a useful guideline when calculating the design requirements for a new application. In the AD7725, data transfers between processors are fully synchronous. As a result, the user does not have to consider timing issues.



a) FIR Data Path Representation



b) FIR Post Processor Implementation

Figure 18. AD7725 Processor Mapping

The processor core is optimised for signal conditioning applications. In this type of application, the most common function is generally filtering. The core can support any filter structure, whether FIR, IIR, recursive or non-recursive. As can be seen from the previous example, this type of algorithm maps very efficiently to the post processor.

Data can be transparently decimated or interpolated when passed between processors. This simplifies the design of multi-rate filtering and gives great flexibility when specifying the final output word rate. The AD7725 post processor supports decimation/interpolation by factors up to 255.

To program the AD7725, the user must produce a configuration file which contains the programming data for the intended function. The AD7725 compiler generates this file. The compiler accepts filter coefficient data as an input and automatically generates the required device programming data. The user must enter the filter parameters and coefficient data as shown in Figure 19.

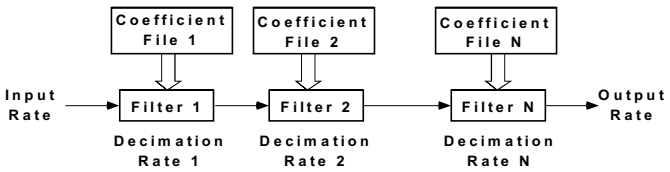


Figure 19. Filter Parameter Specification

When powered on in Boot-from-ROM mode, the AD7725 will automatically load a default filter characteristic which is stored on chip. This characteristic is shown in Figure 20. In all other modes, the device must be configured using external data.

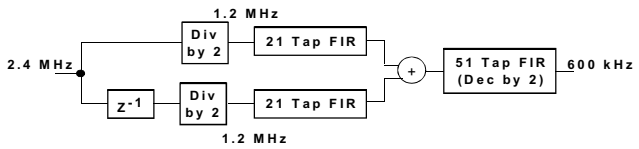


Figure 20a) Default Post Processor Programming

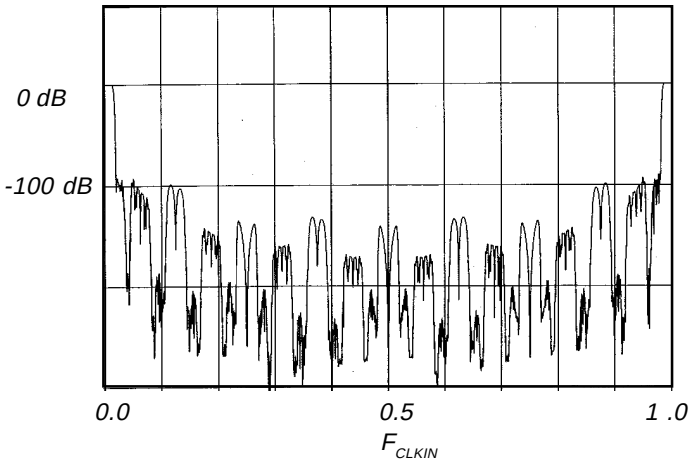


Figure 20b) Filter Response of Default Filter

PROGRAMMING THE POST PROCESSOR

The coefficients file for the FIR filter response can be generated using a digital filter design package such as QEDesign. This package allows the user to design different filter types (FIR, IIR, etc). The response of the filter can be plotted so that the user knows the response (cutoff frequency, rolloff, attenuation) before generating the coefficients. When using the post processor, the data is available to the processor at 2.4 MHz. When decimation is employed, in a multi stage filter, the first filter will be operated at 2.4 MHz and the user can then decimate between stages. The number of taps which can be contained in the post processor is 108. Therefore, a single filter with 108 taps can be generated or, a multi stage filter can be designed whereby the total number of taps adds up to 108.

At a given filter frequency, any bandwidth requires the same number of taps. However, the number of taps increases as the filter rolloff is increased. Therefore, a filter with a bandwidth of 300 kHz awhich rolloffs between 300 kHz and 600 kHz uses less taps than a filter with a cutoff frequency of 300 kHz which rolloffs between 300 kHz and 450 kHz.

To reduce the number of taps needed, a multi stage filter can be designed with decimation performed between stages. When decimation is performed, the noise is wrapped around the filter frequency divided by 2 each time the output is decimated by 2 so, the user needs to ensure that the quantisation noise is reduced sufficiently i.e. the quantisation noise should be filtered in a given area if this region will map into the bandwidth of interest during decimation. With appropriate filtering, the noise floor will increase by 3 dB each time that the data stream is decimated by 2. However, the noise floor is down at 120 dB prior to decimation. Therefore, with suitable decimation, the SNR will be 90 dB typically at the AD7725 output.

Although decimation causes the noise floor to increase by 3 dB each time that the data stream is decimated by 2, decimation causes a reduction in the number of filter taps needed for a given response. For example, the number of taps needed to generate a cutoff frequency of 300 kHz and a stopband frequency of 600 kHz will equal the number of taps needed to generate a filter with a cutoff frequency of 300 kHz and a stopband frequency of 450 kHz if the data stream is decimated by 2 prior to the filtering stage. However, the user must ensure that the quantisation noise has been filtered prior to this filtering stage. Otherwise, the noise floor will be increased in the bandwidth of interest and the SNR will degrade.

To generate an FIR filter with a cutoff frequency of 300 kHz, a stopband frequency of 600 kHz, a passband ripple of 0.01 dB and a stopband attenuation of 90 dB requires 47 taps when the Kaiser window is used. To generate a similar filter with a stopband frequency of 450 kHz requires 93 taps. By decimating the data stream prior to filtering, the filter frequency will equal 1.2 MHz rather than 2.4 MHz and the number of taps needed to generate this response is 47.

When the user has generated the coefficients, these can be loaded into the AD7725 compiler. To generate a multi stage filter, each stage can be generated separately and the compiler will amalgamate the separate files to generate the overall response.

MODES OF OPERATION

SERIAL MODE

The serial mode is selected by tying S/P to VDD. In serial mode, the default filter type can be used (ROM mode). Alternatively, the filter can be user-defined and, the user can then load the configuration file from a DSP or from external EPROM. Devices can also be daisy-chained in serial mode, allowing several devices to share a common serial interface.

In all serial modes, except the ROM mode, a status register can be read to ensure that the user-defined filter information is correctly loaded. The status register is shown in Table 2.

TABLE 2. STATUS REGISTER BITS

Bits	Function	Description
D15 - D6	Reserved	
D5	Configured	Set to 1 at the end of loading the configuration file if the data is correctly loaded. Set to 0 if an error occurs during loading the configuration data. This bit is reset to 0 at the start of loading the configuration data.
D4	Ready	This bit indicated when the Power on Reset (POR) is complete. When the bit is set to 1, the device is ready to receive an instruction.
D3	Reserved	
D2	ID Error	If configuration data has an incorrect ID, this bit is set to 1. If the ID is correct, this bit is set to 0.
D1	CRC Error	If the configuration data is corrupt, this bit is set to 1. If the data is correct, this bit is set to 0.
D0	Data Error	During each conversion cycle, the data is checked for overflow/ underflow. If an overflow/underflow occurs, this bit is set to 1. If the data is within specification, the bit is set to 0. This bit is reset at the beginning of each conversion cycle.

Using the Default Filter

When the AD7725 is used with the default filter, the information contained in the on-board ROM is loaded into the postprocessor on power up. This mode of operation is selected by tying both SMODE0 and SMODE1 to ground. A signal is not available on SCO until the power up sequence is complete. When the filter information has been loaded, SCO becomes active and the AD7725 will begin converting. FSI and SDI are not used in this mode so, they should be hardwired to ground. SCO will have a frequency of CLKIN or CLKIN/2, the frequency being selected by SCR. Addtionally, the SCO edge on which the data is output from the device can be selected using CFMT. With SCR = 0, SCO equals CLKIN. With SCR = 1, SCO equals half the CLKIN frequency. With CFMT = 0, data is output on the SCO rising edge while data is output on the falling edge when CFMT = 1.

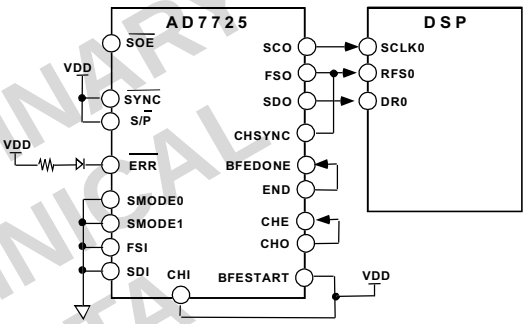


Figure 21. AD7725 uses its Default Filter.

The default filter has a cutoff frequency of 100 kHz and a stopband frequency of 200 kHz. The filter response is shown in Figure 22. The digital words are available at the serial interface at CLKIN/32.

Figure 22. Filter Response of Default Filter.

Loading Configuration Data from a DSP

The DSP mode is selected by tying SMODE1 to ground and SMODE0 to VDD. In DSP mode, the AD7725 can be operated with the default filter or, a filter can be developed off chip and the resulting configuration filter can be loaded into the AD7725 from the DSP.

When the AD7725 powers up and settles, SCO becomes active and the device awaits the first instruction. The user can then inform the AD7725 whether to accept an external configuration file or whether to load the default filter data from the on-board ROM. After loading the configuration information, the status register can be read and the user can instruct the AD7725 to begin conversions.

The AD7725 has a synchronous serial interface. The AD7725 generates the serial clock SCO whose frequency can be CLKIN (SCR = 0) or CLKIN/2 (SCR = 1).

SCO must have a frequency equal to CLKIN if the AD7725 outputs data at CLKIN/16. For lower output word rates, either clock frequency can be used. To load configuration data or instructions into the AD7725, an FSI pulse of one CLKIN cycle wide informs the AD7725 that data is being transferred into the device. The data is loaded using the next 16 SCLK cycles following the detection of the FSI pulse. If a read instruction is loaded into the AD7725 (read the status register), the user must wait until this instruction is completed before issuing the next instruction.

When the AD7725 is instructed to output an Analog to Digital conversion result, the AD7725 will continuously output conversion data until it receives another instruction to perform another function.

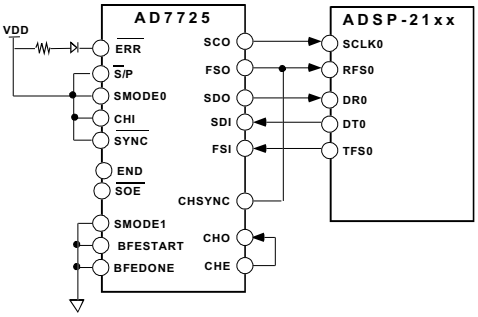


Figure 23. Loading the Configuration Data from a DSP.

Configuring the AD7725 using External EPROM

The AD7725 provides an interface which can be used to load the configuration data from an external EPROM on power up. Again, on power up, the EPROM is activated and the configuration information is transferred to the AD7725. When the information has been transferred, SCO is enabled and the AD7725 is ready to begin conversions.

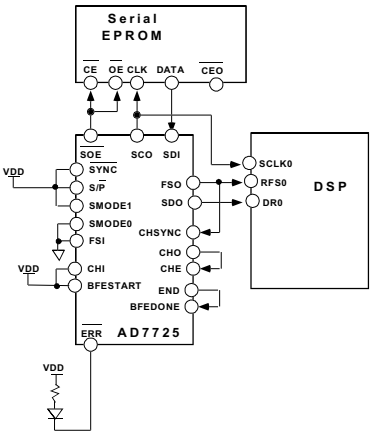


Figure 24. Loading the Configuration Data from an External EPROM.

To select this mode, SMODE1 is tied to VDD and SMODE0 is tied to ground. When the AD7725 powers up and settles, SOE goes low. SOE enables the output pin of the EPROM and resets its pointer. SCO becomes active and the configuration data is latched into the AD7725 on the SCO rising edge. SCO has a frequency of CLKIN/16 during this loading procedure. When the configuration file has been loaded into the AD7725, SOE goes high and SCO will have a frequency of CLKIN or CLKIN/2 depending on the polarity of SCR. The status register can be read to confirm that the configuration was loading successfully and the AD7725 can be instructed to begin conversions.

Daisy-Chaining Mode

Several AD7725s can be daisy-chained so that they are configured from a common EPROM and share a serial interface onto which their conversion data is transferred. Figure 25 shows the circuit diagram for connecting two AD7725s in daisy-chain mode. With the master device, SMODE1 is tied to VDD while SMODE0 is tied to ground. The mode pins have the same polarity as when a single device is being loaded from an EPROM. The slave device has both SMODE0 and SMODE1 tied to VDD.

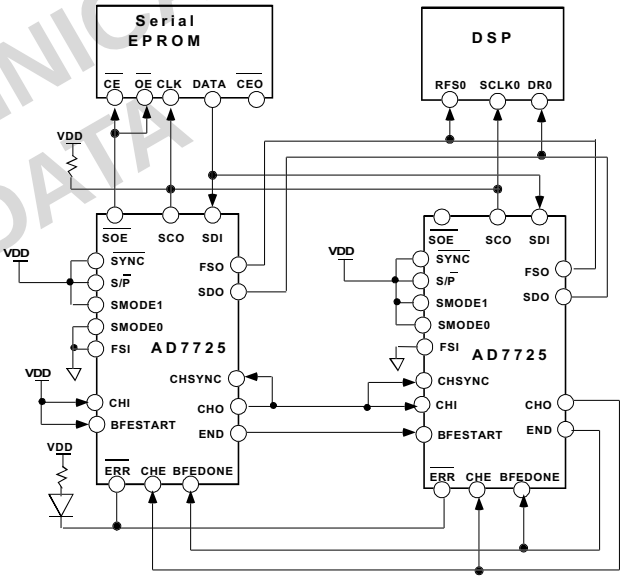


Figure 25. Daisy-Chaining Devices whch are Configured from an EPROM

When BFESTART is high, the associated device is loaded with configuration data. When the loading of the configuration data is complete, END goes high. In daisy-chaining mode, END of the first device can be applied to BFESTART of the next device so, the slave will be loaded with configuration data. When the last device in the chain is loaded with configuration data, its END

signal goes high. This signal is applied to the BFEDONE input of all the devices so that all devices will know when the configuration procedure is complete.

CHI, CHO and CHE are used when the devices are performing conversions. When CHI is taken high, the associated device outputs its digital conversion word onto the serial interface. When it has output its 16-bit word, CHO goes high. By tying CHO of the first device to CHI of the next device, the second device is informed to output its digital conversion word. This procedure continues through the devices until the last device in the chain outputs its digital word. CHO of the last device is connected to CHE of each device. Once a device has output a digital word, CHI of the device is not monitored until the device reveices a pulse on CHE. This indicates that all devices have output their digital conversion data.

The user needs to ensure that there is sufficient time between conversions so that all devices in the chain can output their 16-bit digital word before the next conversion is complete. If there is insufficient time, some conversion information will be lost.

SERIAL MODE INSTRUCTION SET AND STATUS REGISTER

TABLE 3. INSTRUCTION SET FOR SERIAL MODE

Instruction	Hex Code	Description
BFR	7004	Boot from Internal ROM
RdID	A700	Read Device ID
RdCONV	B600	Read Converter Data. When this instruction is written to the AD7725, the device will continue to output conversion data until another instruction is issued.
RdStatus	A800	Read Status Register
WrConfig	7000	Write Configuration Data
ClrFlags	1000	Clear Status Register Flags (CRC Error and ID Error)

In DSP mode, the READY bit in the status register will be set to 1 when the AD7725 has powered up completely. An instruction then needs to be issued to inform the AD7725 whether the filter response in ROM is being used or a user-defined filter response is being used. For example, if a user-defined response is being used, code 7000h to the AD7725. The device then knows that data is being loaded from an external source. The configuration data is loaded into the device using FSI, SDI and SCO. When the configuration file has been loaded (END will go high), the status register should be read to ensure that the device ID was correct and to determine if the loaded data was corrupt. If the configuration data is loaded successfully, conversions can begin by writing B600h to the AD7725.

If an error occurs while loading the configuration data, the CRC and/or Device ID flag bits will be set in the status register. The user should reset these flags to zero and load the configuration data again (instruction 7000h followed by the configuration data).

In EPROM mode, the configuration data is loaded automatically on power up from the EPROM. However, the status register should be checked to ensure that the configuration data was correctly loaded.

In ROM mode, the status register/instruction set is not available to the user.

PARALLEL MODE

The parallel mode is selected by tying S/$\overline{P}$ to ground. The SMODE0 and SMODE1 pins are not used in this mode so, they should be hardwired low. The parallel interface is a standard interface which interfaces to Digital Signal Processors and Microcontrollers. Figure 26 shows the interface between the AD7725 and a microprocessor. Pins RD/$\overline{WR}$, $\overline{CS}$ and RS are used along with the data pins D0 to D15 to write instructions/data and read the status register/data.

During a read cycle, the RS pin informs the AD7725 whether the status register or a conversion result is being read. When RS is low, the status register is being read while the data register is read when RS is high. Similarly, during a WR cycle, an instruction is written when RS is low and data (such as configuration data) is written when RS is high.

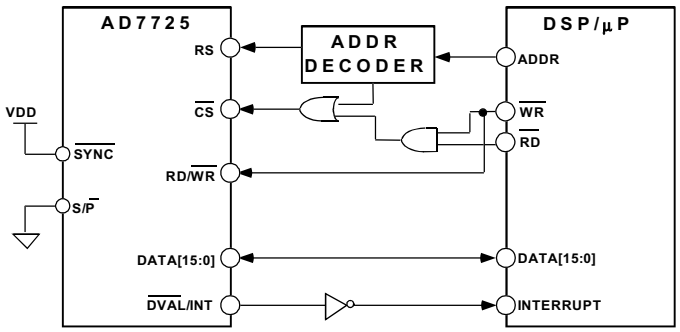


Figure 26. AD7725 Parallel Interface to Microprocessor.

When the AD7725 is powered up, INT goes high when the AD7725 has powered up and settled and is ready for programming. The device can then be loaded with a filter response from the microprocessor or the filter response contained in ROM can be used. An instruction is written to the AD7725 to inform the device of the filter response being used (ROM or an external filter response). If an external filter response is being used, it is loaded from the microprocessor. INT goes high when the AD7725 is ready to accept the configuration data. RS is taken high

to load the data. Each time the AD7725 reads in 16 bits, it generates an INT when the next 16 bits of data can be loaded. The status register can be read while loading the configuration data to check for corrupt data.

Loading the Configuration Data in Parallel Mode

The configuration file can hold up to 8272 bits of information. After power up, the user first needs to send an instruction to the AD7725 to inform the device that configuration data is being loaded via the interface. The complete configuration data can then be loaded into the device. The configuration file contains the device ID which is loaded into the AD7725. The AD7725 checks the ID to ensure that the following configuration is to be loaded into the device. If the ID is incorrect, a bit is set in the status register to inform the user that the device ID is incorrect.

The postprocessor can hold up to 8064 bits of data. The data is split into blocks of 672 bits in the configuration file. This consists of 42 words of configuration data along with a CRC instruction i.e. the data is checked for corruption. The AD7725 accepts the first 672 bits of information and checks the data for errors before loading the information into the postprocessor. If there are no errors, the data is loaded into the postprocessor and the AD7725 awaits the next 672 bits of data. If the data is corrupt, the AD7725 abandons loading the data into the postprocessor. The CRC bit in the status register is set to 1, indicating that the configuration data is corrupt. In parallel mode, the status register can be read while loading the configuration data. RS is taken low and RD/$\overline{WR}$ is taken high to read the status register. When CS is taken low, the contents of the status register will be output i.e. a 'Read the Status Register' instruction does not have to be issued first.

The status register is shown in Table 4. The status register gives further information in parallel mode compared to serial mode. See Table 5 for details.

TABLE 4: STATUS REGISTER (PARALLEL MODE)

Bit	Name	Function
15	InstrBUSY	This bit is set to 1 when an instruction is being performed
14	Data Ready	This bit is set to 1 when a data conversion is complete to indicate that the data register has been updated with a new digital word
13	Data Request	This bit is set to 1 when the AD7725 is converting to indicate that the digital words being output from the device are data words rather than control words
12	ID Error	This bit is set to 1 if the programming data has an incorrect ID Value
11	CRC Error	This bit is set to 1 if Corrupt Data is loaded into the Device
10	Data Error	This bit is set to 1 if an underflow/ overflow occurs to indicate that the conversion result is invalid
9	InstrReg[15]	Instruction Register Bit 15
8	InstrReg[14]	Instruction Register Bit 14
7	InstrReg[13]	Instruction Register Bit 13
6	InstrReg[12]	Instruction Register Bit 12
5	InstrReg[11]	Instruction Register Bit 11
4	InstrReg[10]	Instruction Register Bit 10
3	InstrReg[9]	Instruction Register Bit 9
2	InstrReg[8]	Instruction Register Bit 8
1	ROM Used	This bit is set to 1 when the Filter Response is provided by the ROM and it is set to 0 when the filter is user-defined
0	Reserved	

TABLE 5. INSTRUCTION SET FOR PARALLEL MODE

Instruction	Hex Code	Description
BFR	7004	Boot from Internal ROM
RdID	A700	Read Device ID
RdCONV	B600	Read Converter Data. When this instruction is written to the AD7725, the device will continue to output conversion data until another instruction is issued.
RdStatus	A800	Read Status Register
WrConfig	7000	Write Configuration Data
WrConfigEM	7008	Write Configuration Data, Mask Errors
ClrFlags	1000	Clear Status Register Flags (CRC Error and ID Error)