1MSPS, 12-Bit ADCs in µSO-8

Preliminary Technical Data — AD7475/95

FEATURES

Fast Throughput Rate: 1MSPS
Specified for V_{DD} of 2.7 V to 5.25 V
Low Power:
3mW typ at 1MSPS with 3V Supplies
9mW typ at 1MSPS with 5V Supplies
Wide Input Bandwidth:
70dB SNR at 500kHz Input Frequency
Flexible Power/Serial Clock Speed Management
No Pipeline Delays
High Speed Serial Interface SPI/QSPI/µWire/DSP Compatible
Onboard Reference 2.5V (AD7495 only)
Standby Mode: 1µA max
8-Pin µSOIC and SOIC Packages

GENERAL DESCRIPTION

The AD7475 /AD7495 are 12-bit high speed, low power, successive-approximation ADCs. The parts operate from a single 2.7 V to 5.25 V power supply and feature throughput rates up to 1MSPS. The parts contain a low-noise, wide bandwidth track/hold amplifier which can handle input frequencies in excess of 1MHz.

The conversion process and data acquisition are controlled using CS and the serial clock allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of CS and conversion is also initiated at this point. There are no pipelined delays associated with the part.

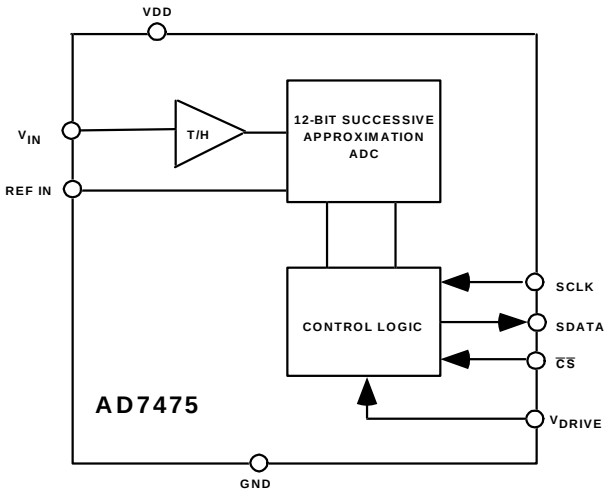
The AD7475/AD7495 use advanced design techniques to achieve very low power dissipation at high throughput rates. With 3V supplies and 1MSPS throughput rate, the AD7475 consumes just 1mA, while the AD7495 consumes 1.2mA. With 5V supplies and 1MSPS, the current consumption is 1.8mA for the AD7475 and 2mA for the AD7495.

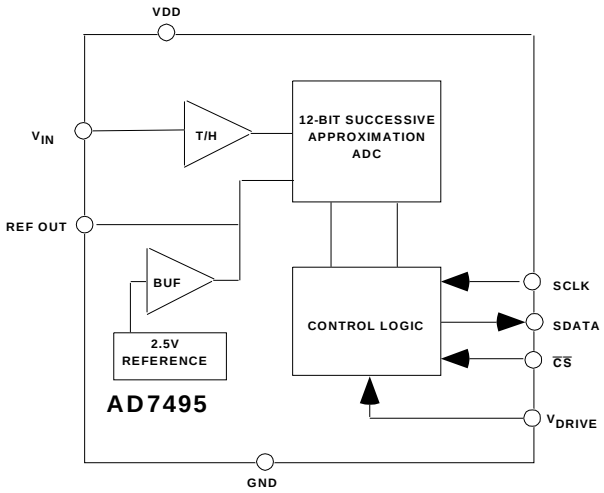
The analog input range for the part is 0 to REF IN. The +2.5V reference for the AD7475 is applied externally to the REF IN pin while the AD7495 has an onboard 2.5V reference. The conversion rate is determined by the SCLK.

PRODUCT HIGHLIGHTS

1. High Throughput with Low Power Consumption
   The AD7475 offers 1MSPS throughput rates with 3mW power consumption.
2. Single Supply Operation with V_{DRIVE} Function.
   The AD7475/AD7495 operate from a single +2.7V to +5 V supply. The V_{DRIVE} function allows the serial interface to connect directly to either 3V or 5V processor systems independant of V_{DD}.
3. Flexible Power/Serial Clock Speed Management
   The conversion rate is determined by the serial clock allowing the power to be reduced as the conversion time is reduced through the serial clock speed increase. The part also features a shutdown mode to maximize power efficiency at lower throughput rates. Power consumption is 1µA max when in shutdown.
4. No Pipeline Delay
   The part features a standard successive-approximation ADC with accurate control of the sampling instant via a CS input and once off conversion control.

FUNCTIONAL BLOCK DIAGRAMS





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AD7475—SPECIFICATIONS[1]

(V_{DD} = +2.7 V to +5.25 V, REF IN = 2.5 V, f_{SCLK} = 20 MHz unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Signal to Noise + Distortion Ratio[2] (SINAD)	69	69	dB min	F_{IN} =455kHz Sine Wave, f_{SAMPLE} = 1Msps
Signal to Noise Ratio (SNR)[2]	70	70	dB min	F_{IN} =455kHz Sine Wave, f_{SAMPLE} = 1Msps
Total Harmonic Distortion (THD)	–76	-76	dB max	F_{IN} = 455kHz Sine Wave, f_{SAMPLE} = 1Msps
Peak Harmonic or Spurious Noise (SFDR)	–76	-76	dB max	F_{IN} =455kHz Sine Wave, f_{SAMPLE} = 1Msps
Intermodulation Distortion (IMD)				
Second Order Terms	–78	-78	dB typ	
Third Order Terms	–78	-78	dB typ	
Aperture Delay	20	20	ns max	
Aperture Jitter	50	50	ps typ	
Full Power Bandwidth	20	20	MHz typ	@ 3 dB
DC ACCURACY				
Resolution	12	12	Bits	
Integral Nonlinearity	±2	±1	LSB max	
Differential Nonlinearity	±0.9	±0.9	LSB max	Guaranteed No Missed Codes to 12 Bits. (B Grade)
Offset Error	±3	±3	LSB max	
Gain Error	±3	±3	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to REF IN		Volts	
DC Leakage Current	±1	±1	µA max	
Input Capacitance	20	20	pF typ	
REFERENCE INPUT				
REF IN Input Voltage Range	2.5	2.5	Volts	±1% for specified performance
dc Leakage Current	±1	±1	µA max	
Input Capacitance	20	20	pF typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.8	2.8	V min	V_{DRIVE} = 5V
	1.8	1.8	V min	V_{DRIVE} = 3V
Input Low Voltage, V_{INL}	0.4	0.4	V max	
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DRIVE} -0.2		V min	I_{SOURCE} = 200 µA; V_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} =200µA
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[3]	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	800	800	ns max	16 SCLK cycles with SCLK at 20MHz
Track/Hold Acquisition Time	300	300	ns max	Sine Wave Input
Throughput Rate	1	1	MSPS max	See Serial Interface Section

AD7475—SPECIFICATIONS[1]

(V_{DD} = +2.7 V to +5.25 V, REF IN = 2.5 V, f_{SCLK} = 20 MHz unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
POWER REQUIREMENTS				
V_{DD}	+2.7/+5.25	+2.7/+5.25	V min/max	
V_{DRIVE}	+2.7/+5.25	+2.7/+5.25	V min/max	
I_{DD}[4]				Digital I/Ps = 0V or V_{DRIVE}.
Normal Mode(Static)	750	750	µA typ	V_{DD} = 4.75V to 5.25V. SCLK on or off.
Normal Mode (Operational)	1.8	1.8	mA max	V_{DD} = 4.75V to 5.25V. F_{SAMPLE} = 1MSPS
	1.25	1.25	mA max	V_{DD} = 2.7V to 3.3V. F_{SAMPLE} = 1MSPS
Partial Power-Down Mode	450	450	µA typ	F_{SAMPLE} = 100kSPS
Partial Power-Down Mode	90	90	µA max	(Static)
Full Power-Down Mode	1	1	µA max	SCLK on or off.
Power Dissipation[4]				
Normal Mode (Operational)	9	9	mW max	V_{DD} = 5V. F_{SAMPLE} = 1MSPS
	3.75	3.75	mW max	V_{DD} = 3V. F_{SAMPLE} = 1MSPS
Partial Power-Down(Static)	450	450	µW max	V_{DD} = 5V.
	270	270	µW max	V_{DD} = 3V.
Full Power-Down	5	5	µW max	V_{DD} = 5 V.
	3	3	µW max	V_{DD} = 3 V.

NOTES

[1]Temperature ranges as follows: A, B Versions: –40°C to +85°C.

[2]SNR calculation includes distortion and noise components.

[3]Sample tested @ +25°C to ensure compliance.

[4]See POWER VERSUS THROUGHPUT RATE section.

Specifications subject to change without notice.

AD7495—SPECIFICATIONS[1] (V_{DD} = +2.7 V to +5.25 V, f_{SCLK} = 20 MHz unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Signal to Noise + Distortion [2] (SINAD)	69	69	dB min	F_{IN} =455kHz Sine Wave, f_{SAMPLE} = 1Msps
Signal to Noise Ratio (SNR)[2]	70	70	dB min	F_{IN} =455kHz Sine Wave, f_{SAMPLE} = 1Msps
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Peak Harmonic or Spurious Noise (SFDR)	–76	-76	dB max	F_{IN} =455kHz Sine Wave, f_{SAMPLE} = 1Msps
Intermodulation Distortion (IMD)				
Second Order Terms	–78	-78	dB typ	
Third Order Terms	–78	-78	dB typ	
Aperture Delay	20	20	ns max	
Aperture Jitter	50	50	ps typ	
Full Power Bandwidth	20	20	MHz typ	@ 3 dB
DC ACCURACY				
Resolution	12	12	Bits	
Integral Nonlinearity	±2	±1	LSB max	
Differential Nonlinearity	±0.9	±0.9	LSB max	Guaranteed No Missed Codes to 12 Bits. (B Grade)
Offset Error	±3	±3	LSB max	
Gain Error	±3	±3	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to 2.5	0 to 2.5	Volts	
DC Leakage Current	±1	±1	µA max	
Input Capacitance	20	20	pF typ	
REFERENCE OUTPUT				
REF OUT Output Voltage	2.5	2.5	V typ	
REF OUT Impedance	tbd	tbd		
REF OUT Temperature Coefficient	50	50	ppm/°C typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.8	2.8	V min	V_{DRIVE} = 5V
	1.8	1.8	V min	V_{DRIVE} = 3V
Input Low Voltage, V_{INL}	0.4	0.4	V max	
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DRIVE} -0.2		V min	I_{SOURCE} = 200 µA; V_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} =200µA
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[3]	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	800	800	ns max	16 SCLK cycles with SCLK at 20MHz
Track/Hold Acquisition Time	300	300	ns max	Sine Wave Input
Throughput Rate	1	1	MSPS max	See Serial Interface Section.

AD7495–SPECIFICATIONS[1] (V_{DD} = +2.7 V to +5.25 V, f_{SCLK} = 20MHz unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
POWER REQUIREMENTS				
V_{DD}	+2.7/+5.25	+2.7/+5.25	V min/max	
V_{DRIVE}	+2.7/+5.25	+2.7/+5.25	V min/max	
I_{DD}[4]				Digital I/Ps = 0V or V_{DRIVE}.
Normal Mode(Static)	1.1	1.1	mA typ	V_{DD} = 4.75V to 5.25V. SCLK on or off.
Normal Mode (Operational)	2.5	2.5	mA max	V_{DD} = 4.75V to 5.25V. F_{SAMPLE} = 1MSPS
	1.7	1.7	mA max	V_{DD} = 2.7V to 3.3V. F_{SAMPLE} = 1MSPS
Partial Power-Down Mode			µA typ	F_{SAMPLE} = 100kSPS
Partial Power-Down Mode	190	190	µA max	(Static)
Full Power-Down Mode	90	90	µA typ	V_{DD} = 4.75V to 5.25V F_{SAMPLE} = 1kSPS
Full Power-Down Mode	1	1	µA max	(Static) SCLK on or off.
Power Dissipation[4]				
Normal Mode (Operational)	12.5	12.5	mW max	V_{DD} = 5V. F_{SAMPLE} = 1MSPS
	5.1	5.1	mW max	V_{DD} = 3V. F_{SAMPLE} = 1MSPS
Partial Power-Down(Static)	950	950	µW max	V_{DD} = 5V.
	570	570	µW max	V_{DD} = 3V.
Full Power-Down	5	5	µW max	V_{DD} = 5 V.
	3	3	µW max	V_{DD} = 3 V.

NOTES
[1]Temperature ranges as follows: A, B Versions: –40°C to +85°C.
[2]SNR calculation includes distortion and noise components.
[3]Sample tested @ +25°C to ensure compliance.
[4]See POWER VERSUS THROUGHPUT RATE section.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +2.7 V to +5.25 V, REF IN = 2.5 V (AD7475); T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} AD7475/AD7495	Units	Description
f_{SCLK}[2]	10	kHz min	
	20	MHz max	
$t_{CONVERT}$	16* t_{SCLK}		t_{SCLK}= 1/f_{SCLK}
	800	ns max	f_{SCLK} = 20MHz
t_{quiet}	100	ns min	Minimum Quiet Time required between conversions
t_2	10	ns min	CS to SCLK Setup Time
t_3[3]	12	ns max	Delay from CS Until SDATA 3-State Disabled
t_4[3]	40	ns max	Data Access Time After SCLK Falling Edge
t_5	0.4t_{SCLK}	ns min	SCLK Low Pulse Width
t_6	0.4t_{SCLK}	ns min	SCLK High Pulse Width
t_7	10	ns min	SCLK to Data Valid Hold Time
t_8[4]	10	ns min	SCLK falling Edge to SDATA High Impedance
	25	ns max	SCLK falling Edge to SDATA High Impedance
t_9[4]	15	ns max	CS rising Edge to SDATA High Impedance
$t_{power-up}$	200	µs typ	Power up time from Full power-down

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 Volts. See Figure 2.

[2]Mark/Space ratio for the SCLK input is 40/60 to 60/40.

[3]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.0 V.

[4]t_8 and t_9 are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 25 pF capacitor. This means that the times, t_8 and t_9, quoted in the timing characteristics are the true bus relinquish time of the part and are independent of the bus loading.

Specifications subject to change without notice.

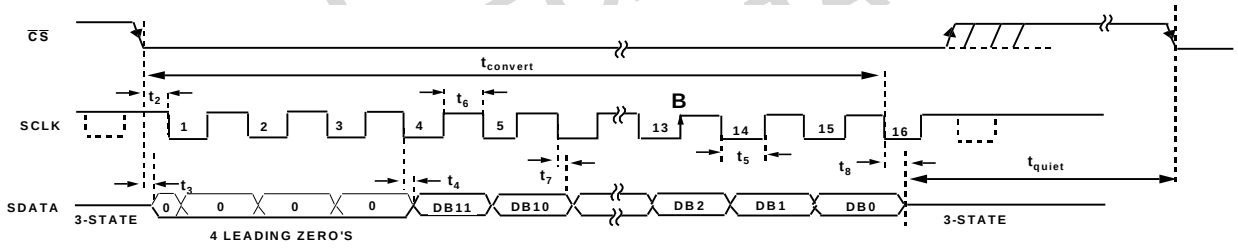


Figure 1. Serial Interface Timing Diagram

Timing Example 1: Having f_{SCLK} = 20 MHz and a Throughput of 1 MSPS, gives a cycle time of t_2 + 12.5(1/f_{SCLK}) + t_{acq} = 1 µs. With t_2 = 10 ns min, this leaves t_{acq} to be 365 ns. This 365 ns satisfies the requirement of 300 ns for t_{acq}. From figure 2, t_{acq} comprises of 2.5(1/f_{SCLK}) + t_8 + t_{quiet}, t_8 = 25 ns. This allows a value of 215 ns for t_{quiet} satisfying the minimum requirement of 100ns.

Timing Example 2: Having f_{SCLK} = 5 MHz and a Throughput of 315 KSPS, gives a cycle time of t_2 + 12.5(1/f_{SCLK}) + t_{acq} = 3.174 µs. With t_2 = 10 ns min, this leaves t_{acq} to be 664 ns. This 664 ns satisfies the requirement of 300 ns for t_{acq}. From figure 2, t_{acq} comprises of 2.5(1/f_{SCLK}) + t_8 + t_{quiet}, t_8 = 25 ns. This allows a values of 139 ns for t_{quiet} satisfying the minimum requirement of 100ns. As in this example and with other slower clock values, the signal may already be acquired before the conversion is complete, but it is still necessary to leave 100 ns minimum t_{quiet} between conversions. In example 2 the signal should be fully acquired at approximately point C in figure 2.

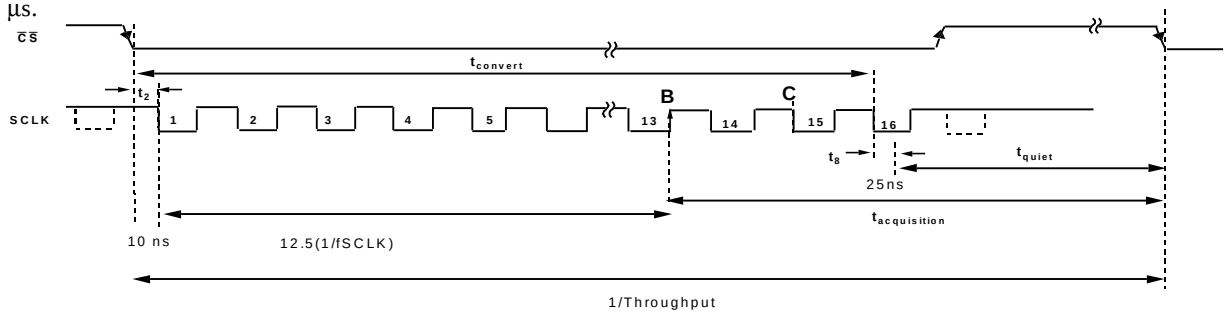


Figure 2. Serial Interface Timing Example

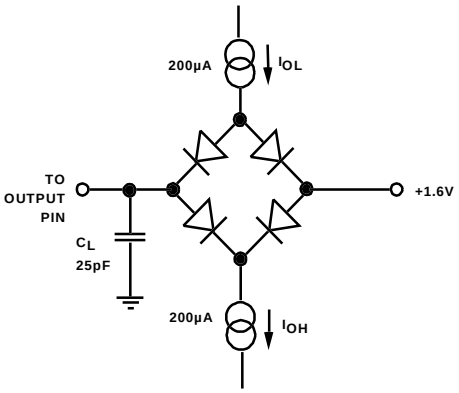
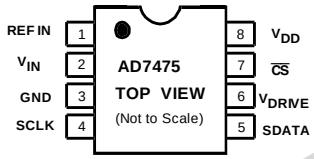
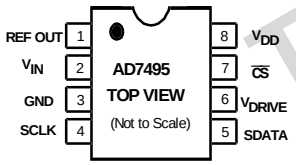


Figure 3. Load Circuit for Digital Output Timing Specifications

AD7475 PINCONFIGURATION SOIC/ µSOIC



AD7495 PINCONFIGURATION SOIC/ µSOIC



ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	–0.3 V to 7 V
V_{DRIVE} to GND	–0.3 V to V_{DD} + 0.3 V
Analog Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND	–0.3 V to V_{DD} + 0.3 V
REF IN to GND	–0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2]	±10 mA
Operating Temperature Range	
Commercial (A Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
SOIC, µSOIC Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	157°C/W (SOIC)
	205.9°C/W (µSOIC)
θ_{JC} Thermal Impedance	56°C/W (SOIC)
	43.74°C/W (µSOIC)
Lead Temperature, Soldering	
Vapor Phase (60 secs)	+215°C
Infared (15 secs)	+220°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100 mA will not cause SCR latch up.

ORDERING GUIDE

Model	Range	Linearity Error (LSB)[1]	Package Option[2]	Branding
AD7495AR	-40°C to +85°C	±2	SO-8	AD7495AR
AD7495BR	-40°C to +85°C	±1	SO-8	AD7495BR
AD7495ARM	-40°C to +85°C	±2	RM-8	CCA
AD7495BRM	-40°C to +85°C	±2	RM-8	CCB
AD7475AR	-40°C to +85°C	±2	SO-8	AD7475AR
AD7475BR	-40°C to +85°C	±1	SO-8	AD7475BR
AD7475ARM	-40°C to +85°C	±2	RM-8	C9A
AD7475BRM	-40°C to +85°C	±2	RM-8	C9B
EVAL-AD7495CB[3]	Evaluation Board			
EVAL-AD7475CB[3]	Evaluation Board			
EVAL-CONTROL BOARD[4]	Controller Board			

NOTES

[2]R = SOIC; RM = µSOIC.

[3]This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.

[4]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7475/AD7495 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin No.	Pin Mnemonic	Function
1	REF IN	Reference Input for the AD7475. An external reference must be applied to this input. The voltage range for the external reference is 2.5V±1% for specified performance.
	REF OUT	Reference Output for the AD7495. A minimum 100nF capacitance is required from this pin to GND. The internal reference can be taken from this pin but buffering is required before it is applied elsewhere in a system.
2	V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0 to REFIN.
3	GND	Analog Ground. Ground reference point for all circuitry on the AD7475/AD7495. All analog input signals and any external reference signal should be referred to this GND voltage. Both of these pins should connect to the AGND plane of a system.
4	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7475/AD7495's conversion process.
5	SDATA	Data Out. Logic Output. The conversion result from the AD7475/AD7495 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream consists of four leading zeros followed by the 12 bits of conversion data which is provided MSB first.
6	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines what voltage the interface of the AD7475/AD7495 will operate at.
7	CS	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7475/AD7495 and also frames the serial data transfer.
8	V_{DD}	Power Supply Input. The V_{DD} range for the AD7475/AD7495 is from +2.7V to +5.25V.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e AGND + 0.5 LSB

Gain Error
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., V_{REF} – 1.5 LSB) after the offset error has been adjusted out.

Track/Hold Acquisition Time
The track/hold amplifier returns into track mode on the 13th SCLK rising edge (see Serial Interface section). Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±0.5 LSB, after the return from track.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

Signal to (*Noise* + *Distortion*) = (6.02 *N* + 1.76) *dB*

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7475/ AD7495, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7475/AD7495 are tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

PSR (Power Supply Rejection)
Variations in power supply will affect the full-scale transition, but not the conveter's linearity. Power Supply Rejection is the maximum change in the full-scale transition point due to a change in power-supply voltage from the nominal value.

AD7475/AD7495 PERFORMANCE CURVES

Figure 4 shows a typical FFT plot for the AD7475 at 1MHz sample rate and 100kHz input frequency.

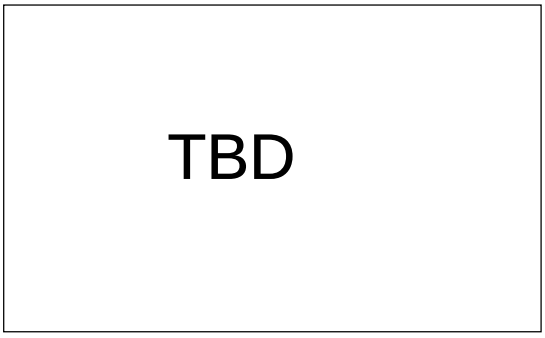


Figure 4. AD7475 Dynamic Performance

Figure 5 shows the SNR versus frequency for a 5V supply.

Figure 5. AD7475 SNR vs Input Frequency

CIRCUIT INFORMATION

The AD7475/AD7495 are fast, micro-power, 12-bit, single supply, A/D converters. The parts can be operated from a +2.7V to +5.25V supply. When operated from either a +5V supply or a +3V supply, the AD7475/ AD7495 are capable of throughput rates of 1Msps when provided with a 20MHz clock.

The AD7475/AD7495 provide the user with an on-chip track/hold, A/D converter, and a serial interface housed in either an 8-pin SOIC or µSOIC package, which offers the user considerable space saving advantages over alternative solutions. The AD7495 also has an on-chip 2.5V reference. The serial clock input accesses data from the part but also provides the clock source for the successive-approximation A/D converter. The analog input range is 0 to REF IN for the AD7475 or 0 to REF OUT for the AD7495.

The AD7475/AD7495 also feature power-down options to allow power saving between conversions. The power-down feature is implemented across the standard serial interface as described in the "Modes of Operation" section.

CONVERTER OPERATION

The AD7475/AD7495 are 12-bit successive approximation analog-to -digital converters based around a capacitive DAC. The AD7475/95 can convert analog input signals in the range 0 V to V_{REF}. Figures 6 and 7 show simplified schematics of the ADC. The ADC comprises of Control Logic, SAR and a Capacitive DAC, which are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. Figure 6 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on V_{IN}.

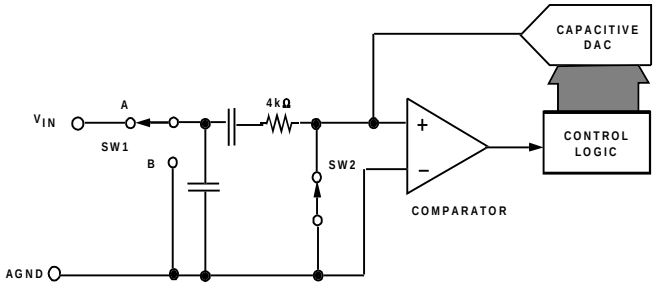


Figure 6. ADC Acquisition Phase

When the ADC starts a conversion, see figure 7, SW2 will open and SW1 will move to position B causing the comparator to become unbalanced. The Control Logic and the Capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced the conversion is complete. The Control Logic generates the ADC output code. Figure 8 shows the ADC transfer function.

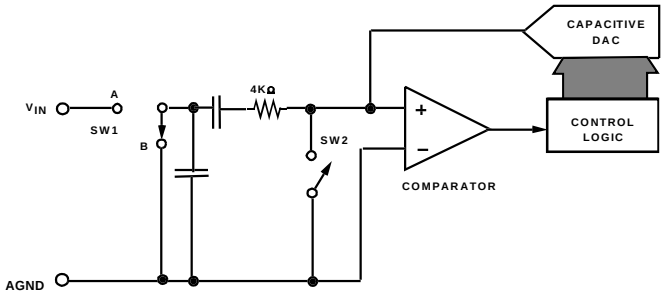


Figure 7. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the AD7475/AD7495 is straight binary. The designed code transitions occur at successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, etc.). The LSB size is = $V_{REF}/4096$. The ideal transfer characteristic for the AD7475/AD7495 is shown in figure 8 below.

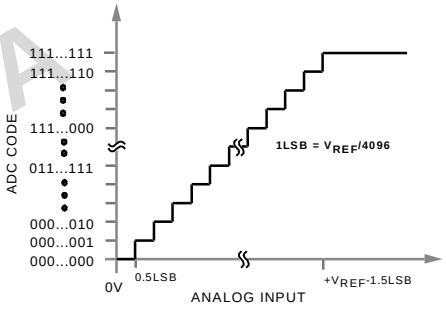


Figure 8. AD7475/AD7495 Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 9 and figure 10 show a typical connection diagram for the AD7475 and AD7495 respectively. In both set-ups the GND pin is connected to the analog ground plane of the system. In figure 9 REF IN is connected to a decoupled 2.5V supply from a reference source, the AD780, to provide an analog input range of 0V to 2.5V. Although the AD7475 is connected to a V_{DD} of +5V, the serial interface is connected to a +3V microprocessor. The V_{DRIVE} pin of the AD7475 is connected to the same +3V supply of the microprocessor to allow a 3V logic interface, see 'Digital Inputs. In figure 10, the REF OUT pin of the AD7495 is connected to a buffer and then applied to a level shifting circuit used on the analog input to allow a bipolar signal to be applied to the AD7495. A minimum 100nF capacitance is required on the REF OUT pin to GND. The conversion result from both ADCs is output in a 16-bit word with four leading zeroes followed by the MSB of the 12-bit result. For applications where power consumption is of concern, the power-down modes should

be used between conversions or bursts of several conversions to improve power performance. See Modes of Operation section of the datasheet.

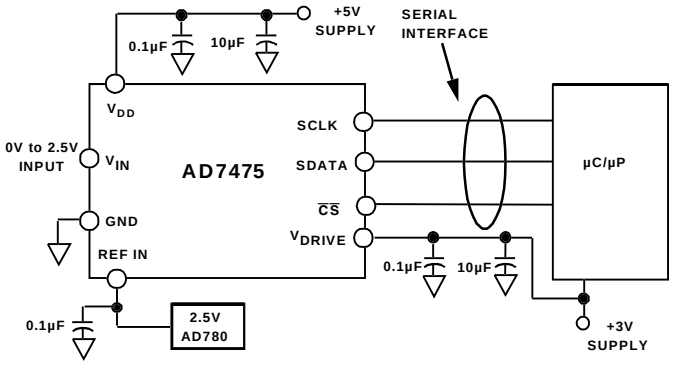


Figure 9. AD7475 Typical connection Diagram

conducting current into the substrate. 20mA is the maximum current these diodes can conduct without causing irreversable damage to the part. The capacitor C1 in figure 11 is typically about 4pF and can primarily be attributed to pin capacitance. The resistor R1 is a lumped component made up of the on resistance of a switch. This resistor is typically about 100Ω. The capacitor C2 is the ADC sampling capacitor and has a capacitance of 16pF typically.For ac applications, removing high frequency components from the analog input signal is recommended by use of an RC low-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal to noise ratio are critical the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp will be a function of the particular application.

When no amplifier is used to drive the analog input the source impedance should be limited to low values. The maximum source impedance will depend on the amount of

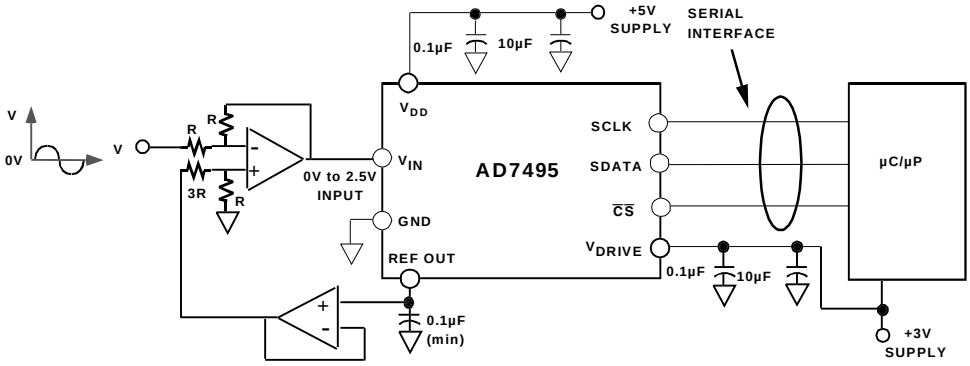


Figure 10. AD7495 Typical connection Diagram

Analog Input

Figure 11 shows an equivalent circuit of the analog input sturcture of the AD7475/AD7495. The two diodes D1 and D2 provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 200mV. This will cause these diodes to become forward biased and start

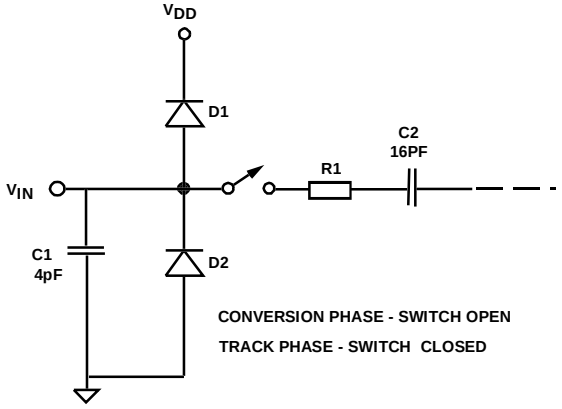


Figure 11. Equivalent Analog Input Circuit

total harmonic distortion (THD) that can be tolerated. The THD will increase as the source impedance increases and performance will degrade. Figure 12 shows a graph of the total harmonic distortion versus analog input signal frequency for different source impedances.

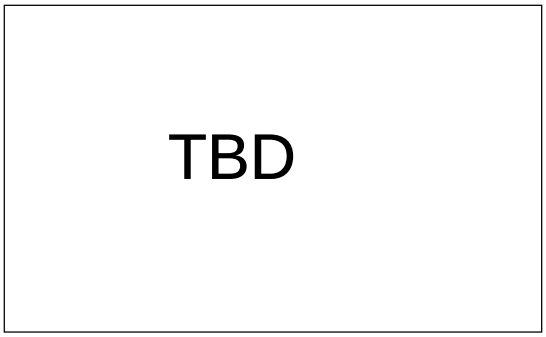


Figure 12. THD vs. Analog Input Frequency

Reference Section

An external reference source should be used to supply the 2.5 V reverence to the AD7475. Errors in the reference source will result in gain errors in the AD7475 transfer function and will add the specified full scale errors on the part. A capacitor of at least 0.1 uF should be placed on the REF IN pin. Suitable reference sources for the AD7475 include the AD780, the AD680 and the AD1852.

The AD7495 contains an on chip 2.5 V reference. As shown in Figure 13 the voltage that appears at the REF OUT pin is internally buffered before being applied to the ADC, the output impedence of this buffer is typically 10 Ohms. The reference is capable of sourcing up to 2 mA. The REF OUT pin should be decoupled to AGND using a 100nF or greater capacitor.

If the 2.5 V internal reference is to be used to drive another device that is capable of glitching the reference at critical times, then the reference will have to be buffered before driving the device. To esure optimum performance of the AD7495 it is recommended that the Internal Reference not be over driven.

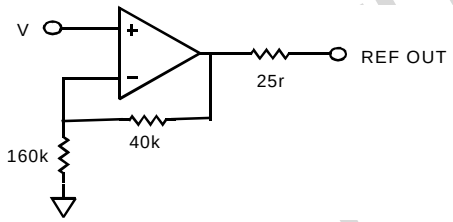


Figure 13. AD7495 Reference Circuit

MODES OF OPERATION

The mode of operation of the AD7475/AD7495 is selected by controlling the (logic) state of the CS signal during a conversion. There are three possible modes of operation, Normal Mode, Partial Power-Down Mode and Full Power-Down Mode. The point at which CS is pulled high after the conversion has been initiated will determine which power-down mode, if any, that the device will enter. Similarly, if already in a power-down mode then CS can control whether the device will return to Normal operation or remain in power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements.

Normal Mode

This mode is intended for fastest throughput rate performance as the user does not have to worry about any power-up times with the AD7475/AD7495 remaining fully-powered all the time. Figure 14 shows the general diagram of the operation of the AD7475/AD7495 in this mode.

The conversion is iniated on the falling edge of CS as described in the Serial Interface section. To ensure the part remains fully powered up at all times CS must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of CS. If CS is brought high any time after the 10th SCLK falling edge but before the 16th SCLK falling edge the part will remain powered up but the conversion will be terminated and SDATA will go back into tri-state. Sixteen serial clock cycles are required to complete the conversion and access the conversion result. CS may idle high until the next conversion or may idle low until sometime prior to the next conversion, (effectively idling CS low).

Once a data transfer is complete (SDATA has returned to tri-state), another conversion can be initiated after the quiet time, t_{quiet}, has elapsed by bringing CS low again.

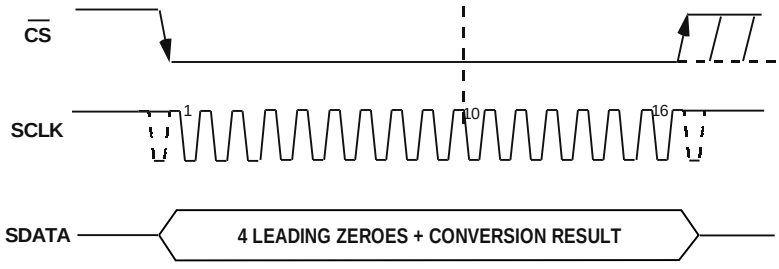


Figure 14. Normal Mode Operation

Partial Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required; either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate and then the ADC is powered down for a relatively long duration between these bursts of several conversions. When the AD7475 is in partial power down, all analog circuitry is powered down except for the bias current generator and in the case of the AD7495 all analog circuitry is powered down except for the on-chip reference and reference buffer.

To enter Partial Power-Down, the conversion process must be interrupted by bringing CS high anywhere after the second falling edge of SCLK and before the tenth falling edge of SCLK as shown in Figure 15. Once CS has been brought high in this window of SCLKs, then the part will enter partial power down and the conversion that was intiated by the falling edge of CS will be terminated and SDATA will go back into tri-state. If CS is brought high before the second SCLK falling edge, then the part will remain in Normal Mode and will not power-down. This will avoid accidental powerdown due to glitches on the CS line.

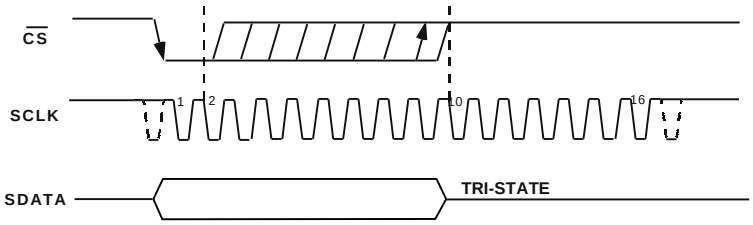


Figure 15. Entering Partial Power-Down Mode

In order to exit this mode of operation and power the AD7475/AD7495 up again, a dummy conversion is performed. On the falling edge of CS the device will begin to power up, and will continue to power up as long as CS is held low until after the falling edge of the tenth SCLK. The device will be fully powered up once 16 SCLKs have elapsed and valid data will result from the next conversion as shown in figure 16. If CS is brought high before the second falling edge of SCLK, then the AD7475/AD7495 will go back into partial power down again. This avoids accidental power up due to glitches on the CS line, as although the device may begin to power up on the falling edge of CS, it will power down again on the rising edge of CS. If in Partial Power-Down and CS is brought high between the second and tenth falling edges of SCLK then the device will enter Full Power Down Mode.

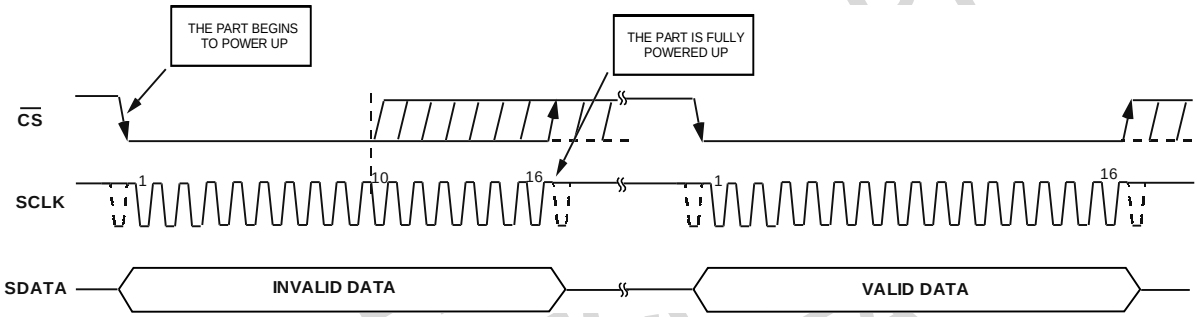


Figure 16. Exiting Partial Power-Down Mode

Full Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required than that in the Partial Power Down Mode, as power up from a full power down would not be complete in just one dummy conversion. This mode is more suited to applications where a series of conversions performed at a relatively high throughput rate would be followed by a long period of inactivity and hence power down. When the AD7475/AD7495 is in full power down, all analog circuitry is powered down. See Power-up Times section.

Full Power-Down is entered in a similar way as partial power down except the timing sequence shown in Figure 15 must be executed twice.The conversion process must be interrupted in a similar fashion by bringing CS high anywhere after the second falling edge of SCLK and before the tenth falling edge of SCLK. The device will enter partial power down at this point. To reach full power down, the next conversion cycle must be interrupted in the same way as shown in Figure 17. Once CS has been brought high in this window of SCLKs, then the part will power down completely.

NOTE: It is not necessary to complete the 16 SCLKs once CS has been brought high to enter a power down mode.

To exit Full Power Down, and power the AD7475/AD7495 up again, a dummy conversion is performed as when powering up from partial power down. On the falling edge of CS the device will begin to power up, and will continue to power up as long as CS is held low until after the falling edge of the tenth SCLK. The power up time is longer than one dummy conversion cycle however and this time must elapse before a conversion can be initaited as shown in Figure 18. See Power-up Times section for the power up times associated with the AD7475 and the AD7495.

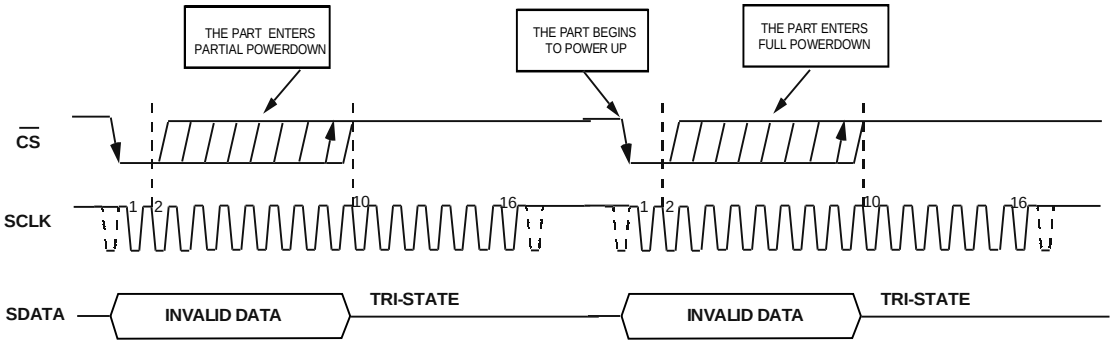


Figure 17. Entering Full Power-Down Mode

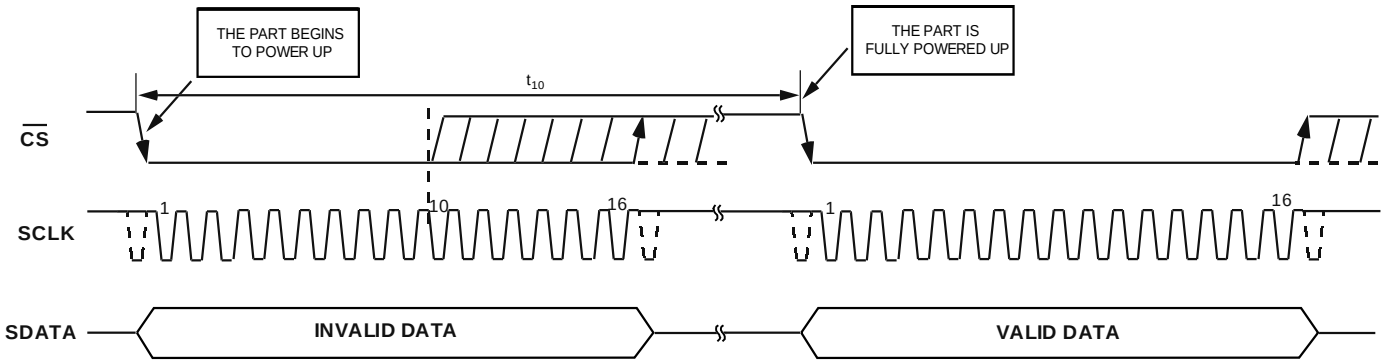


Figure 18. Exiting Full Power-Down Mode

SERIAL INTERFACE

Figure 19 shows the detailed timing diagram for serial interfacing to the AD7475/AD7495. The serial clock provides the conversion clock and also controls the transfer of information from the AD7475/AD7495 during conversion.

CS initiates the data transfer and conversion process. The falling edge of CS puts the track and hold into hold mode, takes the bus out of tristate and the analog input is sampled at this point. The conversion is also initiated at this point and will require 16 SCLK cycles to complete. Once 13 SCLK falling edges have elapsed, then the track and hold will go back into track on the next SCLK rising edge as shown in figure 19. On the 16th SCLK falling edge the SDATA line will go back into tristate. If the rising edge of CS occurs before 16 SCLKs have elapsed, then the conversion will be terminated and the SDATA line will go back into tri-state, as shown in figure 20, otherwise SDATA returns to tristate on the 16th SCLK falling edge as shown in figure 19.

Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7475/95. CS going low provides the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges beginning with the 2nd leading zero, thus the first falling clock edge on the serial clock has the second leading zero provided. The final bit in the data transfer is valid on the sixteenth falling edge, having being clocked out on the previous (15th) falling edge. In applications with a slower SCLK, it may be possible to read in data on each SCLK rising edge, i.e. the first rising edge of SCLK after the CS falling edge would provide the first leading zero and the 15th rising SCLK edge would have DB0 provided.

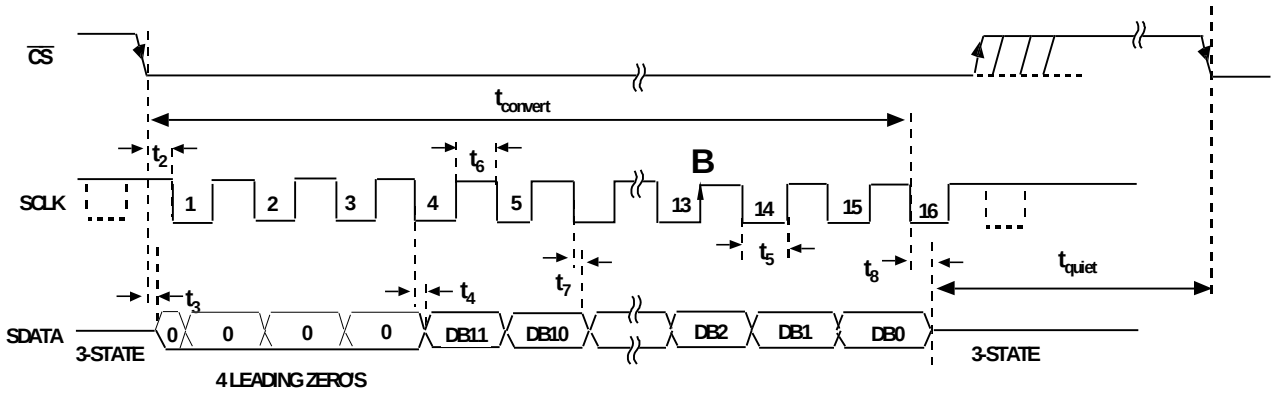


Figure 19. Serial Interface Timing Diagram

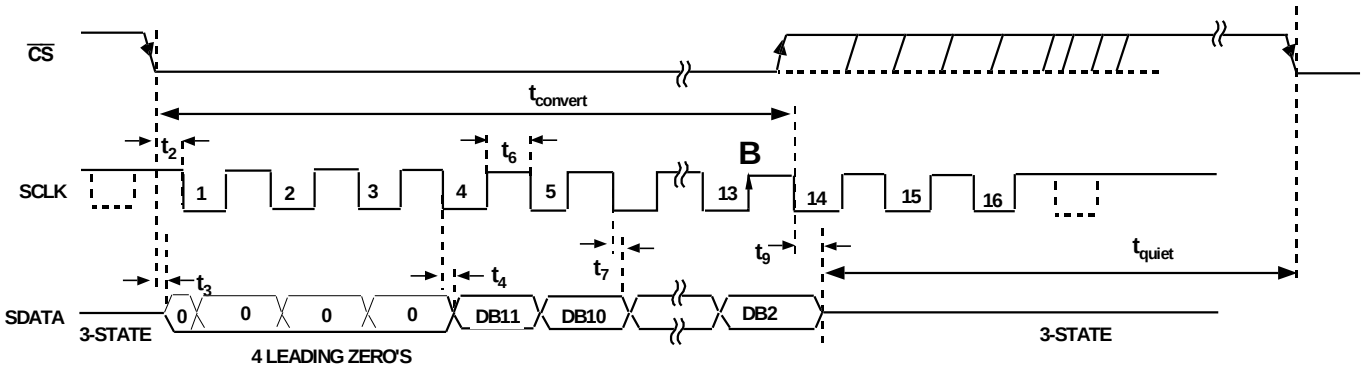


Figure 20. Serial Interface Timing Diagram

MICROPROCESSOR INTERFACING

The serial interface on the AD7475/AD7495 allows the parts to be directly connected to a range of many different microprocessors. This section explains how to interface the AD7475/AD7495 with some of the more common microcontroller and DSP serial interface protocols.

AD7475/AD7495 to TMS320C5x/C54x

The serial interface on the TMS320C5x/C54x uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices like the AD7475/AD7495. The CS input allows easy interfacing between the TMS320C5x/C54x and the AD7475/AD7495 without any glue logic required. The serial port of the TMS320C5x/C54x is set up to operate in burst mode with internal CLKX (TX serial clock) and FSX (TX frame sync). The serial port control register (SPC) must have the following setup: FO = 0, FSM = 1, MCM = 1 and TXM = 1. The format bit, FO, may be set to 1 to set the word length to 8-bits, in order to implement the power-down modes on the AD7475/AD7495. The connection diagram is shown in Figure 21. It should be noted that for signal processing applications, it is imperative that the frame synchronisation signal from the TMS320C5x/C54x will provide equidistant sampling.The V_{DRIVE} pin of the AD7475/AD7495 takes the same supply voltage as that of the TMS320C5x/C54x. This allows the ADC to operate at a higher voltage than the serial interface, i.e. TMS320C5x/C54x, if necessary.

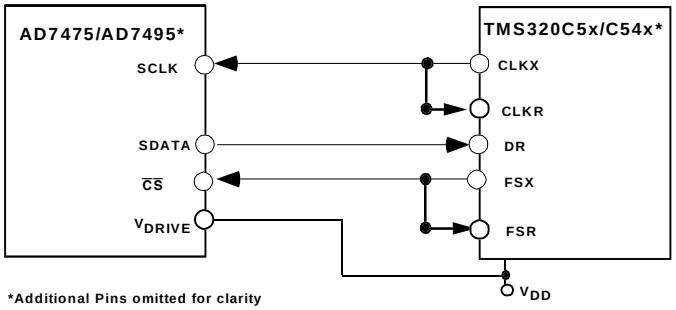


Figure 21. Interfacing to the TMS320C5x

AD7475/AD7495 to ADSP21xx

The ADSP21xx family of DSPs are interfaced directly to the AD7475/AD7495 without any glue logic required. The V_{DRIVE} pin of the AD7475/AD7495 takes the same supply voltage as that of the ADSP21xxx. This allows the ADC to operate at a higher voltage than the serial interface, i.e. ADSP21xxx, if necessary.

The SPORT control register should be set up as follows:

TFSW = RFSW = 1, Alternate Framing
INVRFS = INVTFS = 1, Active Low Frame Signal
DTYPE = 00, Right Justify Data
SLEN = 1111, 16-Bit Data words
ISCLK = 1, Internal serial clock
TFSR = RFSR = 1, Frame every word
IRFS = 0,
ITFS = 1.

To implement the power-down modes SLEN should be set to 1001 to issue an 8-bit SCLK burst.

The connection diagram is shown in Figure 22. The ADSP21xx has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in Alternate Framing Mode and the SPORT control register is set up as described. The Frame synchronisation signal generated on the TFS is tied to CS and as with all signal processing applications

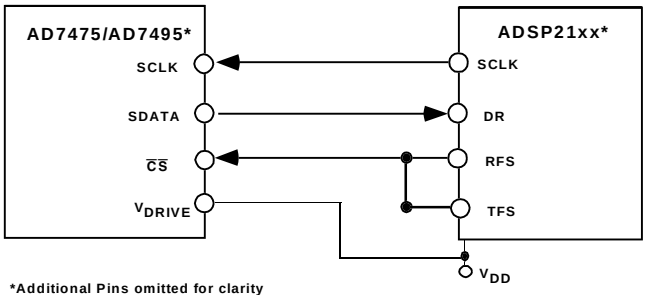


Figure 22. Interfacing to the ADSP-21xx

equidistant sampling is necessary. However, in this example, the timer interrupt is used to control the sampling rate of the ADC and under certain conditions, equidistant sampling may not be acheived.

The Timer registers etc. are loaded with a value which will provide an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and hence the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instrustion to transmit with TFS is given, (i.e. AX0=TX0), the state of the SCLK is checked. The DSP will wait until the SCLK has gone High, Low and High before transmission will start. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, then the data may be transmitted or it may wait until the next clock edge.

For example, the ADSP2111 has a master clock frequency of 16MHz. If the SCLKDIV register is loaded with the value 3 then a SCLK of 2MHz is obtained, and 8 master clock periods will elapse for every 1 SCLK period. If the timer registers are loaded with the value 803, then 100.5 SCLKs will occur between interrupts and subsequently between transmit instructions. This situation will result in non-equidistant sampling as the transmit instruction is occuring on a SCLK edge. If the number of SCLKs between interrupts is a whole integer figure of N then equidistant sampling will be implemented by the DSP.

AD7475/AD7495 to DSP56xxx

The connection diagram in figure 23 shows how the AD7475/AD7495 can be connected to the SSI (Synchronous Serial Interface) of the DSP56xxx family of DSPs from Motorola. The SSI is operated in Synchronous Mode (SYN bit in CRB =1) with internally generated 1-bit clock period frame sync for both TX and RX (bits FSL1 =1 and FSL0 =0 in CRB). Set the word length to 16 by setting bits WL1 =1 and WL0 = 0 in CRA. To implement the power-down modes on the AD7475/AD7495 then the word length can be changed to 8 bits by setting bits WL1 = 0 and WL0 = 0 in CRA. It should be noted that for signal processing applications, it is imperative that the frame synchronisation signal from the DSP56xxx will provide equidistant sampling. The V_{DRIVE} pin of the AD7475/AD7495 takes the same supply voltage as that of the DSP56xxx. This allows the ADC to operate at a higher voltage than the serial interface, i.e. DSP56xxx, if necessary.

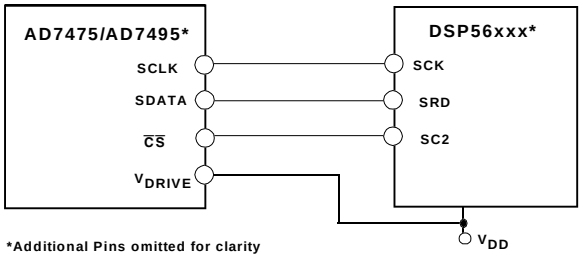


Figure 23. Interfacing to the DSP56xx

AD7475/AD7495 to MC68HC16

The Serial Peripheral Interface (SPI) on the MC68HC16 is configured for Master Mode (MSTR = 1), Clock Polarity Bit (CPOL) = 1 and the Clock Phase Bit (CPHA) = 0. The SPI is configured by writing to the SPI Control Register (SPCR) - see 68HC16 user manual. The serial transfer will take place as a 16-bit operation when the SIZE bit in the SPCR register is set to SIZE = 1. To implement the power-down modes with an 8-bit transfer set SIZE = 0. A connection diagram is shown in figure 24. The V_{DRIVE} pin of the AD7475/AD7495 takes the same supply voltage as that of the MC68HC16. This allows the ADC to operate at a higher voltage than the serial interface, i.e. MC68HC16, if necessary.

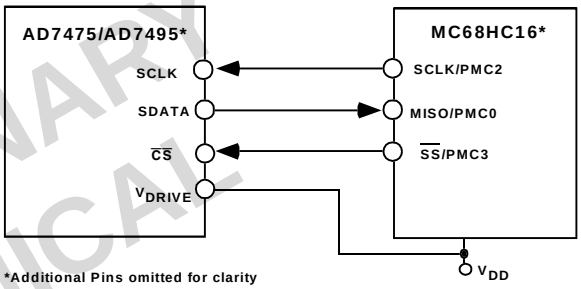
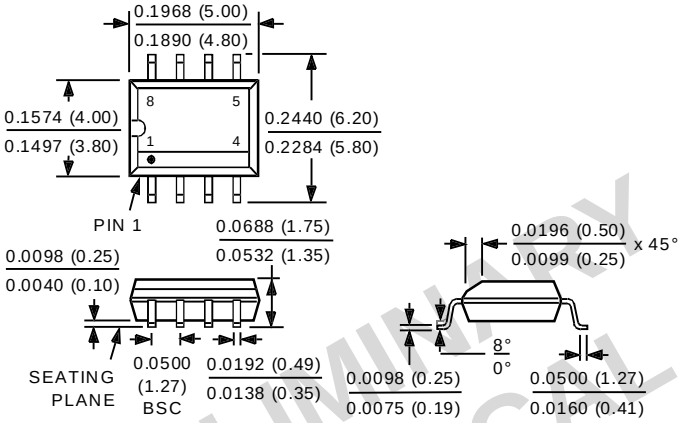


Figure 24. Interfacing to the MC68HC16

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-lead SOIC (SO-8)



8-lead microSOIC (RM-8)