ANALOG DEVICES

Low-Power CMOS Analog Front End with Flash based DSP Microcomputer

Preliminary Technical Data — AD73511

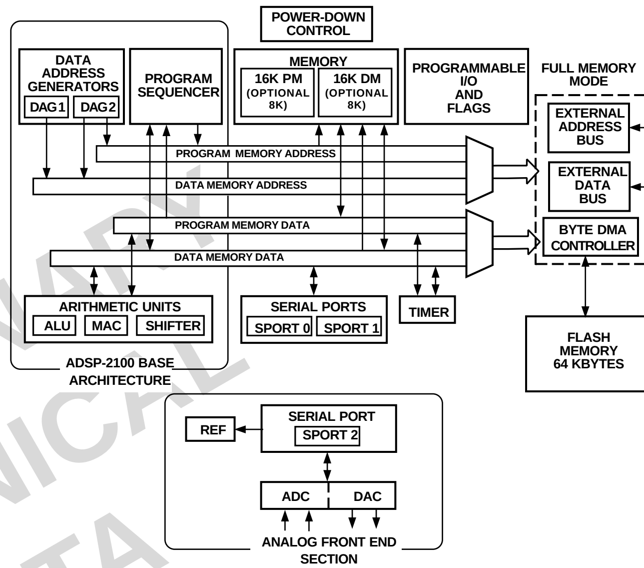
FEATURES

AFE PERFORMANCE
16-Bit A/D Converter
16-Bit D/A Converter
Programmable Input/Output Sample Rates
77 dB ADC SNR
77 dB DAC SNR
64 kS/s Maximum Sample Rate
–90 dB Crosstalk
Low Group Delay (25 µs typ per ADC Channel, 50 µs typ per DAC Channel)
Programmable Input/Output Gain
On-Chip Reference

DSP PERFORMANCE
19 ns Instruction Cycle Time @ 3.3 Volts, 52 MIPS Sustained Performance
AD73511-80
80K Bytes of On-Chip RAM, Configured as 16K Words Program Memory RAM and 16K Words Data Memory RAM
AD73511-40
40K Bytes of On-Chip RAM, Configured as 8K Words Program Memory RAM and 8K Words Data Memory RAM

FLASH Memory
64 kbytes
Writable in pages of 128 bytes
Fast Page Write Cycle of 5 ms (typical)

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD73511 is a single-device incorporating a single analog front end, microcomputer optimized for digital signal processing (DSP) and a FLASH based boot memory for the DSP.

The AD73511's analog front end (AFE) section is suitable for general purpose applications including speech and telephony. The AFE section features a 16-bit A/D converter and a 16-bit D/A converter. Each converter provides 77 dB signal-to-noise ratio over a voiceband signal bandwidth.

The AD73511 is particularly suitable for a variety of applications in the speech and telephony area including low bit rate, high quality compression, speech enhancement, recognition and synthesis. The low group delay characteristic of the AFE makes it suitable for single or multichannel active control applications. The A/D and D/A conversion channels feature programmable input/ouput gains with ranges 38 dB and 21 dB respectively. An on-chip reference voltage is included to allow single supply operation.

The sampling rate of the AFE is programmable with four separate settings offering 64, 32, 16 and 8 kHz sampling rates (from a master clock of 16.384 MHz) while the serial port (SPORT2) allows easy expansion of the number of I/O channels by cascading extra AFEs external to the AD73511.

The AD73511's DSP engine combines the ADSP-2100 family base architecture (three computational units, data address generators and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, Flag I/O, extensive interrupt capabilities and on-chip program and data memory.

The AD73511-80 integrates 80K bytes of on-chip memory configured as 16K words (24-bit) of program RAM, and 16K words (16-bit) of data RAM. The AD73511-40 integrates 40K bytes of on-chip memory configured as 8K words (24-bit) of program RAM, and 8K words (16-bit) of data RAM. Both devices feature a Flash memory array of 64 kbytes (512 kbits) connected to the DSP's byte-wide DMA port (BDMA). This allows non-volatile storage of the DSP's boot code and system data parameters. Power-down circuitry is also provided to meet the low power needs of battery operated portable equipment. The AD73511 is available in a 119-ball PBGA package.

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ARCHITECTURE OVERVIEW

The AD73511 instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The AD73511 assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

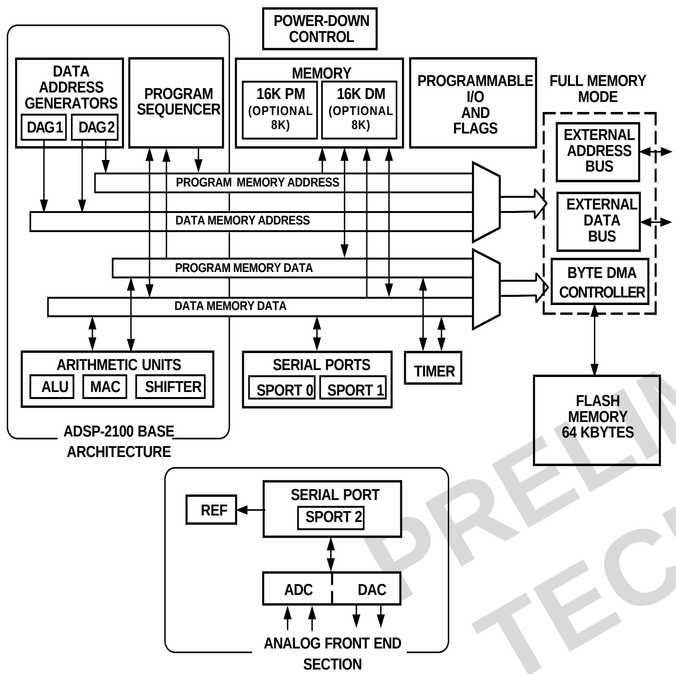


Figure 1. Functional Block Diagram

Figure 1 is an overall block diagram of the AD73511. The processor section contains three independent computational units: the ALU, the multiplier/accumulator (MAC) and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization and derive exponent operations.

The internal result (R) bus connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the AD73511 executes looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

An interface to low cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The AD73511 can respond to eleven interrupts. There can be up to six external interrupts (one edge-sensitive, two level-sensitive and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORTs), the Byte DMA port and the power-down circuitry. There is also a master RESET signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation.

Each port can generate an internal programmable serial clock or accept an external serial clock.

The AD73511 provides up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, there are eight flags that are programmable as inputs or outputs and three flags that are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) is decremented every *n* processor cycle, where *n* is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

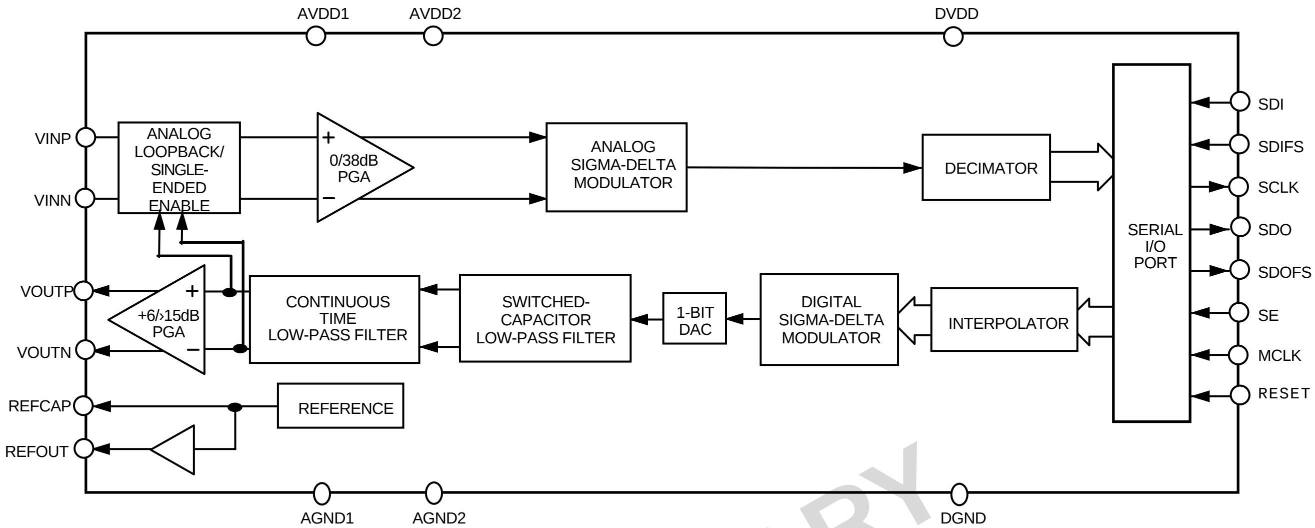


Figure 2: Functional Block Diagram of Analog Front End Section

Analog Front End

The AFE section is configured as a separate block which is normally connected to either SPORT0 or SPORT1 of the DSP section. As it is not hard-wired to either SPORT the user has total flexibility in how they wish to allocate system resources to support the AFE. It is also possible to further expand the number of analog I/O channels connected to the SPORT by cascading other single or dual channel AFEs (AD73311 or AD73322) external to the AD73511.

The AFE is configured as a single I/O channel (similar to that of the discrete AD73311L - refer to the AD73311L datasheet for more details) having a 16-bit sigma-delta based ADC and DAC. Both ADC and DAC share a common reference whose nominal value is 1.2V. Figure 2 shows a block diagram of the AFE section of the AD73511. It shows an ADC and DAC as well as a common reference. Communication to both channels is handled by the SPORT2 block which interfaces to either SPORT0 or SPORT1 of the DSP section.

The I/O channel features fully differential inputs and outputs. The input section allows direct connection to the internal Programmable Gain Amplifier at the input of the sigma-delta ADC section. The input section also features programmable differential channel inversion and configuration of the the differential input as two separate single-ended inputs. The ADC features a second order sigma-delta modulator which samples at MCLK/8. Its bitstream output is filtered and decimated by a Sinc-cubed decimator to provide a sample rate selectable from 64 kHz, 32 kHz, 16 kHz or 8 kHz (based on an MCLK of 16.384 MHz).

The DAC channel features a Sinc-cubed interpolator which increases the sample rate from the selected rate to the digital sigma-delta modulator rate of MCLK/8. The digital sigma-delta modulator's output bit-stream is fed to a single-bit DAC whose output is reconstructed/filtered by two stages of low-pass filtering (switched capacitor and continuous time) before being applied to the differential output driver.

AD73511–SPECIFICATIONS

(AVDD = DVDD = +3.0V to 3.6V; DGND = AGND = 0 V, f_{MCLK} = 16.384 MHz, f_{SAMP} = 64 kHz; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER	Min	Typ	Max	Units	Test Conditions
AFE SECTION					
REFERENCE					
REFCAP					
Absolute Voltage, V_{REFCAP}	1.08	1.2	1.32	V	
REFCAP TC		50		ppm/°C	0.1 µF Capacitor Required from REFCAP to AGND2
REFOUT					
Typical Output Impedance		145		Ω	
Absolute Voltage, V_{REFOUT}	1.08	1.2	1.32	V	Unloaded
Minimum Load Resistance	1			kΩ	
Maximum Load Capacitance			100	pF	
ADC SPECIFICATIONS					
Maximum Input Range at VIN[2, 3]		1.578		V p-p	Measured Differentially.
		–2.85		dBm	Max. Input = (1.578/1.2)*V_{REFCAP}
Nominal Reference Level at VIN		1.0954		V p-p	Measured Differentially
(0 dBm0)		–6.02		dBm	
Absolute Gain					
PGA = 0 dB	–2.2	-0.6	+1.0	dB	1.0 kHz, 0 dBm0
PGA = 38 dB		–1.0		dB	1.0 kHz, 0 dBm0
Gain Tracking Error		±0.1		dB	1.0 kHz, +3 dBm0 to –50 dBm0
Signal to (Noise + Distortion)					Refer to Figure 5
PGA = 0 dB	70	76		dB	300 Hz to 3400 Hz;
	70	74		dB	0 Hz to f_{SAMP}/2;
		72		dB	300 Hz to 3400 Hz; f_{SAMP} = 64 kHz
		56		dB	0 Hz to f_{SAMP}/2; f_{SAMP} = 64 kHz
PGA = 38 dB		60		dB	300 Hz to 3400 Hz;
				59	dB 0 Hz to f_{SAMP}/2
Total Harmonic Distortion					
PGA = 0 dB		–85	–70	dB	300 Hz to 3400 Hz;
PGA = 38 dB		–85		dB	300 Hz to 3400 Hz;
Intermodulation Distortion		–82		dB	PGA = 0 dB
Idle Channel Noise		–76		dBm0	PGA = 0 dB
Crosstalk		–100		dB	ADC Input Level: 1.0kHz, 0 dBm0 DAC Input at Idle
DC Offset	–20	+2	+25	mV	PGA = 0 dB
Power Supply Rejection		–84		dB	Input Signal Level at AVDD and DVDD Pins: 1.0 kHz, 100 mV p-p Sine Wave
Group Delay[4, 5]		25		µs	f_{SAMP} = 64 kHz
Input Resistance at PGA[2, 4, 6]		45		kΩ	DMCLK = 16.384 MHz
DAC SPECIFICATIONS					
Maximum Voltage Output Swing[2]					
Single Ended		1.578		V p-p	PGA = 6 dB
		–2.85		dBm	Max. Output = (1.578/1.2)*V_{REFCAP}
Differential		3.156		V p-p	PGA = 6 dB
		3.17		dBm	Max. Output = 2*((1.578/1.2)*V_{REFCAP})
Nominal Voltage Output Swing (0 dBm0)					
Single-Ended		1.0954		V p-p	PGA = 6 dB
		–6.02		dBm	
Differential		2.1909		V p-p	PGA = 6 dB
		0		dBm	
Output Bias Voltage	1.08	1.2	1.32	V	REFOUT Unloaded
Absolute Gain	–1.8	-0.7	+0.4	dB	1.0 kHz, 0 dBm0; Unloaded
Gain Tracking Error		± 0.1		dB	1.0 kHz, +3 dBm0 to –50 dBm0
Signal to (Noise + Distortion) at 0 dBm0					
PGA = 0 dB	70	77		dB	300 Hz to 3400 Hz
			76		dB 300 Hz to 3400 Hz; f_{SAMP} = 64 kHz
PGA = 6 dB		77		dB	300 Hz to 3400 Hz;
		77		dB	300 Hz to 3400 Hz; f_{SAMP} = 64 kHz

PARAMETER	Min	Typ	Max	Units	Test Conditions (STYLE: table col.head)
Total Harmonic Distortion at 0 dBm0					
PGA = 0 dB		-80	–70	dB	
PGA = 6 dB		-80		dB	
Intermodulation Distortion		–85		dB	PGA = 0 dB
Idle Channel Noise		–76		dBm0	PGA = 0 dB
Crosstalk		–100		dB	ADC Input Level: AGND; DAC Output Level: 1.0 kHz, 0 dBm0
Power Supply Rejection		–81		dB	Input Signal Level at AVDD and DVDD Pins: 1.0 kHz, 100 mV p-p Sine Wave
Group Delay[4, 5]		25		μs	f_{SAMP} = 64 kHz; Interpolator Bypassed
		50		μs	f_{SAMP} = 64 kHz
Output DC Offset[2, 7]	–30	+5	+50	mV	PGA = 6 dB
Minimum Load Resistance, R_L[2, 8]					
Single-Ended[4]	150			Ω	
Differential	150			Ω	
Maximum Load Capacitance, C_L[2, 8]					
Single-Ended[4]			500	pF	
Differential			100	pF	
LOGIC INPUTS					
V_{INH}, Input High Voltage	DVDD – 0.8		DVDD	V	
V_{INL}, Input Low Voltage	0		0.8	V	
I_{IH}, Input Current	-10		+10	μA	
C_{IN}, Input Capacitance			10	pF	
LOGIC OUTPUT					
V_{OH}, Output High Voltage	DVDD – 0.4		DVDD	V	|IOUT| - 100 μA
V_{OL}, Output Low Voltage	0		0.4	V	|IOUT| - 100 μA
Three-State Leakage Current	–10		+10	μA	
POWER SUPPLIES					
AVDD1, AVDD2	3.0		3.6	V	
DVDD	3.0		3.6	V	
I_{DD}[10]					See Table I

NOTES

1 Operating temperature range is as follows: –20°C to +85°C. Therefore, T_{MIN} = –20°C and T_{MAX} = +85°C.

2 Test conditions: Input PGA set for 0 dB gain, Output PGA set for 6 dB gain, no load on analog outputs (unless otherwise noted).

3 At input to sigma-delta modulator of ADC.

4 Guaranteed by design.

5 Overall group delay will be affected by the sample rate and the external digital filtering.

6 The ADC's input impedance is inversely proportional to DMCLK and is approximated by: $(3.3 * 10^{11})$/DMCLK.

7 Between VOUTP1 and VOUTN1 or between VOUTP2 and VOUTN2.

8 At VOUT output.

9 Frequency responses of ADC and DAC measured with input at audio reference level (the input level that produces an output level of –10 dBm0), with 38 dB preamplifier bypassed and input gain of 0 dB.

10 Test Conditions: no load on digital inputs, analog inputs ac coupled to ground, no load on analog outputs.

Specifications subject to change without notice.

AD73511–SPECIFICATIONS

(AVDD = DVDD = +3.0V to 3.6V; DGND = AGND = 0 V, f_{MCLK} = 16.384 MHz, f_{SAMP} = 64 kHz; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER		Test Conditions	Min	Typ	Max	Unit
DSP SECTION						
V_{IH}	Hi-Level Input Voltage[1, 2]	@ V_{DD} = max	2.0			V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DD} = max	2.2			V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min			0.8	V
V_{OH}	Hi-Level Output Voltage[1, 4, 5]	@ V_{DD} = min				
		I_{OH} = –0.5 mA	2.4			V
		@ V_{DD} = min				
		I_{OH} = –100 µA[6]	V_{DD} – 0.3			V
V_{OL}	Lo-Level Output Voltage[1, 4, 5]	@ V_{DD} = min				
		I_{OL} = 2 mA			0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DD} = max				
		V_{IN} = V_{DD} max			10	µA
I_{IL}	Lo-Level Input Current[3]	@ V_{DD} = max				
		V_{IN} = 0 V			10	µA
I_{OZH}	Three-State Leakage Current[7]	@ V_{DD} = max				
		V_{IN} = V_{DD} max[8]			10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DD} = max				
		V_{IN} = 0 V[8]			10	µA
I_{DD}	Supply Current (Idle)[9]	@ V_{DD} = 3.3				
		t_{CK} = 19 ns[10]		10		mA
	t_{CK} = 25 ns[10]		8		mA	
t_{CK} = 30 ns[10]		7		mA		
I_{DD}	Supply Current (Dynamic)[11]	@ V_{DD} = 3.3				
		T_{AMB} = +25°C				
		t_{CK} = 19 ns[10]		51		mA
	t_{CK} = 25 ns[10]		41		mA	
t_{CK} = 30 ns[10]		34		mA		
C_I	Input Pin Capacitance[3, 6, 12]	@ V_{IN} = 2.5 V				
		f_{IN} = 1.0 MHz				
		T_{AMB} = +25°C			8	pF
C_O	Output Pin Capacitance[6, 7, 12, 13]	@ V_{IN} = 2.5 V				
		f_{IN} = 1.0 MHz				
		T_{AMB} = +25°C			8	pF

NOTES
[1]Bidirectional pins: D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7.
[2]Input only pins: RESET, BR, DR0, DR1, PWD.
[3]Input only pins: CLKIN, RESET, BR, DR0, DR1, PWD.
[4]Output pins: BG, PMS, DMS, BMS, IOMS, CMS, RD, WR, PWDACK, A0, DT0, DT1, CLKOUT, FL2–0, BGH.
[5]Although specified for TTL outputs, all AD73511 outputs are CMOS-compatible and will drive to V_{DD} and GND, assuming no dc loads.
[6]Guaranteed but not tested.
[7]Three-statable pins: A0–A13, D0–D23, PMS, DMS, BMS, IOMS, CMS, RD, WR, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, PF0–PF7.
[8]0 V on BR.
[9]Idle refers to AD73511 state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.
[10]V_{IN} = 0 V and 3 V. For typical figures for supply currents, refer to Power Dissipation section.
[11]I_{DD} measurement taken with all instructions executing from internal memory. 50% of the instructions are multifunction (types 1, 4, 5, 12, 13, 14), 30% are type 2 and type 6, and 20% are idle instructions.
[12]Applies to PBGA package type.
[13]Output pin capacitance is the capacitive load for any three-stated output pin.

Specifications subject to change without notice.

POWER CONSUMPTION

CONDITIONS	Typ.	Max.	SE	MCLK On	Test Conditions
AFE SECTION					
ADC On Only	7	7.2	1	YES	REFOUT Disabled
ADC and DAC On	11	12	1	YES	REFOUT Disabled
REFCAP On Only	0.65	1.00	0	NO	REFOUT Disabled
REFCAP and REFOUT On Only	2.7	3.8	0	NO	
All AFE Sections Off	0.6	0.65	0	YES	MCLK Active Levels Equal to 0V and DVDD
All AFE Sections Off	2 µA	10 µA	0	NO	Digital Inputs Static and Equal to 0 V or DVDD
DSP SECTION					
Idle Mode	6.4		-	-	
Dynamic	43		-	-	

The above values are in mA and are typical values unless otherwise noted.

TIMING CHARACTERISTICS - AFE SECTION

Parameter	Limit	Units	Description
Clock Signals			See Figure 1
t_1	61	ns min	16.384 MHz MCLK Period
t_2	24.4	ns min	MCLK Width High
t_3	24.4	ns min	MCLK Width Low
Serial Port			See Figures 3 and 4
t_4	t_1	ns min	SCLK Period (SCLK = MCLK)
t_5	$0.4 * t_1$	ns min	SCLK Width High
t_6	$0.4 * t_1$	ns min	SCLK Width Low
t_7	20	ns min	SDI/SDIFS Setup Before SCLK Low
t_8	0	ns min	SDI/SDIFS Hold After SCLK Low
t_9	10	ns max	SDOFS Delay From SCLK High
t_{10}	10	ns min	SDOFS Hold After SCLK High
t_{11}	10	ns min	SDO Hold After SCLK High
t_{12}	10	ns max	SDO Delay From SCLK High
t_{13}	30	ns max	SCLK Delay from MCLK

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD73511BB-80	-20 C to +85 C	119-Ball Plastic Ball Grid Array	B-119
AD73511BB-40	-20 C to +85 C	119-Ball Plastic Ball Grid Array	B-119

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD73511 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PBGA BALL CONFIGURATION

	1	2	3	4	5	6	7
A	IRQE/PF4	DMS	VDD (INT)	CLKIN	A11/IAD10	A7/IAD6	A4/IAD3
B	IRQL0/PF5	PMS	WR	XTAL	A12/IAD11	A8/IAD7	A5/IAD4
C	IRQL1/PF6	IOMS	RD	VDD (EXT)	A13/IAD12	A9/IAD8	GND
D	IRQ2/PF7	CMS	BMS	CLKOUT	GND	A10/IAD9	A6/IAD5
E	DT0	TFS0	RFS0	A3/IAD2	A2/IAD1	A1/IAD0	A0
F	DR0	SCLK0	DT1/F0	PWDACK	BGH	MODE A/PF0	MODE B/PF1
G	TFS1/IRQ1	RFS1/IRQ0	DR1/FI	GND	PWD	VDD (EXT)	MODE C/PF2
H	SCLK1	ERESET	RESET	PF3	FL0	FL1	FL2
J	EMS	EE	ECLK	D23	D22	D21	D20
K	ELOUT	ELIN	EINT	D19	D18	D17	D16
L	BG	D3/IACK	D5/IAL	D8	D9	D12	D15
M	EBG	D2/IAD15	D4/IS	D7/IWR	VDD (EXT)	D11	D14
N	BR	D1/IAD14	VDD (INT)	D6/IRD	GND	D10	D13
P	EBR	D0/IAD13	DVDD	DGND	ARESET	SCLK2	AMCLK
R	SDO	SDOFS	SDIFS	SDI	SE	REFCAP	REFOUT
T	VINP	NC	VINN	NC	NC	NC	NC
U	AGND	AVDD	NC	NC	VOUTP	VOUTN	NC

TOP VIEW

NOTES:
VDD (INT) › DSP CORE SUPPLY
VDD (EXT) › DSP I/O DRIVER SUPPLY
BOTH VDD (INT) AND VDD (EXT) SHOULD BE POWERED FROM THE SAME SUPPLY.

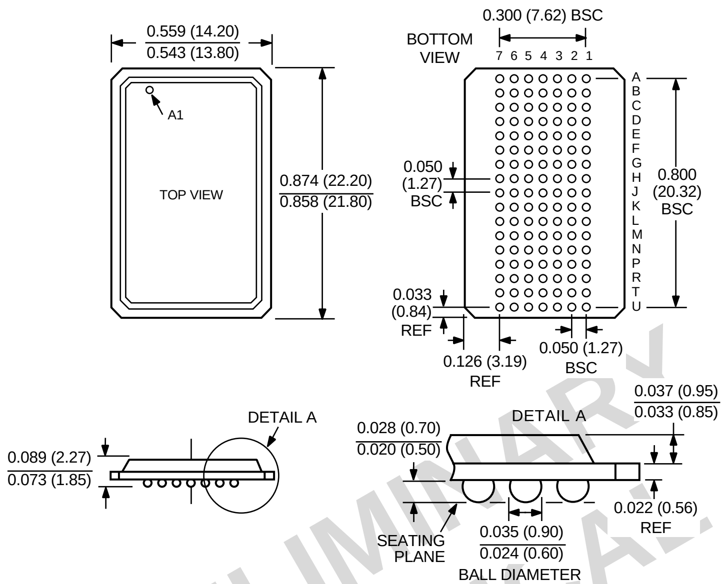
PIN FUNCTION DESCRIPTION

Mnemonic	Function
VINP	Analog Input to the positive terminal of the input Channel.
VINN	Analog Input to the negative terminal of the input Channel.
REFOUT	Buffered Reference Output, which has a nominal value of 1.2 V.
REFCAP	A Bypass Capacitor to AGND2 of 0.1 µF is required for the on-chip reference. The capacitor should be fixed to this pin.
AVDD2	Analog Power Supply Connection for Codec 2.
AGND2	Analog Ground/Substrate Connection for Codec 2.
DGND	Digital Ground/Substrate Connection.
DVDD	Digital Power Supply Connection.
$\overline{ARESET}$	Active Low Reset Signal. This input resets the entire chip, resetting the control registers and clearing the digital circuitry.
SCLK	Output Serial Clock whose rate determines the serial transfer rate to/from the codec. It is used to clock data or control information to and from the serial port (SPORT). The frequency of SCLK is equal to the frequency of the master clock (MCLK) divided by an integer number—this integer number being the product of the external master clock rate divider and the serial clock rate divider.
MCLK	Master Clock Input. MCLK is driven from an external clock signal.
SDO	Serial Data Output of the Codec. Both data and control information may be output on this pin and is clocked on the positive edge of SCLK. SDO is in three-state when no information is being transmitted and when SE is low.
SDOFS	Framing Signal Output for SDO Serial Transfers. The frame sync is one-bit wide and it is active one SCLK period before the first bit (MSB) of each output word. SDOFS is referenced to the positive edge of SCLK. SDOFS is in three-state when SE is low.
SDIFS	Framing Signal Input for SDI Serial Transfers. The frame sync is one-bit wide and it is valid one SCLK period before the first bit (MSB) of each input word. SDIFS is sampled on the negative edge of SCLK and is ignored when SE is low.
SDI	Serial Data Input of the Codec. Both data and control information may be input on this pin and are clocked on the negative edge of SCLK. SDI is ignored when SE is low.
SE	SPORT Enable. Asynchronous input enable pin for the SPORT. When SE is set low by the DSP, the output pins of the SPORT are three-stated and the input pins are ignored. SCLK is also disabled internally in order to decrease power dissipation. When SE is brought high, the control and data registers of the SPORT are at their original values (before SE was brought low), however the timing counters and other internal registers are at their reset values.
AGND1	Analog Ground/Substrate Connection for Codec 1.
AVDD1	Analog Power Supply Connection for Codec 1.
$\overline{RESET}$	(Input) Processor Reset Input
$\overline{BR}$	(Input) Bus Request Input
$\overline{BG}$	(Output) Bus Grant Output
$\overline{BGH}$	(Output) Bus Grant Hung Output
$\overline{DMS}$	(Output) Data Memory Select Output
$\overline{PMS}$	(Output) Program Memory Select Output
$\overline{IOMS}$	(Output) Memory Select Output
$\overline{BMS}$	(Output) Byte Memory Select Output
$\overline{CMS}$	(Output) Combined Memory Select Output
$\overline{RD}$	(Output) Memory Read Enable Output
$\overline{WR}$	(Output) Memory Write Enable Output
$\overline{IRQ2}$/	(Input) Edge- or Level-Sensitive Interrupt
PF7	(Input/Output) Request.[1] Programmable I/O Pin
$\overline{IRQL0}$/	(Input) Level-Sensitive Interrupt Requests[1]
PF6	(Input/Output) Programmable I/O Pin
$\overline{IRQL1}$/	(Input) Level-Sensitive Interrupt Requests[1]
PF5	(Input/Output) Programmable I/O Pin
$\overline{IRQE}$/	(Input) Edge-Sensitive Interrupt Requests[1]
PF4	(Input/Output) Programmable I/O Pin
Mode D/	(Input) Mode Select Input—Checked Only During RESET
PF3	(Input/Output) Programmable I/O Pin During Normal Operation
Mode C/	(Input) Mode Select Input—Checked Only During RESET
PF2	(Input/Output) Programmable I/O Pin During Normal Operation
Mode B/	(Input) Mode Select Input—Checked Only During RESET
PF1	(Input/Output) Programmable I/O Pin During Normal Operation

Mode A/ *PF0*	(Input) Mode Select Input—Checked Only During RESET (Input/Output) Programmable I/O Pin During Normal Operation
CLKIN, XTAL	(Inputs) Clock or Quartz Crystal Input
CLKOUT	(Output) Processor Clock Output
SPORT0	(Inputs/Outputs) Serial Port I/O Pins
SPORT1	(Inputs/Outputs) Serial Port I/O Pins
$\overline{\text{IRQ1}}$:$\overline{\text{0}}$	(Inputs) Edge- or Level-Sensitive Interrupts,
FI	(Input) Flag In[2]
FO	(Output) Flag Out[2]
$\overline{\text{PWD}}$	(Input) Power-Down Control Input
PWDACK	(Output) Power-Down Control Output
FL0, FL1, FL2	(Outputs) Output Flags
VDD and GND	Power and Ground
EZ-Port	(Inputs/Outputs) For Emulation Use

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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