

### FEATURES

- V/F Conversion to 1 MHz
- Reliable Monolithic Construction
- Very Low Nonlinearity
  - 0.002% typ at 10 kHz
  - 0.005% typ at 100 kHz
  - 0.07% typ at 1 MHz
- Input Offset Trimmable to Zero
- CMOS or TTL Compatible
- Unipolar, Bipolar, or Differential V/F
- V/F or F/V Conversion
- Available in Surface Mount
- MIL-STD-883 Compliant Versions Available

### PRODUCT DESCRIPTION

The AD650 V/F/V (voltage-to-frequency or frequency-to-voltage converter) provides a combination of high frequency operation and low nonlinearity previously unavailable in monolithic form. The inherent monotonicity of the V/F transfer function makes the AD650 useful as a high-resolution analog-to-digital converter. A flexible input configuration allows a wide variety of input voltage and current formats to be used, and an open-collector output with separate digital ground allows simple interfacing to either standard logic families or opto-couplers.

The linearity error of the AD650 is typically 20 ppm (0.002% of full scale) and 50 ppm (0.005%) maximum at 10 kHz full scale. This corresponds to approximately 14-bit linearity in an analog-to-digital converter circuit. Higher full-scale frequencies or longer count intervals can be used for higher resolution conversions. The AD650 has a useful dynamic range of six decades allowing extremely high resolution measurements. Even at 1 MHz full scale, linearity is guaranteed less than 1000 ppm (0.1%) on the AD650KN, BD, and SD grades.

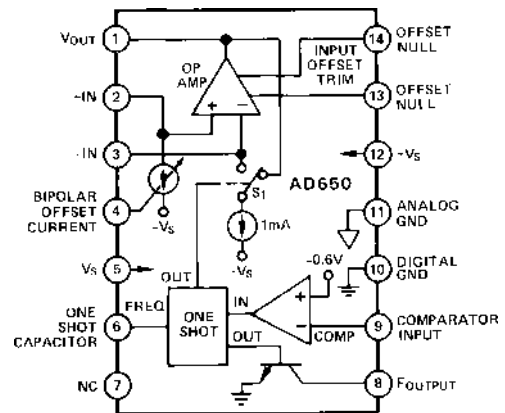
In addition to analog-to-digital conversion, the AD650 can be used in isolated analog signal transmission applications, phased locked-loop circuits, and precision stepper motor speed controllers. In the F/V mode, the AD650 can be used in precision tachometer and FM demodulator circuits.

The input signal range and full-scale output frequency are user-programmable with two external capacitors and one resistor. Input offset voltage can be trimmed to zero with an external potentiometer.

### REV. B

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### PIN CONFIGURATION



The AD650JN and AD650KN are offered in a plastic 14-lead DIP package. The AD650JP is available in a 20-lead plastic leaded chip carrier (PLCC). Both plastic packaged versions of the AD650 are specified for the commercial (0°C to +70°C) temperature range. For industrial temperature range (-25°C to +85°C) applications, the AD650AD and AD650BD are offered in a ceramic package. The AD650SD is specified for the full -55°C to +125°C extended temperature range.

### PRODUCT HIGHLIGHTS

1. In addition to very high linearity, the AD650 can operate at full-scale output frequency up to 1 MHz. The combination of these two features makes the AD650 an inexpensive solution for applications requiring high resolution monotonic A/D conversion.
2. The AD650 has a very versatile architecture that can be configured to accommodate bipolar, unipolar, or differential input voltages, or unipolar input currents.
3. TTL or CMOS compatibility is achieved using an open collector frequency output. The pull-up resistor can be connected to voltages up to +30 V, or +15 V or +5 V for conventional CMOS or TTL logic levels.
4. The same components used for V/F conversion can also be used for F/V conversion by adding a simple logic biasing network and reconfiguring the AD650.
5. The AD650 provides separate analog and digital grounds. This feature allows prevention of ground loops in real-world applications.
6. The AD650 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD650/883B data sheet for detailed specifications.

# AD650—SPECIFICATIONS (@ +25°C, with $V_S = \pm 15$ V, unless otherwise noted)

Model	AD650J/AD650A			AD650K/AD650B			AD650S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
<b>DYNAMIC PERFORMANCE</b>										
Full-Scale Frequency Range			1			1			1	MHz
Nonlinearity <sup>1</sup> $f_{MAX} = 10$ kHz		0.002	0.005	0.002	0.005		0.002	0.005		%
$f_{MAX} = 100$ kHz		0.005	<b>0.02</b>	0.005	<b>0.02</b>		0.005	<b>0.02</b>		%
$f_{MAX} = 500$ kHz		0.02	0.05	0.02	0.05		0.02	0.05		%
$f_{MAX} = 1$ MHz		0.1		0.05	<b>0.1</b>		0.05	<b>0.1</b>		%
Full-Scale Calibration Error <sup>2</sup> , 100 kHz		$\pm 5$		$\pm 5$			$\pm 5$			%
1 MHz		$\pm 10$		$\pm 10$			$\pm 10$			%
vs. Supply <sup>3</sup>	-0.015		<b>+0.015</b>	-0.015		<b>+0.015</b>	-0.015		<b>+0.015</b>	% of FSR/V
vs. Temperature										
A, B, and S Grades										
at 10 kHz			$\pm 75$			$\pm 75$			$\pm 75$	ppm/°C
at 100 kHz			$\pm 150$			$\pm 150$			<b><math>\pm 150</math></b>	ppm/°C
J and K Grades										
at 10 kHz		$\pm 75$		$\pm 75$						ppm/°C
at 100 kHz		$\pm 150$		$\pm 150$						ppm/°C
<b>BIPOLAR OFFSET CURRENT</b>										
Activated by 1.24 k $\Omega$ Between Pins 4 and 5	0.45	0.5	0.55	0.45	0.5	0.55	0.45	0.5	0.55	mA
<b>DYNAMIC RESPONSE</b>										
Maximum Settling Time for Full Scale Step Input	1 Pulse of New Frequency Plus 1 $\mu$ s			1 Pulse of New Frequency Plus 1 $\mu$ s			1 Pulse of New Frequency Plus 1 $\mu$ s			
Overload Recovery Time Step Input	1 Pulse of New Frequency Plus 1 $\mu$ s			1 Pulse of New Frequency Plus 1 $\mu$ s			1 Pulse of New Frequency Plus 1 $\mu$ s			
<b>ANALOG INPUT AMPLIFIER (V/F Conversion)</b>										
Current Input Range (Figure 1)	0		+0.6	0		+0.6	0		+0.6	mA
Voltage Input Range (Figure 5)	-10		0	-10		0	-10		0	V
Differential Impedance	2 M $\Omega$   10 pF			2 M $\Omega$   10 pF			2 M $\Omega$   10 pF			
Common-Mode Impedance	1000 M $\Omega$   10 pF			1000 M $\Omega$   10 pF			1000 M $\Omega$   10 pF			
Input Bias Current										
Noninverting Input		40	<b>100</b>		40	<b>100</b>		40	<b>100</b>	nA
Inverting Input		$\pm 8$	<b><math>\pm 20</math></b>		$\pm 8$	<b><math>\pm 20</math></b>		$\pm 8$	<b><math>\pm 20</math></b>	nA
Input Offset Voltage (Trimable to Zero)			<b><math>\pm 4</math></b>			<b><math>\pm 4</math></b>			<b><math>\pm 4</math></b>	mV
vs. Temperature ( $T_{MIN}$ to $T_{MAX}$ )		$\pm 30$		$\pm 30$			$\pm 30$		$\pm 30$	$\mu$ V/°C
Safe Input Voltage		$\pm V_S$		$\pm V_S$			$\pm V_S$		$\pm 30$	C
<b>COMPARATOR (F/V Conversion)</b>										
Logic "0" Level	$-V_S$		-1	$-V_S$		-1	$-V_S$		+1	V
Logic "1" Level	0		$+V_S$	0		$+V_S$	0		$+V_S$	V
Pulse Width Range <sup>4</sup>	0.1		( $0.3 \times t_{OS}$ )	0.1		( $0.3 \times t_{OS}$ )	0.1		( $0.3 \times t_{OS}$ )	$\mu$ s
Input Impedance		250			250			250		k $\Omega$
<b>OPEN COLLECTOR OUTPUT (V/F Conversion)</b>										
Output Voltage in Logic "0"										
$I_{SINK} \leq 8$ mA, $T_{MIN}$ to $T_{MAX}$			0.4			0.4			0.4	V
Output Leakage Current in Logic "1"			<b>100</b>			<b>100</b>			<b>100</b>	nA
Voltage Range <sup>5</sup>	0		+36	0		+36	0		+36	V
<b>AMPLIFIER OUTPUT (F/V Conversion)</b>										
Voltage Range (1500 $\Omega$ min Load Resistance)	0		+10	0		+10	0		+10	V
Source Current (750 $\Omega$ max Load Resistance)	10			10			10			mA
Capacitive Load (Without Oscillation)			100			100			100	pF
<b>POWER SUPPLY</b>										
Voltage, Rated Performance	$\pm 9$		<b><math>\pm 18</math></b>	$\pm 9$		<b><math>\pm 18</math></b>	$\pm 9$		<b><math>\pm 18</math></b>	V
Quiescent Current			<b>8</b>			<b>8</b>			<b>8</b>	mA
<b>TEMPERATURE RANGE</b>										
Rated Performance – N Package	0		+70	0		+70				°C
D Package	-25		+85	-25		+85	-55		+125	°C

## NOTES

<sup>1</sup>Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a fraction of full scale.

<sup>2</sup>Full-scale calibration error adjustable to zero.

<sup>3</sup>Measured at full-scale output frequency of 100 kHz.

<sup>4</sup>Refer to F/V conversion section of the text.

<sup>5</sup>Referred to digital ground.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those test are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

### ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage	36 V
Storage Temperature	-55°C to +150°C
Differential Input Voltage	±10 V
Maximum Input Voltage	±V <sub>S</sub>
Open Collector Output Voltage Above Digital GND	36 V
Current	50 mA
Amplifier Short Circuit to Ground	Indefinite
Comparator Input Voltage	±V <sub>S</sub>

### PIN CONFIGURATION

PIN NO.	D-14	N-14	P-20A
1	V <sub>OUT</sub>	V <sub>OUT</sub>	NC
2	+IN	+IN	V <sub>OUT</sub>
3	-IN	-IN	+IN
4	BIPOLAR OFFSET CURRENT	BIPOLAR OFFSET CURRENT	-IN
5	-V <sub>S</sub>	-V <sub>S</sub>	NC
6	ONE SHOT CAPACITOR	ONE SHOT CAPACITOR	BIPOLAR OFFSET CURRENT
7	NC	NC	NC
8	F <sub>OUTPUT</sub>	F <sub>OUTPUT</sub>	-V <sub>S</sub>
9	COMPARATOR INPUT	COMPARATOR INPUT	ONE SHOT CAPACITOR
10	DIGITAL GND	DIGITAL GND	NC
11	ANALOG GND	ANALOG GND	NC
12	+V <sub>S</sub>	+V <sub>S</sub>	F <sub>OUTPUT</sub>
13	OFFSET NULL	OFFSET NULL	COMPARATOR INPUT
14	OFFSET NULL	OFFSET NULL	DIGITAL GND
15			NC
16			ANALOG GND
17			NC
18			+V <sub>S</sub>
19			OFFSET NULL
20			OFFSET NULL

### ORDERING GUIDE

Model	Gain Tempco ppm/°C 100 kHz	1 MHz Linearity	Specified Temperature Range °C	Package Description	Package Option
AD650JN	150 typ	0.1% typ	0 to +70	Plastic DIP	N-14
AD650KN	150 typ	0.1% max	0 to +70	Plastic DIP	N-14
AD650JP	150 typ	0.1% typ	0 to +70	Plastic Leaded Chip Carrier (PLCC)	P-20A
AD650AD	150 max	0.1% typ	-25 to +85	Ceramic DIP	D-14
AD650BD	150 max	0.1% max	-25 to +85	Ceramic DIP	D-14
AD650SD	150 max	0.1% max	-55 to +125	Ceramic DIP	D-14

# AD650

## CIRCUIT OPERATION UNIPOLAR CONFIGURATION

The AD650 is a *charge balance* voltage-to-frequency converter. In the connection diagram shown in Figure 1, or the block diagram of Figure 2a, the input signal is converted into an equivalent current by the input resistance  $R_{IN}$ . This current is *exactly* balanced by an internal feedback current delivered in short, timed bursts of current may be thought of as precisely defined packets of charge. The required number of charge packets, each producing one pulse of the output transistor, depends upon the amplitude of the input signal. Since the number of charge packets delivered per unit time is dependent on the input signal amplitude, a linear voltage-to-frequency transformation will be accomplished. The frequency output is furnished via an open collector transistor.

A more rigorous analysis demonstrates how the charge balance voltage-to-frequency conversion takes place.

A block diagram of the device arranged as a V-to-F converter is shown in Figure 2a. The unit is comprised of an input integrator, a current source and steering switch, a comparator and a one-shot. When the output of the one-shot is low, the current steering switch  $S_1$  diverts all the current to the output of the op amp; this is called the Integration Period. When the one-shot has been triggered and its output is high, the switch  $S_1$  diverts all the current to the summing junction of the op amp; this is called the Reset Period. The two different states are shown in Figure 2 along with the various branch currents. It should be noted that the output current from the op amp is the same for either state, thus minimizing transients.

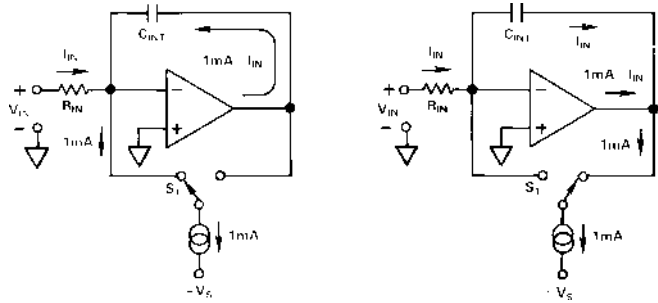


Figure 2b. Reset Mode

Figure 2c. Integrate Mode

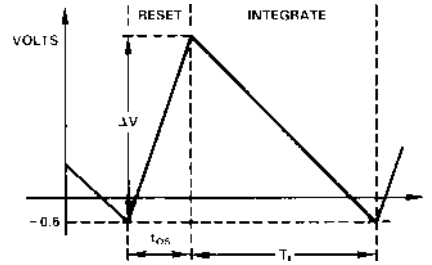


Figure 2d. Voltage Across  $C_{INT}$

The positive input voltage develops a current ( $I_{IN} = V_{IN}/R_{IN}$ ) which charges the integrator capacitor  $C_{INT}$ . As charge builds up on  $C_{INT}$ , the output voltage of the integrator ramps downward towards ground. When the integrator output voltage (Pin 1) crosses the comparator threshold ( $-0.6$  volt) the comparator triggers the one shot, whose time period,  $t_{OS}$  is determined by the one shot capacitor  $C_{OS}$ .

Specifically, the one shot time period is:

$$t_{OS} = C_{OS} \times 6.8 \times 10^3 \text{ sec/F} + 3.0 \times 10^{-7} \text{ sec} \quad (1)$$

The Reset Period is initiated as soon as the integrator output voltage crosses the comparator threshold, and the integrator ramps upward by an amount:

$$\Delta V = t_{OS} \cdot \frac{dV}{dt} = \frac{t_{OS}}{C_{INT}} (1 \text{ mA} - I_{IN}) \quad (2)$$

After the Reset Period has ended, the device starts another Integration Period, as shown in Figure 2, and starts ramping downward again. The amount of time required to reach the comparator threshold is given as:

$$T_I = \frac{\Delta V}{\frac{dV}{dt}} = \frac{t_{OS}/C_{INT}(1 \text{ mA} - I_{IN})}{I_{IN}/C_{INT}} = t_{OS} \left( \frac{1 \text{ mA}}{I_{IN}} - 1 \right) \quad (3)$$

The output frequency is now given as:

$$f_{OUT} = \frac{1}{t_{OS} + T_I} = \frac{I_{IN}}{t_{OS} \times 1 \text{ mA}} = 0.15 \frac{\text{F} \cdot \text{Hz}}{\text{A}} \frac{V_{IN}/R_{IN}}{C_{OS} + 4.4 \times 10^{-11} \text{ F}} \quad (4)$$

Note that  $C_{INT}$ , the integration capacitor has no effect on the transfer relation, but merely determines the amplitude of the sawtooth signal out of the integrator.

### One Shot Timing

A key part of the preceding analysis is the one shot time period that was given in equation (1). This time period can be broken down into approximately 300 ns of propagation delay, and a second time segment dependent linearly on timing capacitor  $C_{OS}$ . When the one shot is triggered, a voltage switch that holds Pin 6

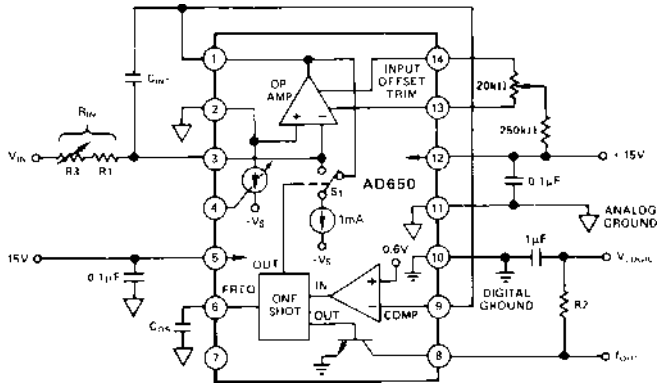


Figure 1. Connection Diagram for V/F Conversion, Positive Input Voltage

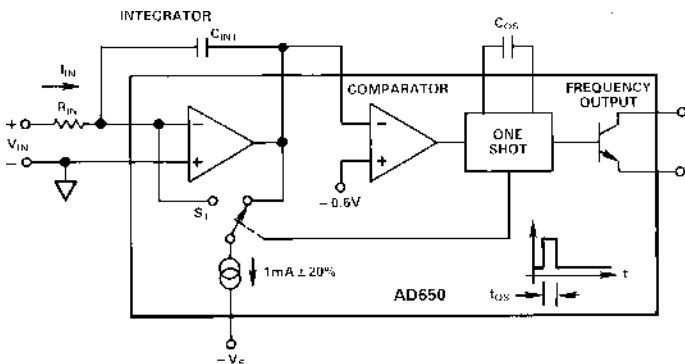


Figure 2a. Block Diagram

at analog ground is opened allowing that voltage to change. An internal 0.5 mA current source connected to Pin 6 then draws its current out of  $C_{OS}$ , causing the voltage at Pin 6 to decrease linearly. At approximately  $-3.4$  V, the one shot resets itself, thereby ending the timed period and starting the V/F conversion cycle over again. The total one shot time period can be written mathematically as:

$$t_{OS} = \frac{\Delta V C_{OS}}{I_{DISCHARGE}} + T_{GATE DELAY} \quad (5)$$

substituting actual values quoted above,

$$t_{OS} = \frac{-3.4 V \times C_{OS}}{-0.5 \times 10^{-3} A} + 300 \times 10^{-9} \text{ sec} \quad (6)$$

This simplifies into the timed period equation given above.

### COMPONENT SELECTION

Only four component values must be selected by the user. These are input resistance  $R_{IN}$ , timing capacitor  $C_{OS}$ , logic resistor R2, and integration capacitor  $C_{INT}$ . The first two determine the input voltage and full-scale frequency, while the last two are determined by other circuit considerations.

Of the four components to be selected, R2 is the easiest to define. As a pull-up resistor, it should be chosen to limit the current through the output transistor to 8 mA if a TTL maximum  $V_{OL}$  of 0.4 V is desired. For example, if a 5 V logic supply is used, R2 should be no smaller than  $5 V/8 \text{ mA}$  or 625  $\Omega$ . A larger value can be used if desired.

$R_{IN}$  and  $C_{OS}$  are the only two parameters available to set the full-scale frequency to accommodate the given signal range. The “swing” variable that is affected by the choice of  $R_{IN}$  and  $C_{OS}$  is nonlinearity. The selection guide of Figure 3 shows this quite graphically. In general, larger values of  $C_{OS}$  and lower full-scale input currents (higher values of  $R_{IN}$ ) provide better linearity. In Figure 3, the implications of four different choices of  $R_{IN}$  are shown. Although the selection guide is set up for a unipolar configuration with a zero to 10 V input signal range, the results can be extended to other configurations and input signal ranges. For a full scale frequency of 100 kHz (corresponding to 10 V input), you can see that among the available choices,  $R_{IN} = 20 \text{ k}$  and  $C_{OS} = 620 \text{ pF}$  gives the lowest nonlinearity, 0.0038%. Also, if you wish to use the highest frequency that will give the 20 ppm minimum nonlinearity, it is approximately 33 kHz (40.2 k $\Omega$  and 1000 pF).

For input signal spans other than 10 V, the input resistance must be scaled proportionately. For example, if 100 k $\Omega$  is called out for a 0 V–10 V span, 10k would be used with a 0 V–1 V span, or 200 k $\Omega$  with a  $\pm 10$  V bipolar connection.

The last component to be selected is the integration capacitor  $C_{INT}$ . In almost all cases, the best value for  $C_{INT}$  can be calculated using the equation:

$$C_{INT} = \frac{10^{-4} F/sec}{f_{MAX}} \quad (1000 \text{ pF minimum}) \quad (7)$$

When the proper value for  $C_{INT}$  is used, the charge balance architecture of the AD650 provides continuous integration of the input signal, hence large amounts of noise and interference

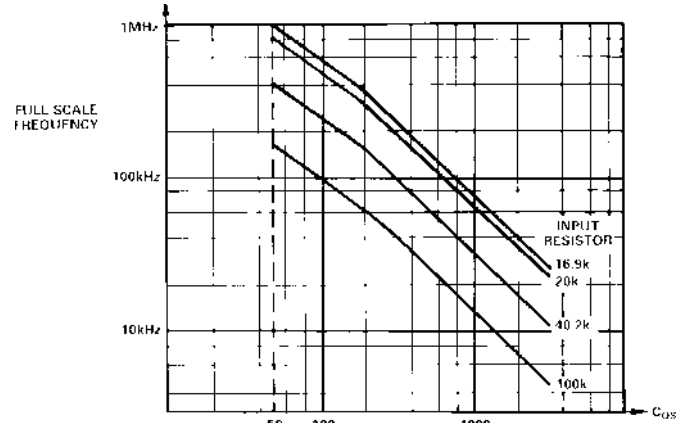


Figure 3a. Full-Scale Frequency vs.  $C_{OS}$

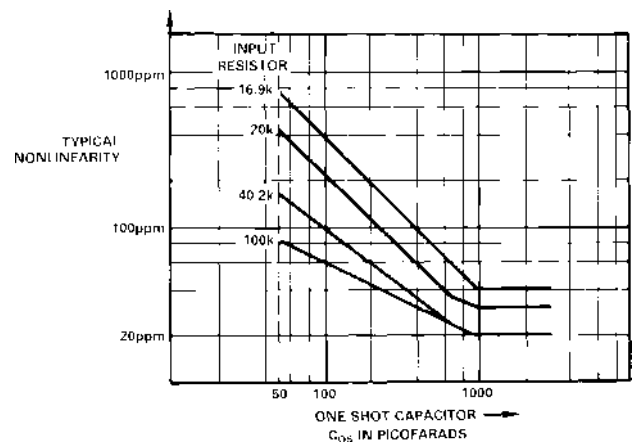


Figure 3b. Typical Nonlinearity vs.  $C_{OS}$

can be rejected. If the output frequency is measured by counting pulses during a constant gate period, the integration provides infinite normal-mode rejection for frequencies corresponding to the gate period and its harmonics. However, if the integrator stage becomes saturated by an excessively large noise pulse, the continuous integration of the signal will be interrupted, allowing the noise to appear at the output. If the approximate amount of noise that will appear on  $C_{INT}$  is known ( $V_{NOISE}$ ), the value of  $C_{INT}$  can be checked using the following inequality:

$$C_{INT} > \frac{t_{OS} \times 1 \times 10^{-3} A}{+V_S - 3V - V_{NOISE}} \quad (8)$$

For example, consider an application calling for a maximum frequency of 75 kHz, a 0 volt–1 volt signal range, and supply voltages of only  $\pm 9$  volts. The component selection guide of Figure 3 is used to select 2.0 k $\Omega$  for  $R_{IN}$  and 1000 pF for  $C_{OS}$ . This results in a one shot time period of approximately 7  $\mu\text{s}$ . Substituting 75 kHz into equation 7 yields a value of 1300 pF for  $C_{INT}$ . When the input signal is near zero, 1 mA flows through the integration capacitor to the switched current sink during the reset phase, causing the voltage across  $C_{INT}$  to increase by approximately 5.5 volts. Since the integrator output stage requires approximately 3 volts head room for proper operation, only 0.5 volt margin remains for integrating extraneous noise on the signal line. A negative noise pulse at this time might saturate the integrator, causing an error in signal integration. Increasing  $C_{INT}$  to 1500 pF or 2000 pF will provide much more noise margin, thereby eliminating this potential trouble spot.



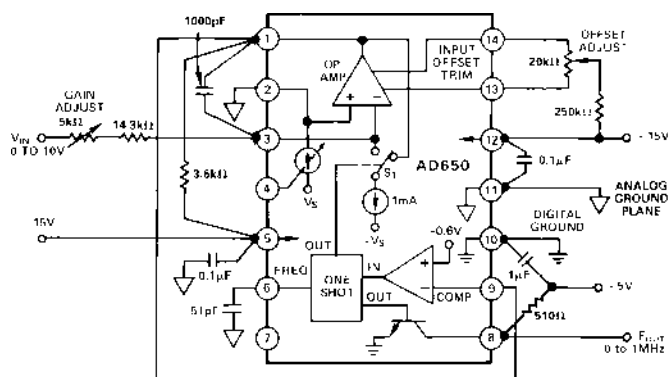


Figure 7. 1 MHz V/F Connection Diagram

### DECOUPLING AND GROUNDING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10  $\Omega$  to 100  $\Omega$ ) in the supply lines to provide a measure of decoupling between the various circuits in a system. Ceramic capacitors of 0.1  $\mu\text{F}$  to 1.0  $\mu\text{F}$  should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD650.

In addition, a larger board level decoupling capacitor of 1  $\mu\text{F}$  to 10  $\mu\text{F}$  should be located relatively close to the AD650 on each power supply line. Such precautions are imperative in high resolution data acquisition applications where one expects to exploit the full linearity and dynamic range of the VFC. Although some types of circuits may operate satisfactorily with power supply decoupling at only one location on each circuit board, such practice is strongly discouraged in high accuracy analog design.

Separate digital and analog grounds are provided on the AD650. The emitter of the open collector frequency output transistor is the only node returned to the digital ground. All other signals are referred to analog ground. The purpose of the two separate grounds is to allow isolation between the high precision analog signals and the digital section of the circuitry. As much as several hundred millivolts of noise can be tolerated on the digital ground without affecting the accuracy of the VFC. Such ground noise is inevitable when switching the large currents associated with the frequency output signal.

At 1 MHz full scale, it is necessary to use a pull-up resistor of about 500  $\Omega$  in order to get the rise time fast enough to provide well defined output pulses. This means that from a 5 volt logic supply, for example, the open collector output will draw 10 mA.

This much current being switched will surely cause ringing on long ground runs due to the self inductance of the wires. For instance, #20 gauge wire has an inductance of about 20 nH per inch; a current of 10 mA being switched in 50 ns at the end of 12 inches of 20 gauge wire will produce a voltage spike of 50 mV. The separate digital ground of the AD650 will easily handle these types of switching transients.

A problem will remain from interference caused by radiation of electro-magnetic energy from these fast transients. Typically, a voltage spike is produced by inductive switching transients; these spikes can capacitively couple into other sections of the circuit. Another problem is ringing of ground lines and power supply lines due to the distributed capacitance and inductance of the wires. Such ringing can also couple interference into sensitive analog circuits. The best solution to these problems is proper bypassing of the logic supply at the AD650 package. A

1  $\mu\text{F}$  to 10  $\mu\text{F}$  tantalum capacitor should be connected directly to the supply side of the pull-up resistor and to the digital ground—Pin 10. The pull-up resistor should be connected directly to the frequency output—Pin 8. The lead lengths on the bypass capacitor and the pull up resistor should be as short as possible. The capacitor will supply (or absorb) the current transients, and large ac signals will flow in a physically small loop through the capacitor, pull up resistor, and frequency output transistor. It is important that the loop be physically small for two reasons: first, there is less self-inductance if the wires are short, and second, the loop will not radiate RFI efficiently.

The digital ground (Pin 10) should be separately connected to the power supply ground. Note that the leads to the digital power supply are only carrying dc current and cannot radiate RFI. There may also be a dc ground drop due to the difference in currents returned on the analog and digital grounds. This will not cause any problem. In fact, the AD650 will tolerate as much as 0.25 volt dc potential difference between the analog and digital grounds. These features greatly ease power distribution and ground management in large systems. Proper technique for grounding requires separate digital and analog ground returns to the power supply. Also, the signal ground must be referred directly to analog ground (Pin 11) at the package. All of the signal grounds should be tied directly to Pin 11, especially the one-shot capacitor. More information on proper grounding and reduction of interference can be found in Reference 1.

### TEMPERATURE COEFFICIENTS

The drift specifications of the AD650 do not include temperature effects of any of the supporting resistors or capacitors. The drift of the input resistors R1 and R3 and the timing capacitor C<sub>OS</sub> directly affect the overall temperature stability. In the application of Figure 2, a 10 ppm/ $^{\circ}\text{C}$  input resistor used with a 100 ppm/ $^{\circ}\text{C}$  capacitor may result in a maximum overall circuit gain drift of:

$$150 \text{ ppm}/^{\circ}\text{C} (\text{AD650A}) + 100 \text{ ppm}/^{\circ}\text{C} (\text{C}_{\text{OS}}) + 10 \text{ ppm}/^{\circ}\text{C} (\text{R}_{\text{IN}}) 260 \text{ ppm}/^{\circ}\text{C}$$

In bipolar configuration, the drift of the 1.24 k $\Omega$  resistor used to activate the internal bipolar offset current source will directly affect the value of this current. This resistor should be matched to the resistor connected to the op amp noninverting input (Pin 2), see Figure 4. That is, the temperature coefficients of these two resistors should be equal. If this is the case, then the effects of the temperature coefficients of the resistors cancel each other, and the drift of the offset voltage developed at the op amp non-inverting input will be determined solely by the AD650. Under these conditions the TC of the bipolar offset voltage is typically  $-200 \text{ ppm}/^{\circ}\text{C}$  and is a maximum of  $-300 \text{ ppm}/^{\circ}\text{C}$ . The offset voltage always decreases in magnitude as temperature is increased.

Other circuit components do not directly influence the accuracy of the VFC over temperature changes as long as their actual values are not so different from the nominal value as to preclude operation. This includes the integration capacitor, C<sub>INT</sub>. A change in the capacitance value of C<sub>INT</sub> simply results in a different rate of voltage change across the capacitor. During the Integration Phase (refer to Figure 2), the rate of voltage change across C<sub>INT</sub> has the opposite effect that it does during the Reset Phase. The result is that the conversion accuracy is unchanged

<sup>1</sup>"Noise Reduction Techniques in Electronic Systems," by H. W. OTT, (John Wiley, 1976).

# AD650

by either drift or tolerance of  $C_{INT}$ . The net effect of a change in the integrator capacitor is simply to change the peak to peak amplitude of the sawtooth waveform at the output of the integrator.

The gain temperature coefficient of the AD650 is not a constant value. Rather the gain TC is a function of both the full-scale frequency and the ambient temperature. At a low full-scale frequency, the gain TC is determined primarily by the stability of the internal reference—a buried Zener reference. This low speed gain TC can be quite good; at 10 kHz full scale, the gain TC near 25°C is typically  $0 \pm 50 \text{ ppm}/^\circ\text{C}$ . Although the gain TC changes with ambient temperature (tending to be more positive at higher temperatures), the drift remains within a  $\pm 75 \text{ ppm}/^\circ\text{C}$  window over the entire military temperature range. At full-scale frequencies higher than 10 kHz dynamic errors become much more important than the static drift of the dc reference. At a full-scale frequency of 100 kHz and above, these timing errors dominate the gain TC. For example, at 100 kHz full-scale frequency ( $R_{IN} = 40 \text{ k}$  and  $C_{OS} = 330 \text{ pF}$ ) the gain TC near room temperature is typically  $-80 \pm 50 \text{ ppm}/^\circ\text{C}$ , but at an ambient temperature near  $+125^\circ\text{C}$ , the gain TC tends to be more positive and is typically  $+15 \pm 50 \text{ ppm}/^\circ\text{C}$ . This information is presented in a graphical form in Figure 8. The gain TC always tends to become more positive at higher temperatures. Therefore, it is possible to adjust the gain TC of the AD650 by using a one-shot capacitor with an appropriate TC to cancel the drift of the circuit. For example, consider the 100 kHz full-scale frequency. An average drift of  $-100 \text{ ppm}/^\circ\text{C}$  means that as temperature is increased, the circuit will produce a lower frequency in response to a given input voltage. This means that the one-shot capacitor must decrease in value as temperature increases in order to compensate the gain TC of the AD650; that is, the capacitor must have a TC of  $-100 \text{ ppm}/^\circ\text{C}$ . Now consider the 1 MHz full-scale frequency.

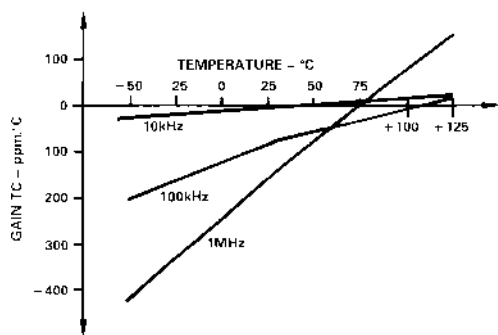


Figure 8. Gain TC vs. Temperature

It is not possible to achieve very much improvement in performance unless the expected ambient temperature range is known. For example, in a constant low temperature application such as gathering data in an Arctic climate (approximately  $-20^\circ\text{C}$ ), a  $C_{OS}$  with a drift of  $-310 \text{ ppm}/^\circ\text{C}$  is called for in order to compensate the gain drift of the AD650. However, if that circuit should see an ambient temperature of  $+75^\circ\text{C}$ , the  $C_{OS}$  cap would change the gain TC from approximately  $0 \text{ ppm}$  to  $+310 \text{ ppm}/^\circ\text{C}$ .

The temperature effects of the components described above are the same when the AD650 is configured for negative or bipolar input voltages, and for F/V conversion as well.

## NONLINEARITY SPECIFICATION

The linearity error of the AD650 is specified by the endpoint method. That is, the error is expressed in terms of the deviation from the ideal voltage to frequency transfer relation after calibrating the converter at full scale and “zero”. The nonlinearity will vary with the choice of one-shot capacitor and input resistor (see Figure 3). Verification of the linearity specification requires the availability of a switchable voltage source (or a DAC) having a linearity error below 20 ppm, and the use of very long measurement intervals to minimize count uncertainties. Every AD650 is automatically tested for linearity, and it will not usually be necessary to perform this verification, which is both tedious and time consuming. If it is required to perform a nonlinearity test either as part of an incoming quality screening or as a final product evaluation, an automated “bench-top” tester would prove useful. Such a system based on the Analog Devices’ LTS-2010 is described in Reference 2.

The voltage-to-frequency transfer relation is shown in Figure 9 with the nonlinearity exaggerated for clarity. The first step in determining nonlinearity is to connect the endpoints of the

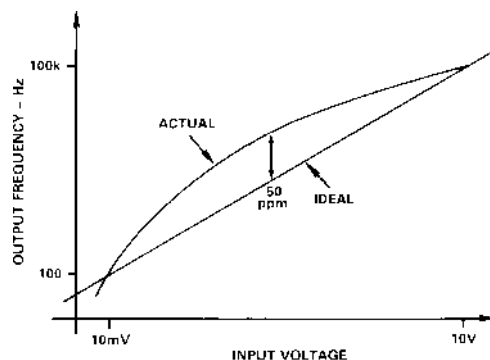


Figure 9a. Exaggerated Nonlinearity at 100 kHz Full Scale

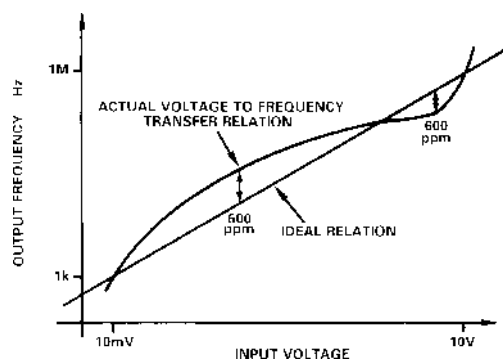


Figure 9b. Exaggerated Nonlinearity at 1 MHz Full Scale

operating range (typically at 10 mV and 10 V) with a straight line. This straight line is then the ideal relationship which is desired from the circuit. The second step is to find the difference between this line and the actual response of the circuit at a few points between the endpoints—typically ten intermediate points will suffice. The difference between the actual and the ideal response is a frequency error measured in hertz. Finally, these frequency errors are normalized to the full-scale frequency and expressed either as parts per million of full scale (ppm) or parts per hundred of full scale (%). For example, on a 100 kHz full

<sup>2</sup>“V-F Converters Demand Accurate Linearity Testing,” by L. DeVito, (Electronic Design, March 4, 1982).



scale, if the maximum frequency error is 5 Hz, the nonlinearity would be specified as 50 ppm or 0.005%. Typically on the 100 kHz scale, the nonlinearity is positive and the maximum value occurs at about midscale (Figure 9a). At higher full-scale frequencies, (500 kHz to 1 MHz), the nonlinearity becomes “S” shaped and the maximum value may be either positive or negative. Typically, on the 1 MHz scale ( $R_{IN} = 16.9k$ ,  $C_{OS} = 51$  pF) the nonlinearity is positive below about 2/3 scale and is negative above this point. This is shown graphically in Figure 9b.

### PSRR

The power supply rejection ratio is a specification of the change in gain of the AD650 as the power supply voltage is changed. The PSRR is expressed in units of parts-per-million change of the gain per percent change of the power supply—ppm/%. For example, consider a VFC with a 10 volt input applied and an output frequency of exactly 100 kHz when the power supply potential is  $\pm 15$  volts. Changing the power supply to  $\pm 12.5$  volts is a 5 volt change out of 30 volts, or 16.7%. If the output frequency changes to 99.9 kHz, the gain has changed 0.1% or 1000 ppm. The PSRR is 1000 ppm divided by 16.7% which equals 60 ppm/%.

The PSRR of the AD650 is a function of the full-scale operating frequency. At low full-scale frequencies the PSRR is determined by the stability of the reference circuits in the device and can be very good. At higher frequencies there are dynamic errors which become more important than the static reference signals, and consequently the PSRR is not quite as good. The values of PSRR are typically  $0 \pm 20$  ppm/% at 10 kHz full-scale frequency ( $R_{IN} = 40$  k,  $C_{OS} = 3300$  pF). At 100 kHz ( $R_{IN} = 40k$ ,  $C_{OS} = 330$  pF) the PSRR is typically  $+80 \pm 40$  ppm/%, and at 1 MHz ( $R_{IN} = 16.9$  k $\Omega$ ,  $C_{OS} = 51$  pF) the PSRR is  $+350 \pm 50$  ppm/%. This information is summarized graphically in Figure 10.

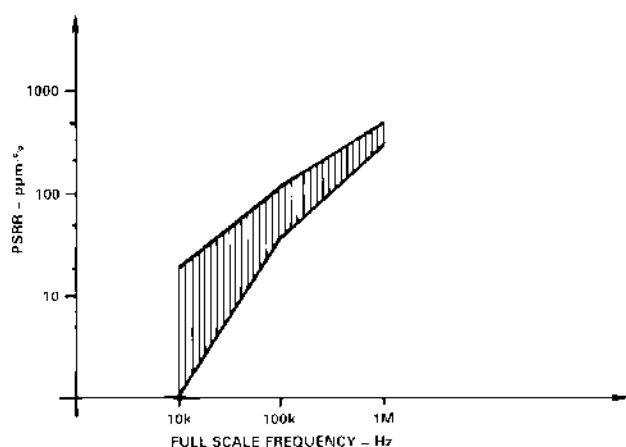


Figure 10. PSRR vs. Full-Scale Frequency

### OTHER CIRCUIT CONSIDERATIONS

The input amplifier connected to Pins 1, 2 and 3 is not a standard operational amplifier. Rather, the design has been optimized for simplicity and high speed. The single largest difference between this amplifier and a normal op amp is the lack of an integrator (or level shift) stage. Consequently the voltage on the output (Pin 1) must always be more positive than 2 volts below the inputs (Pins 2 and 3). For example, in the F-to-V conversion mode, see Figure 6, the noninverting input of the op amp (Pin 2) is grounded, which means that the output (Pin 1) will not be able to go below  $-2$  volts. Normal operation of the circuit as shown

in the figure will never call for a negative voltage at the output but one may imagine an arrangement calling for a bipolar output voltage (say  $\pm 10$  volts) by connecting an extra resistor from Pin 3 to a positive voltage. This will not work.

Care should be taken under conditions where a high positive input voltage exists at or before power up. These situations can cause a latch up at the integrator output (Pin 1). This is a non-destructive latch and, as such, normal operation can be restored by cycling the power supply. Latch up can be prevented by connecting two diodes (e.g., 1N914 or 1N4148) as shown in Figure 4, thereby, preventing Pin 1 from swinging below Pin 2.

A second major difference is that the output will only sink 1 mA to the negative supply. There is no pulldown stage at the output other than the 1 mA current source used for the V-to-F conversion. The op amp will source a great deal of current from the positive supply, and it is internally protected by current limiting. The output of the op amp may be driven to within 3 volts of the positive supply when it is not sourcing external current. When sourcing 10 mA the output voltage may be driven to within 6 volts of the positive supply.

A third difference between this op amp and a normal device is that the inverting input, Pin 3, is bias current compensated and the noninverting input is not bias current compensated. The bias current at the inverting input is nominally zero, but may be as much as 20 nA in either direction. The noninverting input typically has a bias current of 40 nA that always flows into the node (an npn input transistor). Therefore, it is not possible to match input voltage drops due to bias currents by matching input resistors.

The op amp has provisions for trimming the input offset voltage. A potentiometer of 20 k $\Omega$  is connected to Pins 13 and 14 and the wiper is connected to the positive supply through a 250 k $\Omega$  resistor. A potential of about 0.6 volt is established across the 250 k $\Omega$  resistor, and the 3  $\mu$ A current is injected into the null pins. It is also possible to null the op amp offset voltage by using only one of the null pins and use a bipolar current either into or out of the null pin. The amount of current required will be very small—typically less than 3  $\mu$ A. This technique is shown in the applications section of this data sheet: the autozero circuit uses this technique.

The bipolar offset current is activated by connecting a 1.24 k $\Omega$  resistor between Pin 4 and the negative supply. The resultant current delivered to the op amp noninverting input is nominally 0.5 mA and has a tolerance of  $\pm 10\%$ . This current is then used to provide an offset voltage when Pin 2 is tied to ground through a resistor. The 0.5 mA which appears at Pin 2 is also flowing through the 1.24 k $\Omega$  resistor and this current may be by observing the voltage across the 1.24 k $\Omega$  resistor. An external resistor is used to activate the bipolar offset current source to provide the lowest tolerance and temperature drift of the resultant offset voltage. It is possible to use other values of resistance between Pin 4 and  $-V_S$  to obtain a bipolar offset current different than 0.5 mA. Figure 11 is a graph of the relationship between the bipolar offset current and the value of the resistor used to activate the source.



output cannot change very rapidly due to the integrator time constant formed by  $C_{INT}$  and  $R_{IN}$ . While it is possible to decrease the integrator time constant to provide faster settling of the F-to-V output voltage, the carrier feedthrough will then be larger. For signal frequency response in excess of 2 kHz, a phase locked F/V conversion technique such as the one shown in Figure 14 is recommended.

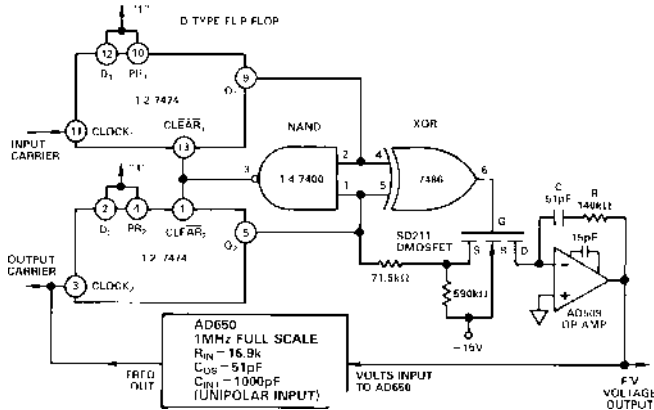


Figure 14. Phase Locked Loop F/V Conversion

In a phase locked loop circuit, the oscillator is driven to a frequency and phase equal to an input reference signal. In applications such as a synthesizer, the oscillator output frequency is first processed through a programmable “divide by N” before being applied to the phase detector as feedback. Here the oscillator frequency is forced to be equal to “N times” the reference frequency and it is this frequency output which is the desired output signal and not a voltage. In this case, the AD650 offers compact size and wide dynamic range.

In signal recovery applications of a PLL, the desired output signal is the voltage applied to the oscillator. In these situations a linear relationship between the input frequency and the output voltage is desired; the AD650 makes a superb oscillator for FM demodulation. The wide dynamic range and outstanding linearity of the AD650 VFC allow simple embodiment of high performance analog signal isolation or telemetry systems. The circuit shown in Figure 14 uses a digital phase detector which also provides proper feedback in the event of unequal frequencies. Such phase-frequency detectors (PFDs) are available in integrated form. For a full discussion of phase lock loop circuits see Reference 3.

An analysis of this circuit must begin at the 7474 dual D flip flop. When the input carrier matches the output carrier in both phase and frequency, the Q outputs of the flip flops will rise at exactly the same time. With two zeros, then two ones on the inputs of the exclusive or (XOR) gate, the output will remain low keeping the DMOS FET switched off. Also, the NAND gate will go low resetting the flip-flops to zero. Throughout the entire cycle just described, the DMOS integrator gate remained off, allowing the voltage at the integrator output to remain unchanged from the previous cycle. However, if the input carrier leads the output carrier by a few degrees, the XOR gate will be turned on for the small time span that the two signals are mismatched. Since  $Q_2$  will be low during the mismatch time, a negative current will be fed into the integrator, causing its output voltage to rise. This in turn will increase the frequency of

the AD650 slightly, driving the system towards synchronization. In a similar manner, if the input carrier lags the output carrier, the integrator will be forced down slightly to synchronize the two signals.

Using a mathematical approach, the  $\pm 25 \mu A$  pulses from the phase detector are incorporated into the phase detector gain,  $K_d$ .

Using a mathematical approach, the  $\pm 25 \mu A$  pulses from the phase detector are incorporated into the phase detector gain,  $K_d$ .

$$K_d = \frac{25 \mu A}{2\pi} = 4 \times 10^{-6} \text{ amperes/radian} \quad (9)$$

Also, the V/F converter is configured to produce 1 MHz in response to a 10 volt input, so its gain  $K_o$ , is:

$$K_o = \frac{2\pi \times 1 \times 10^6 \text{ Hz}}{10 \text{ V}} = 6.3 \times 10^5 \frac{\text{radians}}{\text{volt} \cdot \text{sec}} \quad (10)$$

The dynamics of the phase relationship between the input and output signals can be characterized as a second order system with natural frequency  $\omega_n$ :

$$\omega_n = \sqrt{\frac{K_o K_d}{C}} \quad (11)$$

and damping factor

$$\zeta = \frac{R\sqrt{C K_o K_d}}{2} \quad (12)$$

For the values shown in Figure 14, these relations simplify to a natural frequency of 35 kHz with a damping factor of 0.8.

For those desiring a simple approach to determining component values for other PLL frequencies and VFC full-scale voltage, the following cookbook steps can be used:

1. Determine  $K_o$  (in units of radians per volt second) from the maximum input carrier frequency  $F_{MAX}$  (in hertz) and the maximum output voltage  $V_{MAX}$ .

$$K_o = \frac{2\pi \times F_{MAX}}{V_{MAX}} \quad (13)$$

2. Calculate a value for C based upon the desired loop bandwidth,  $f_n$ . Note that this is the desired frequency range of the output signal. The loop bandwidth ( $f_n$ ) is *not* the maximum carrier frequency ( $f_{MAX}$ ): the signal may be very narrow even though it is transmitted over a 1 MHz carrier.

$$C = \frac{K_o}{f_n^2} \cdot 1 \times 10^{-7} \frac{\text{V} \cdot \text{F}}{\text{Rad} \cdot \text{sec}} \quad \begin{array}{l} \text{C units FARADS} \\ f_n \text{ units HERTZ} \\ K_o \text{ units RAD/VOLT} \cdot \text{SEC} \end{array} \quad (14)$$

3. Calculate R to yield a damping factor of approximately 0.8 using this equation:

$$R = \frac{f_n}{K_o} \cdot 2.5 \times 10^6 \frac{\text{Rad} \cdot \Omega}{\text{V}} \quad \begin{array}{l} \text{R units OHMS} \\ f_n \text{ units HERTZ} \\ K_o \text{ units RAD/VOLT} \cdot \text{SEC} \end{array} \quad (15)$$

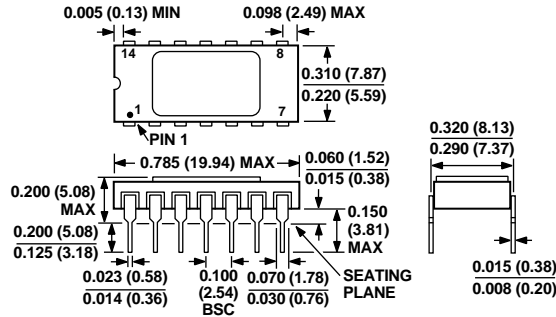
If in actual operation the PLL overshoots or hunts excessively before reaching a final value, the damping factor may be raised by increasing the value of R. Conversely, if the PLL is overdamped, a smaller value of R should be used.

<sup>3</sup>“Phase lock Techniques,” 2nd Edition, by F.M. Gardner, (John Wiley and Sons, 1979)

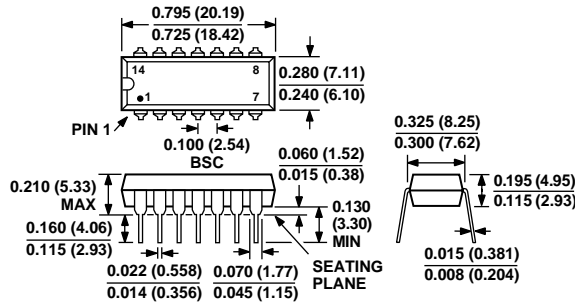
**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

**14-Lead Ceramic DIP  
(D-14)**



**14-Lead Plastic DIP  
(N-14)**



**20-Lead PLCC  
(P-20A)**

