Discrete Multitone (DMT) Coprocessor for ADSL Chipsets

AD6439

FEATURES

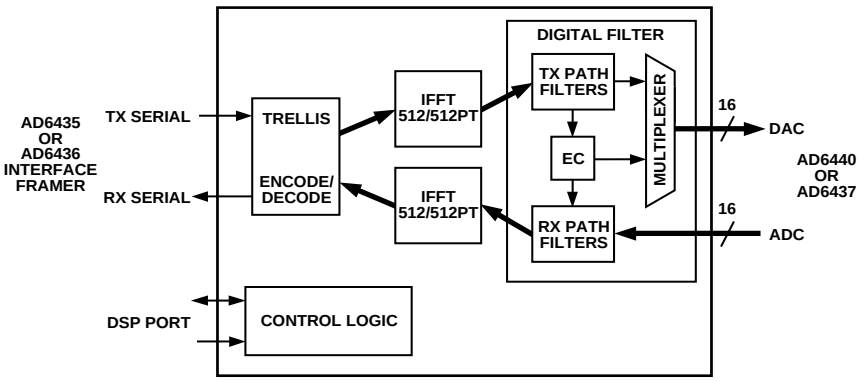
Component in Analog Devices' AD20msp918 ADSL Chipset
Designed to ANSI T1.413 Issue 2/ETSI TR238/ITU G.992.1 and G.992.2
Higher Performance
Improved Data Rates or Longer Reach
Suitable for CO or Residence (ATU-R and ATU-C)
Performs All DMT Functions and Operations
Trellis Coding
Echo Cancellation
Symmetric Transforms (512 Point)
Flexible Allocation of Tones Upstream/Downstream
Supports Symmetric Services (SDSL)
Increased Upstream (e.g., 1 Mbps)
Supports ADSL Over ISDN (Shifted U/S)
Strict Filters for Spectral Compatibility
128-Lead MQFP
–40°C to +85°C, 3.3 V Operation, 1.1 W

GENERAL DESCRIPTION

The AD6439 Discrete Multitone (DMT) Coprocessor is part of Analog Devices ADSL solution, a series of flexible, standards-based chipsets for creating high performance ADSL and SDSL modems that implement a superset of standard Category 2 functionality.

A high performance alternative to the AD6436 DMT Coprocessor, the AD6439 meets the functionality requirements of ANSI T1.413 Category 2 (trellis coding, echo cancellation), but is considerably more versatile. It implements both transmit and receive paths (trellis coding/decoding, IFFT/FFT, filtering and echo cancellation). Symmetric transforms allow flexible allocation of upstream and downstream bandwidth, including symmetric data rates. Improved digital filters exceed the requirements of T1.413 and deliver strict spectral masks (e.g., for VDSL compatibility).

FUNCTIONAL BLOCK DIAGRAM



REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD6439–SPECIFICATIONS

Parameter	Value	Comments
Transmit DAC Port—Data Width	16 Bit	
Transmit DAC Port—Rates	17.664 MHz, 8.832 MHz, 2.208 MHz	At Either CO or RT
Receive ADC Port—Data Width	16 Bit	
Receive ADC Port—Rates	8.832 MHz or 2.208 MHz	At Either CO or RT
Downstream FFT/IFFT	512 Points	256 Tones
Upstream FFT/IFFT	512 Points	256 Tones
Bits/Carrier (Max)	15	
Interface to AD6435/AD6438	Serial 35.328 MHz	Both Transmit and Receive
Power Supply		
V_{DD}	+3.0 V to +3.6 V	
P_{DISS}	< 1.25 W Max at 3.6 V	
Temperature Range	–40°C to +85°C	

Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS

Parameter	Typ Value	Comments
V_{OH}	V_{DD} – 0.4 V dc	At I_{OH} = –0.5 mA
V_{OL}	0.4 V dc	
V_{IH}	2.0 V dc	
V_{IL}	1.0 V dc	
I_{IH}	±500 nA	V_{IN} = V_{DD} = 3.6 V
I_{IL}	±500 nA	V_{IN} = 0 V, V_{DD} = 3.6 V

Specifications subject to change without notice.

TIMING SPECIFICATIONS

TX TIMING

Parameter	Description	Typ	Units
t_{TX-SR}	Setup Time of TX_AEC[15:0] from Rising Edge of TX_CLK	12	ns
t_{TX-HR}	Hold Time of TX_AEC[15:0] from Rising Edge of TX_CLK	6	ns
t_{TX-SF}	Setup Time of TX_AEC[15:0] from Falling Edge of TX_CLK	12	ns
t_{TX-HF}	Hold Time of TX_AEC[15:0] from Falling Edge of TX_CLK	6	ns

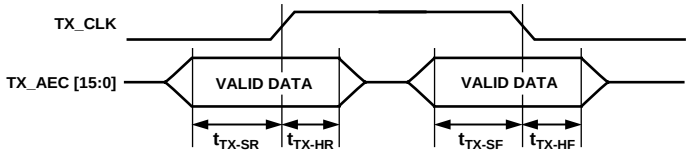


Figure 1. TX Timing

RX TIMING

Parameter	Description	Typ	Units
t_{RX-S}	Setup Time of RX[15:0] from Rising Edge of RX_CLK	25	ns
t_{RX-H}	Hold Time of RX[15:0] from Rising Edge of RX_CLK	0	ns

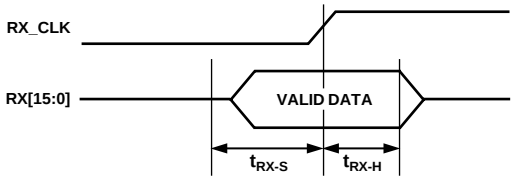


Figure 2. RX Timing

TX SERIAL I/F TIMING

Parameter	Description	Typ	Units
$t_{TFRM-DV}$	TX_FRM Valid to Falling Edge of TX_RX_SCLK	5	ns
t_{TFRM-D}	Hold Time of TX_FRM from Falling Edge of TX_RX_SCLK	10	ns
$t_{TDREQ-DV}$	TX_DREQ Valid to Rising Edge of TX_RX_SCLK	5	ns
$t_{TDREQ-H}$	Hold Time of TX_DREQ from Rising Edge of TX_RX_SCLK	10	ns
t_{TBS-S}	Setup Time of TX_BS from Rising Edge of TX_RX_SCLK	10	ns
t_{TBS-H}	Hold Time of TX_BS from Rising Edge of TX_RX_SCLK	0	ns
t_{TD-S}	Setup Time of TX_SDATA from Rising Edge of TX_RX_SCLK	10	ns
t_{TD-H}	Hold Time of TX_SDATA from Rising Edge of TX_RX_SCLK	0	ns

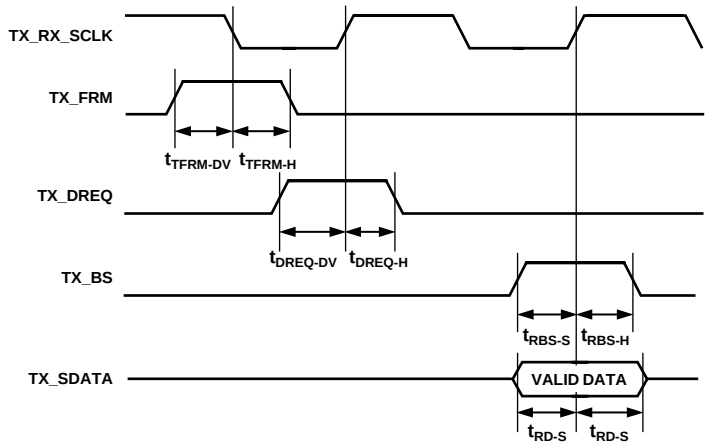


Figure 3. TX Serial IF Timing

RX SERIAL I/F TIMING

Parameter	Description	Typ	Units
$t_{RFRM-DV}$	RX_FRM Valid to Falling Edge of TX_RX_SCLK	5	ns
t_{RFRM-H}	Hold Time of RX_FRM from Falling Edge of TX_RX_SCLK	10	ns
$t_{RDREQ-S}$	Setup Time of RX_DREQ from Rising Edge of TX_RX_SCLK	10	ns
$t_{RDREQ-H}$	Hold Time of RX_DREQ from Rising Edge of TX_RX_SCLK	0	ns
t_{RBS-DV}	RX_BS Valid to Rising Edge of TX_RX_SCLK	5	ns
t_{RBS-H}	Hold Time of RX_BS from Rising Edge of TX_RX_SCLK	10	ns
t_{RD-DV}	RX_SDATA Valid to Rising Edge of TX_RX_SCLK	5	ns
t_{RD-H}	Hold Time of RX_SDATA from Rising Edge of TX_RX_SCLK	10	ns

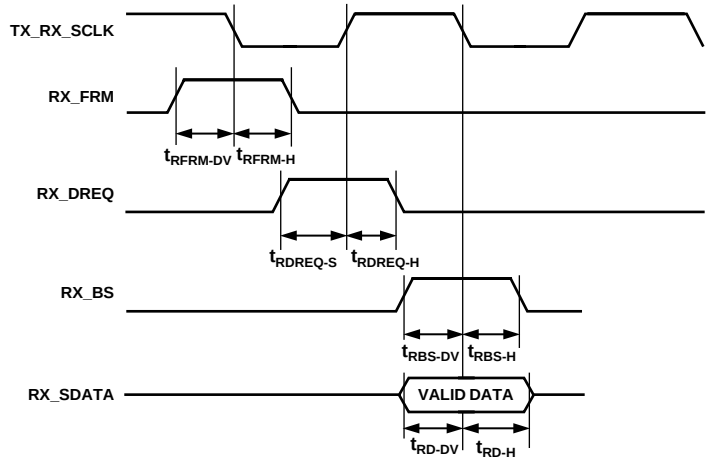


Figure 4. RX Serial IF Timing

READ OPERATION

Parameter	Description	Min	Max	Units
Timing Requirements:				
t_{RDD}	NRD Low to Data Valid		17 + W	ns
t_{AA}	A0–A13, NCS to Data Valid		19 + W	ns
t_{RDH}	Data Hold from NRD High	0		ns
Switching Characteristics:				
t_{RP}	NRD Pulsewidth	20 + W		ns
t_{CRD}	DSP_CLK High to NRD Low	3	16	ns
t_{ASR}	A0–A13, NCS Setup Before NRD Low	2		ns
t_{RDA}	A0–A13, NCS Hold After NRD Deasserted	5		ns
t_{RWR}	NRD High to NRD or NWR Low	12		ns

NOTES
W = wait state x (DSP_CLK period).
AD6439 accesses faster than 20 MHz (DSP_CLK) requires one wait state.

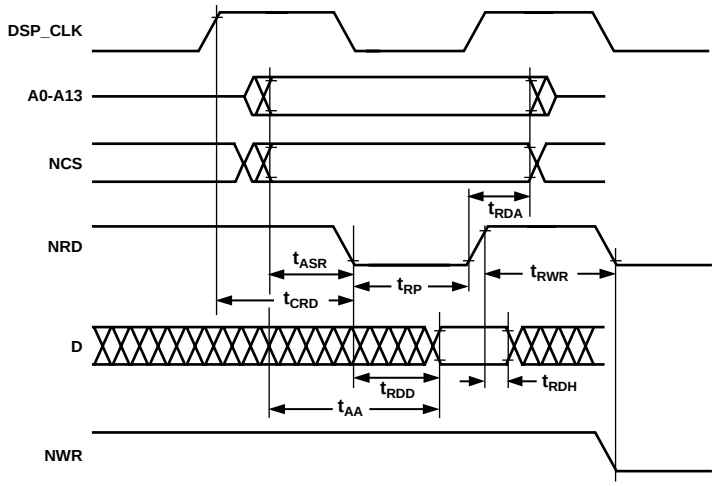


Figure 5. Read Operation

WRITE OPERATION

Parameter	Description	Min	Max	Units
Switching Characteristics:				
t_{DW}	Data Setup Before NWR High	10 + W		ns
t_{DH}	Data Hold After NWR High	6		ns
t_{WP}	NWR Pulsewidth	12 + W		ns
t_{ASW}	A0–A13, NCS Setup Before NWR Low	2		ns
t_{DDR}	Data Disable Before NWR or NRD Low	1		ns
t_{CWR}	DSP_CLK High to NWR Low	3	16	ns
t_{AW}	A0–A13, NCS Setup Before NWR Deasserted	12 + W		ns
t_{WRA}	A0–A13, NCS Hold After NWR Deasserted	5		ns
t_{WWR}	NWR High to NRD or NWR Low	12		ns

NOTES
W = wait state x (DSP_CLK period).
AD6439 accesses faster than 20 MHz (DSP_CLK) requires one wait state.

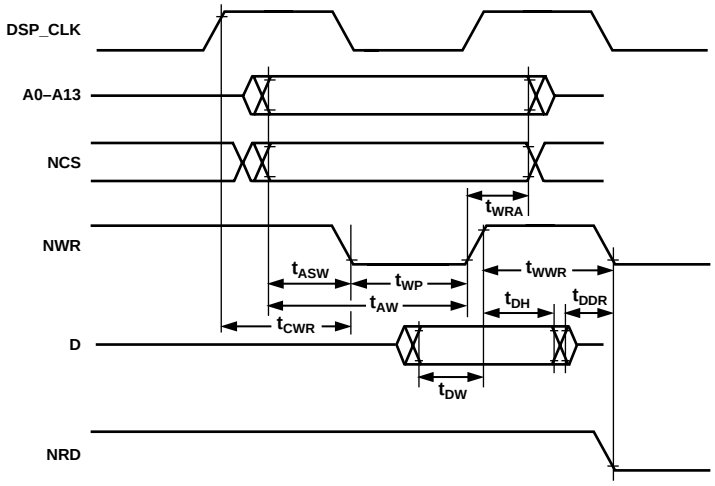


Figure 6. Write Operation

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +4.6 V
Input Voltage . . . . . –0.5 V to V_{DD} + 0.5 V
Output Voltage Swing . . . . . –0.5 V to V_{DD} + 0.5 V
Operating Temperature Range (Ambient) . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) MQFP . . . . . +280°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6439BS	–40°C to +85°C	128-Lead Plastic MQFP	S-128B

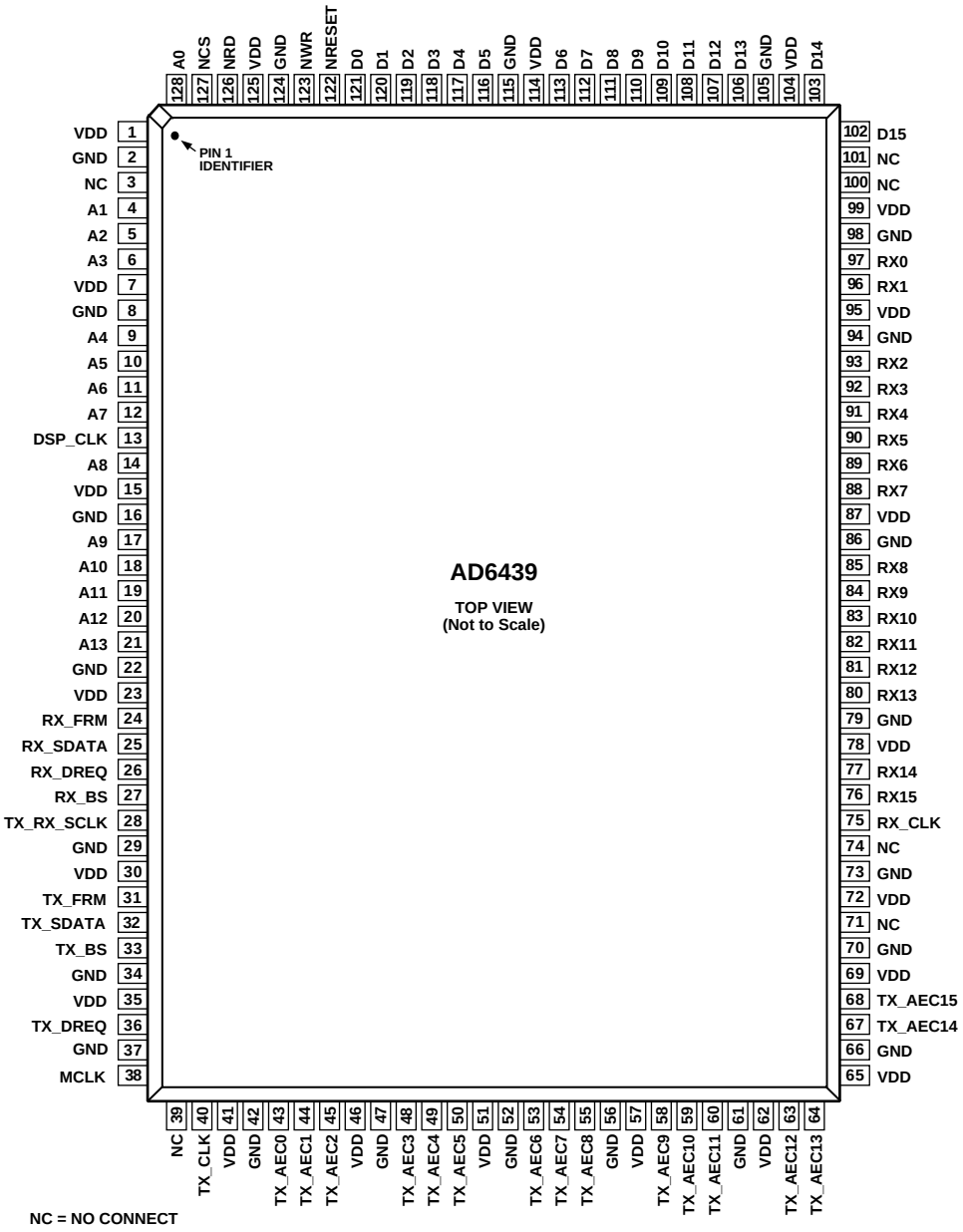
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6439 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin Number	Pin Name	Type	Description
1, 7, 15, 23, 30, 35, 41, 46, 51, 57, 62, 65, 69, 72, 78, 87, 95, 99, 104, 114, 125	VDD	Supply	These pins supply 3.3 V power to the AD6439.
2, 8, 16, 22, 29, 34, 37, 42, 47, 52, 56, 61, 66, 70, 73, 79, 86, 94, 98, 105, 115, 124	GND	Ground	These pins supply ground for the AD6439.
3, 39, 71, 74, 100, 101	NC	No Connection	
13	DSP_CLK	Input	Clock for the DSP interface.
24	RX_FRM	Output	Frame pulse for RX serial port.
25	RX_SDATA	Output	Serial data for RX serial port.
26	RX_DREQ	Input	Data request for RX serial port.
27	RX_BS	Output	Byte strobe for RX serial port.
28	TX_RX_SCLK	Output	Serial clock for TX and RX serial port.
31	TX_FRM	Output	Frame pulse for TX serial port.
32	TX_SDATA	Input	Serial data for TX serial port.
33	TX_BS	Input	Byte strobe for TX serial port.
36	TX_DREQ	Output	Data request for TX serial port.
38	MCLK	Input	Master clock (35.328 MHz).
40	TX_CLK	Output	Output clock used to qualify valid transmit data.
43–45, 48–50, 53–55, 58–60, 63, 64, 67, 68	TX_AEC[0:15]	Outputs	16-bit output for transmit and AEC data stream.
75	RX_CLK	Output	Output clock used to qualify valid receive data.
97, 96, 93–88, 85–80, 77, 76	RX(0:15)	Inputs	16-bit input for receive data stream.
121–116, 113–106, 103, 102	D(0:15)	I/O	16-bit data bus from DSP port.
122	NRESET	Input	Reset pin, active low.
123	NWR	Input	Write strobe from DSP port, active low.
126	NRD	Input	Rad strobe from DSP port, active low.
127	NCS	Input	Chip set from DSP port, active low.
128, 4–6, 9–12, 14, 17–21	A(0:13)	Inputs	14-bit address bus for DSP port.

PIN CONFIGURATION



NC = NO CONNECT

INTRODUCTION

This data sheet describes the functionality and interfacing of the AD6439 Discrete Multitone (DMT) Coprocessor IC. The AD6439 is part of the Analog Devices AD20msp918 ADSL chipset. Other components include:

- AD6438 ATM Interface and Framer IC
- AD6437 Analog Front-End IC
- AD8016 Driver/Receiver
- ADSP-2183 System Control Processor

Figure 7 illustrates the basic interconnection between system components.

An object code license for all modem software is supplied with the AD20msp918 chipset.

When used as part of the AD20msp918 ADSL chipset, internal functionality of the AD6439 is under control of the firmware supplied with the ADSP-2183 and its MP (Messaging Protocol). This protocol supplies a hardware-neutral method of controlling operation of the ADSL chipset that is compatible with various hardware implementations.

The AD6439 is a high performance version of the earlier AD6436 DMT Coprocessor IC and can be used in place of the AD6436 in applications such as the AD20msp910 ADSL chipset. Enhancements to the AD6439 include:

- Trellis Encoder and Decoder Functions Added
- POTS HPF Block Added
- Mask FIR Added
- Digital Echo Canceller Lengthened
- Analog Echo Canceller Block added (Requires AD6440 Chip)
- Standby operation Mode Added
- Symmetric FFT and IFFT Operations Performed

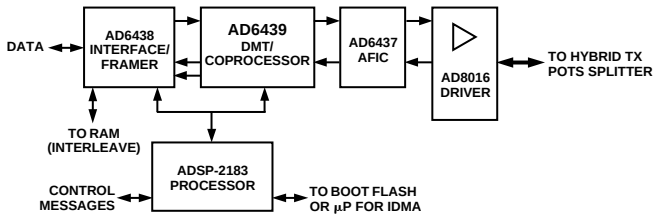


Figure 7. Block Diagram AD20msp918 Chipset

FUNCTIONAL DESCRIPTION

The AD6439 performs encoding and decoding operations, frequency domain equalization (FDQ), FFT/IFFT operations, and a number of digital filter functions, including interpolation/decimation and Time-Domain Equalization (TDQ). It is designed to Category 1 of the ANSI/ETSI standard and relies on Frequency Division Multiplexing (FDM) to separate upstream and downstream signals of up to 256 tones.

The AD6439 consists of six major blocks: a serial interface block, a Trellis/QAM encoder/decoder block, an IFFT block, a digital filter (DFIC) block, and a DSP interface and control block (see Figure 8).

The transmit path starts with serial data received from the AD6435/AD6438. This data is encoded (QAM or Trellis), modulated (IFFT), processed by the digital filter section, and output to the AD6440 or AD6437. It is also used by the echo canceller block to produce an Analog Echo Cancel (AEC) data stream. The AEC data stream is multiplexed on the same output pins as the transmit data stream to minimize the number of pins required by both the AD6439 and the integrated AFE (AD6440). The AD6439 can also be connected directly to the AD6437, however, this does not permit utilization of the analog echo cancel function.

The receive path begins with data being received by the AD6439 from the AD6440 or AD6437 AFE. The receive data stream is processed by the receive path filters, demodulated by the FFT, decoded, and sent to the AD6435/AD6438. The echo canceller provides a digital echo cancel stream used by the receive path filter section.

Encoder/Decoder

The Encode/Decode block handles the QAM or Trellis encoding and decoding of data.

Data received from the AD6435/AD6438 as a 35.328 MHz serial stream is fed to the encoder buffer. This block handles encoding, bin allocation and tone reordering operations. Each subcarrier (from 0 to 255) can handle from 0 to 15 bits, with the density controlled by the bin allocation. This block also handles the pilot tone insertion (Bin 64 in CO mode and Bin 16 in the RT).

The decoder is very similar, recovering the data from the subcarriers and reversing tone ordering and bit allocation operations. It also operates the same way in CO and RT mode. The receive serial interface between the decoder and the AD6435/AD6438 operates at 35.328 MHz.

QAM encoding corresponds to the "Tone Ordering" and "Constellation Encoder and Gain Scaling" blocks in the T1.413 reference model.

IFFT Block

The IFFT block performs a 512-point inverse FFT in CO mode (transmitting the downstream data) and in RT mode (transmitting the upstream data). It also implements gain-scaling at the same time.

While data is being read out of the IFFT block and into the digital filter section, the cyclic prefix is added to the transmit path. The purpose of the cyclic prefix is to make the symbol appear periodic in nature to the receiver. The IFFT produces 512 real data samples, to which 32 samples are added.

FFT Block

On the receive channel, the FFT block performs a 512-point FFT in CO mode (receiving the upstream duplex data) and in RT mode (receiving the downstream simplex data). In addition, carriers can be scaled up to provide full precision for the FDQ and QAM or Trellis decode operations. After the transform, the FFT performs the FDQ decode operation in the output buffer. In addition to performing the FFT, this block also strips off cyclic prefixes and removes pilot tones from the symbol.

Digital Filter Block

This implements a variety of digital filtering operations, including Time Domain Equalization (TDQ) and the interpolation/decimation tasks that connect the digital devices to the analog stage (AD6437/AD6440).

The echo cancellation filter improves system performance by easing the task of the FDM separation filter, reducing the effect of sidelobes in FFT, and reducing the size of the guardband. It also improves line matching.

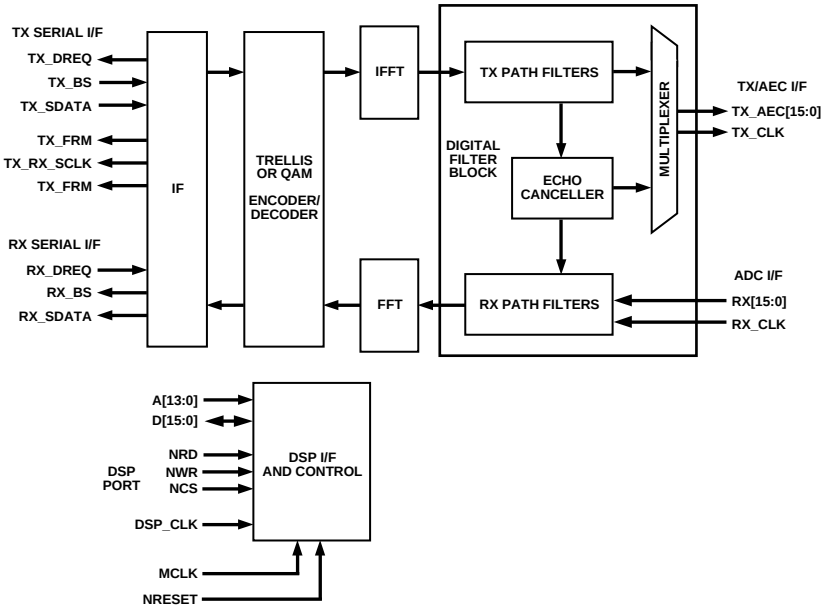


Figure 8. Block Diagram

The AD6439 includes logic for a parallel transmit path to generate an echo-cancellation signal, which operates with a second DAC in the AD6440 codec in the analog domain to implement Category 2 overlapping spectra.

NB Data Width

The AD6436 uses 16-bit datapaths internally. As such, it can take full advantage of high resolution analog stages with up to 16-bit resolution. Note: The AD6437/AD6440 (companion part in the AD20msp918 chipset) is only specified to 12-bit linearity.

INTERFACE TIMING

The AD6439 contains a transmit serial port which accepts a bit stream from an AD6435/AD6438, a receive serial port that sends a bit stream to an AD6435/AD6438, ADC and DAC interfaces, and a DSP host port to allow a DSP to monitor signals and control the data through the device. The analog echo canceller interface is identical to the DAC interface.

TX Serial Interface

The TX serial interface between the AD6439 and the AD6435/AD6438 uses five signals:

TX_RX_SCLK:	Serial clock provided by AD6439
TX_DREQ:	Data request provided by AD6439
TX_FRAME:	Frame strobe provided by AD6439
TX_BS:	Byte strobe provided by AD6435/AD6438
TX_SDATA:	Serial data provided by AD6435/AD6438

Figure 9 shows the timing of the TX interface signals.

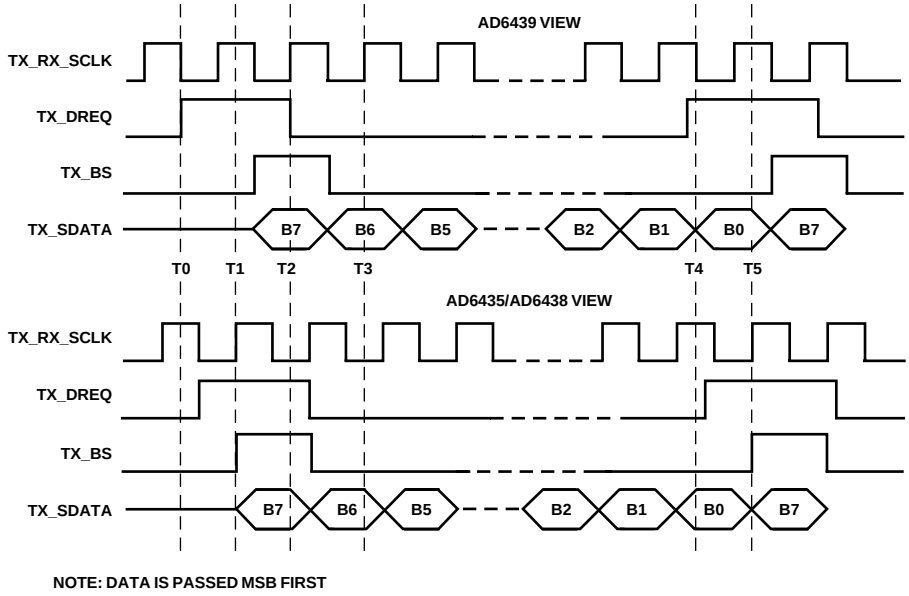


Figure 9. TX Serial Port Timing

This is a byte protocol. The AD6439 raises TX_DREQ on the falling edge of TX_RX_SCLK to request data (ref T0). The AD6435/AD6438 samples the TX_DREQ on its rising clock and when seen, outputs a one clock byte strobe TX_BS (ref T1) and simultaneously places Bit 7 of the byte on the TX_SDATA pin. Then, on the next seven rising clocks the AD6435/AD6438 places Bits 6 through 0 on the TX_SDATA pin.

On the next rising clock, the TX_DREQ line is again sampled (ref T5) and, if it is high and another byte is ready to transmit, outputs the byte strobe coincident with the MSB of the next byte then proceeds to output the rest of the byte in successive clock cycles. If TX_DREQ were low, or another byte was not available yet, the byte strobe would not be output, and TX_DREQ would continue to be sampled on successive rising clock edges while waiting for available data. The AD6435/ AD6438 is free to place Bit 7 of a byte on the TX_SDATA pin even if the AD6439 will not be taking it, as long as the byte strobe is not pulsed. Once the byte strobe is pulsed for Bit 7, the TX_DREQ line is ignored until all 8 bits are sent.

Once TX_DREQ is raised, the AD6439 leaves TX_DREQ high and samples TX_BS on successive rising edges of the clock. Once TX_BS is seen high (ref T2), the AD6439 knows that Bit 7 can be sampled, followed by the remaining seven bits on the next seven rising clocks edges (ref T3). If desired, the TX_DREQ can be dropped at this time.

On the falling edge after Bit 1 has been sampled (ref T4), the AD6439 must raise or lower the TX_DREQ line depending on whether it knows it wants another byte immediately following the current byte. This timing is needed to ensure the AD6435/ AD6438 can detect the TX_DREQ signal as it outputs the last bit.

The TX_FRAME signal, which is not shown, is output by the AD6439 on the rising edge of TX_RX_SCLK to signify the start of a frame. The AD5435/AD5438 does not respond to the TX_DREQ line before the start of a frame, or after the number of data bytes programmed by the DSP has been transferred within a frame.

RX Serial Interface

The RX serial interface between the AD6439 and AD6435/ AD6438 uses five signals:

TX_RX_SCLK:	Serial clock provided by AD6439
RX_FRAME:	Frame strobe provided by AD6439
RX_BS:	Byte strobe provided by AD6439
TX_SDATA:	Serial data provided by AD6439
RX_DREQ:	Data request provided by AD6435/AD6438

Figure 10 shows the timing of the RX interface port signals.

This is a byte protocol. The AD6435/AD6438 raises RX_DREQ on the rising edge of TX_RX_SCLK to request data (ref T0). The AD6439 samples the RX_DREQ on its rising clock and, when seen, outputs a one clock byte strobe RX_BS (ref T1), and at the same time places Bit 7 of the byte on the RX_SDATA pin. On the next seven rising clocks, the AD6439 places Bits 6 through 0 on the RX_SDATA pin. As the last bit is output, the RX_DREQ line is again sampled (ref T5), and if high, and another byte is ready to transmit, outputs the byte strobe coincident with the MSB of the next byte, then proceeds to output the remainder of the byte in successive clock cycles.

If RX_DREQ were low, or another byte not yet available, the byte strobe would not be output, and RX_DREQ would continue to be sampled on successive rising clock edges while waiting for available data. The AD6439 is free to place Bit 7 of the next byte on the pin even if RX_DREQ is low, as long the byte strobe is not pulsed. Once the byte strobe is pulsed for Bit 7, the RX_DREQ line is ignored until all eight bits are sent.

Once RX_DREQ is raised, The AD6435/AD6438 leaves RX_DREQ high and samples RX_BS on successive falling edges of the clock. Once RX_BS is seen high (ref T2), the AD6435/AD6438 samples Bit 0 and knows that the data bits can be sampled on the next 7 falling clocks edges (ref T3). If desired, the RX_DREQ can be dropped at this time. When Bit 1 is being sampled (ref T4), the AD6435/AD6438 must raise or lower the RX_DREQ line depending on whether it knows it wants another byte immediately following the current byte. This timing is needed to ensure the AD6439 can detect the RX_DREQ signal on the rising edge after the last bit.

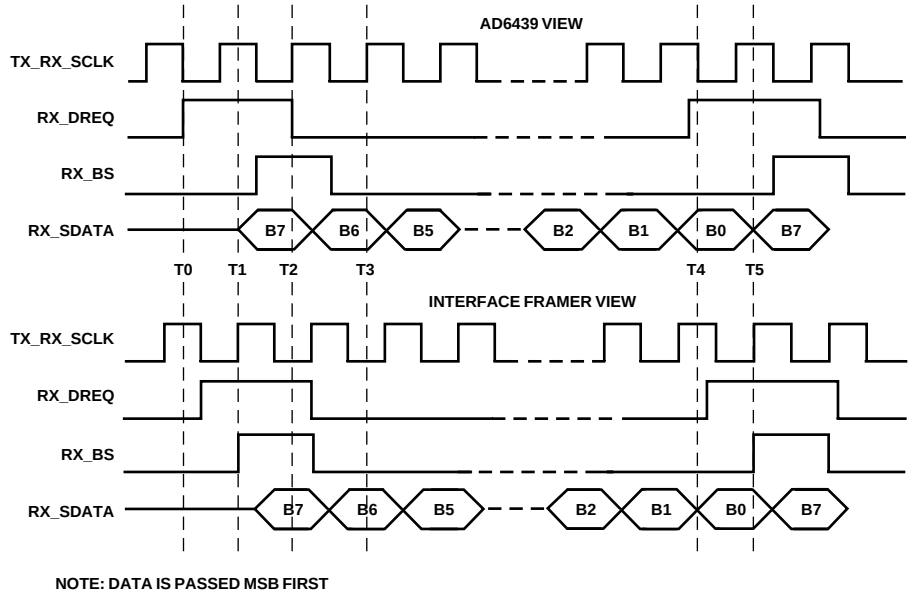


Figure 10. RX Serial Port Timing

Because of the direction of the clock skew, this protocol allows up to one full cycle of skew less some period for settling round trip timing (AD6439 to AD6435/AD6438 and back, or vice-versa). The main difference from the TX path is that the data and RX_BS are sampled by the AD6435/AD6438 on the falling clock edge because of the known direction of clock skew. The time from data request to Bit 7 being received is only one clock (assuming the AD6439 has data ready), so even for the worst case of 9 clocks per byte, the time to transmit a full frame is less than 97 μs, which should be within the safe window for the AD6439.

The RX_FRAME signal, which is not shown, is output by the AD6439 on the rising edge of TX_RX_SCLK to indicate the start of a frame. The AD6435/AD6438 does not raise the RX_DREQ line before the start of a frame, or after the number of data bytes programmed by the DSP has been received within a frame.

DAC Interface

The AD6439 provides 16 bits (TX[15:0]) to a Tx A/D converter and 16 bits (AEC[15:0]) to the AEC A/D (see Figure 8 for the location of this block and Figure 11 for signal timing). These two buses are muxed onto one 16-bit output bus provided to the analog front end (AD6437, AD6440). The TX_CLK signal accompanying the 16-bit data bus qualifies TX and AEC data.

The output bus always provides valid tx sample data on the rising edge of TX_CLK and valid AEC sample data on the falling of TX_CLK. During normal operation, the TX and AEC output sample rates are 17.664 MHz, therefore, on the output data bus, the rate is 35.328 MHz and TX_CLK is 17.664 MHz. TX and AEC data can be down sampled to 8.832 MHz, in which case the output data bus has a rate of 17.664 MHz and the TX_CLK signal is 8.832 MHz. The TX Int8 and AEC Int8 blocks can also be bypassed, making the TX and AEC data rate only 2.208 MHz, the output bus rate 4.416 MHz and the TX_CLK signal 2.208 MHz. Data sent out is unsigned, however the AD6439 can be programmed to send out twos complement binary data.

Note that TX and AEC paths must always be in the same mode. They are either both in normal mode, both in downsample mode, or both in bypass mode.

ADC Interface

The AD6439 includes an interface that accepts 16 bits (RX[15:0]) from an A/D converter (see Figure 8 for the location of this block). The sample rate is 8.832 MHz, but if the Dec4 block is bypassed, the rate is only 2.208 MHz. Signal RX_CLK qualifies when the A/D converter needs to provide valid data. The AD6439 normally assumes that input data is in unsigned binary format, however, it can also be programmed to received twos complement binary data.

DSP Port

The AD6439 includes a DSP port consisting of a 14-bit address bus A[13:0], a 16-bit data bus D[15:0], three bus control pins, NRD, NWR, NCS, and a clock, DSP_CLK. (See Figure 8 for the location of this block and Figure 12 for signal details). The DSP port allows a 2183 DSP to access the AD6439.

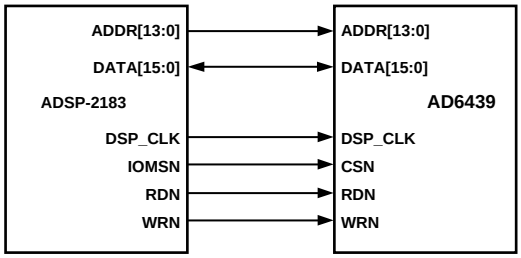


Figure 12. ADSP-2183 AD6439 Interface

PIN DESCRIPTION

The AD6439 carries 79 signal pins (24 output pins, 39 input pins, and 16 bidirectional pins) and 43 supply pins. See Figure 13 (Functional Diagram), Pin Configuration and Pin Function Description) for details.

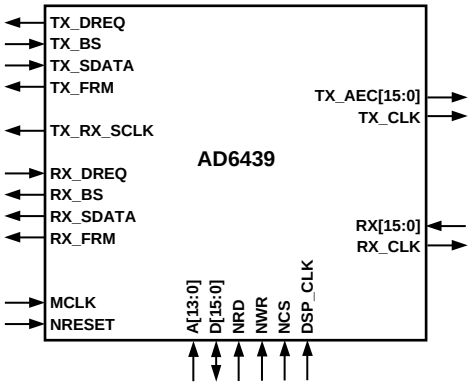


Figure 13. Functional Pin Diagram

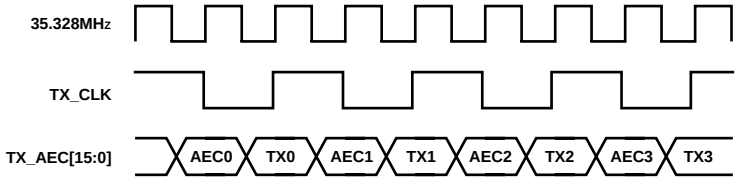
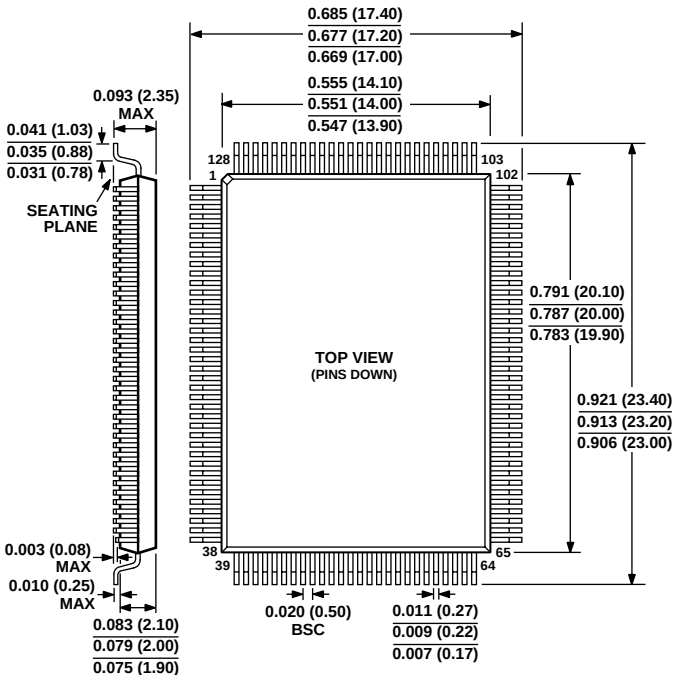


Figure 11. TX_AEC Mux Bus in Normal Operation

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

128-Lead MQFP Plastic Quad Flatpack
(S-128B)



C3514–3–3/99

PRINTED IN U.S.A.