

## Preliminary Technical Data

# AD5544

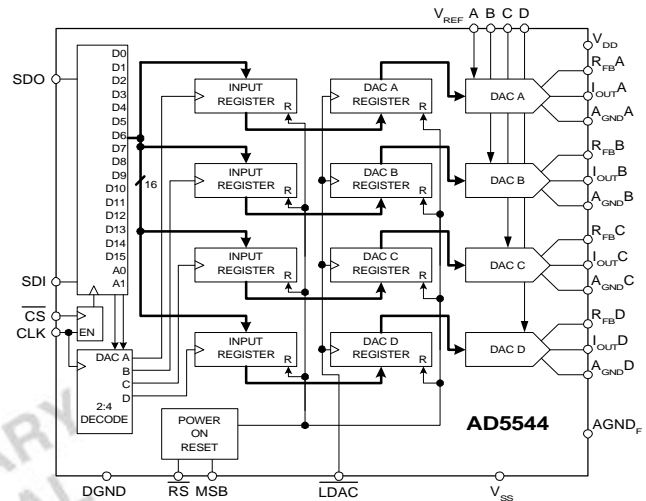
### FEATURES

- 16-bit Resolution**
- 2mA Full Scale Current  $\pm 20\%$ , with  $V_{REF}=10V$**
- 2 $\mu$ s Settling Time**
- $V_{SS}$  BIAS for reduced Zero Scale Error @Temp**
- Midscale (MSB) or Zero Scale Reset**
- 4 Separate 4Q Multiplying Reference-inputs**
- SPI Compatible 3-Wire Interface**
- Double Buffered Registers Enable**  
Simultaneous All Channel Change
- Internal Power ON Reset**
- Compact SSOP-28 Package**

### APPLICATIONS

- Automatic Test Equipment**
- Instrumentation**
- Digitally Controlled Calibration**

### FUNCTIONAL DIAGRAM



### GENERAL DESCRIPTION

The AD5544 quad, 16-bit, a current-output, digital-to-analog converter is designed to operate from a single +5 volt supply.

The applied external reference input voltage  $V_{REF}$  determines the full-scale output-current. On board feedback resistors ( $R_{FB}$ ) provide temperature-tracking full-scale voltage outputs when combined with an external I to V precision amplifier.

A doubled-buffered serial-data interface offers high-speed, three-wire, SPI and micro controller compatible inputs using serial-data-in (SDI), clock (CLK), and a chip-select ( $\overline{CS}$ ). In addition a serial-data-out pin (SDO) allows for daisy chaining when multiple packages are used. A common level-sensitive load-DAC strobe ( $\overline{LDAC}$ ) input allows simultaneous update of all DAC outputs from previously loaded Input Registers. Additionally, an internal power ON reset forces the output voltage to zero at system turn ON. An MSB pin allows system reset assertion ( $\overline{RS}$ ) to force all registers to zero code when  $MSB=0$ , or to half-scale code when  $MSB=1$ .

The AD5544 is packaged in the compact SSOP-28.

### ORDERING GUIDE

MODEL	INL (LSB)	DNL (LSB)	TEMP RANGE	Package Description	Package Option
AD5544JRS	$\pm 4$	$\pm 1.5$	0 / +70°C	SSOP-28	RS-28
AD5544ARS	$\pm 4$	$\pm 1.5$	-40 / +85°C	SSOP-28	RS-28

The AD5544 contains 4196 transistors. The die size measures 122 mil X 204 mil.

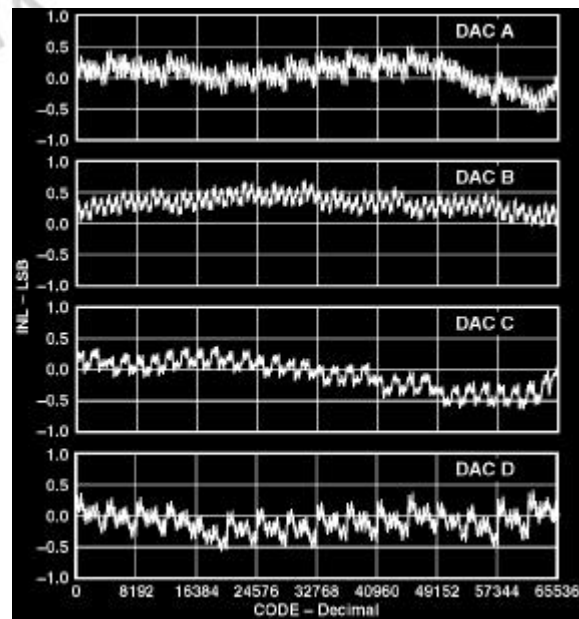


Figure 1. INL Vs Code Plot

REV. PrE, Nov '99

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**ELECTRICAL CHARACTERISTICS** at  $V_{DD} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $I_{OUTX} = \text{Virtual GND}$ ,  $A_{GNDX} = 0V$ ,  $V_{REFA,B,C,D} = 10V$ ,  $T_A = \text{Full Operating temperature Range}$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	5V±10%	UNITS
<b>STATIC PERFORMANCE<sup>1</sup></b>				
Resolution	N	1 LSB = $V_{REF}/2^{16} = 153\mu V$ when $V_{REF} = 10V$	16	Bits
Relative Accuracy	INL		±4	LSB max
Differential Nonlinearity	DNL		±1.5	LSB max
Output Leakage Current	$I_{OUTX}$	Data = 0000 <sub>H</sub> , $T_A = 25^\circ C$	10	nA max
Output Leakage Current	$I_{OUTX}$	Data = 0000 <sub>H</sub> , $T_A = T_A \text{ MAX}$	50	nA max
Full-Scale Gain Error	$G_{FSE}$	$T_A = 25^\circ C$ , Data = FFFF <sub>H</sub>	±2/±10	mV typ/max
Full-Scale Gain Error	$G_{FSE}$	$T_{A-MAX}$ , Data = FFFF <sub>H</sub> , $V_{SS} = -300mV$	±10	mV max
Full-Scale Gain Error	$G_{FSE}$	$T_A = T_{A-MIN}$ , Data = FFFF <sub>H</sub>	±50	mV max
Full-Scale Tempco <sup>2</sup>	$TCV_{FS}$		1	ppm/°C typ
<b>REFERENCE INPUT</b>				
$V_{REFX}$ Range	$V_{REFX}$		-15/+15	V min/max
Input Resistance	$R_{REFX}$		5	k ohm typ <sup>4</sup>
Input Resistance Match	$R_{REFX}$	Channel-to-Channel	1	% typ <sup>4</sup>
Input Capacitance <sup>2</sup>	$C_{REFX}$		5	pF typ
<b>ANALOG OUTPUT</b>				
Output Current	$I_{OUTX}$	Data = FFFF <sub>H</sub>	2	mA typ
Output Capacitance <sup>2</sup>	$C_{OUTX}$	Code Dependent	200	pF typ
<b>LOGIC INPUTS &amp; OUTPUT</b>				
Logic Input Low Voltage	$V_{IL}$		0.8	V max
Logic Input High Voltage	$V_{IH}$		2.4	V min
Input Leakage Current	$I_{IL}$		10	μA max
Input Capacitance <sup>2</sup>	$C_{IL}$		10	pF max
Logic Output Low Voltage	$V_{OL}$	$I_{OL} = 1.6mA$	0.4	V max
Logic Output High Voltage	$V_{OH}$	$I_{OH} = 100\mu A$	4	V min
<b>INTERFACE TIMING<sup>2,3</sup></b>				
Clock Width High	$t_{CH}$		30	ns min
Clock Width Low	$t_{CL}$		30	ns min
CS to Clock Set Up	$t_{CSS}$		0	ns min
Clock to CS Hold	$t_{CSH}$		25	ns min
Clock to SDO Prop Delay	$t_{PD}$		2/20	ns min/max
Load DAC Pulse Width	$t_{LDAC}$		20	ns min
Data Setup	$t_{DS}$		10	ns min
Data Hold	$t_{DH}$		15	ns min
Load Setup	$t_{LDS}$		20	ns min
Load Hold	$t_{LDH}$		20	ns min
<b>SUPPLY CHARACTERISTICS</b>				
Power Supply Range	$V_{DD \text{ RANGE}}$		4.5/5.5	V min/max
Positive Supply Current	$I_{DD}$	Logic Inputs = 0V	100	μA max
Negative Supply Current	$I_{SS}$	Logic Inputs = 0V	0.001/1	μA typ/max
Power Dissipation	$P_{DISS}$	Logic Inputs = 0V	0.3	mW max
Power Supply Sensitivity	PSS	$\Delta V_{DD} = \pm 5\%$	0.006	%/% max

## NOTES:

- All static performance tests (except  $I_{OUT}$ ) are performed in a closed loop system using an external precision OP177 I-to-V converter amplifier. The AD5544  $R_{FB}$  terminal is tied to the amplifier output. Typical values represent average readings measured at 25°C
- These parameters are guaranteed by design and not subject to production testing.
- All input control signals are specified with  $t_R = t_F = 2.5ns$  (10% to 90% of +3V) and timed from a voltage level of 1.5V.
- All AC Characteristic tests are performed in a closed loop system using an OP42 I-to-V converter amplifier.

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PARAMETER	SYMBOL	CONDITION	5V±10%	UNITS
<b>AC CHARACTERISTICS</b>				
Output Voltage Settling Time	$t_S$	To $\pm 0.1\%$ of Full Scale, Data = 0000 <sub>H</sub> to FFFF <sub>H</sub> to 0000 <sub>H</sub>	2	$\mu s$ typ
Reference Multiplying BW	BW-3dB	$V_{REFX} = 100mV_{rms}$ , Data = FFFF <sub>H</sub> , $C_{FB} = 15pF$	2	MHz
DAC Glitch Impulse	Q	$V_{REFX} = 0V$ , Data 0000 <sub>H</sub> to 8000 <sub>H</sub> to 0000 <sub>H</sub>	45	nV-s typ
Feed Through Error	$V_{OUTX}/V_{REFX}$	Data = 0000 <sub>H</sub> , $V_{REFX} = 100mV_{rms}$ , $f = 10KHz$	-68	dB
Crosstalk Error	$V_{OUTA}/V_{REFB}$	Data = 0000 <sub>H</sub> , $V_{REFB} = 100mV_{rms}$ , adjacent channel	-70	dB
Digital Feed Through	Q	CS = 1, and $f_{CLK} = 1MHz$	5	nV-s typ
Total Harmonic Distortion	THD	$V_{REF} = 5V_{P-P}$ , Data = FFFF <sub>H</sub> , $f = 1KHz$	-73	dB typ
Output Spot Noise Voltage	$e_N$	$f = 1kHz$ , BW = 1Hz		nV/ rt Hz

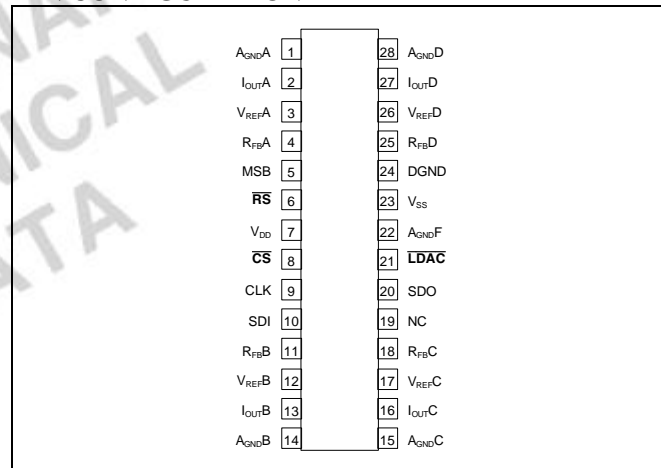
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## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to GND	-0.3V, +8V
$V_{SS}$ to GND	0.3V, -7V
$V_{REF}$ to GND	-18V, 18V
Logic Inputs & Output to GND	-0.3V, +8V
$V(I_{OUT})$ to GND	-0.3V, $V_{DD} + 0.3V$
$A_{GNDX}$ to DGND	-0.3V, +0.3V
Input Current to Any Pin except Supplies	$\pm 50mA$
Package Power Dissipation	$(T_J \text{ MAX} - T_A) / \text{THETA}_{JA}$
Thermal Resistance $\text{THETA}_{JA}$	
28-lead Shrink Surface Mount (RS-28)	100°C/W
Maximum Junction Temperature ( $T_J \text{ MAX}$ )	150°C
Operating Temperature Range	
Models A, B, C	-40°C to +85°C
Models J, K, L	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature:	
R-28 (Vapor Phase, 60 secs)	+215°C
RS-28 (Infrared, 15 secs)	+220°C

## PIN CONFIGURATION



Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

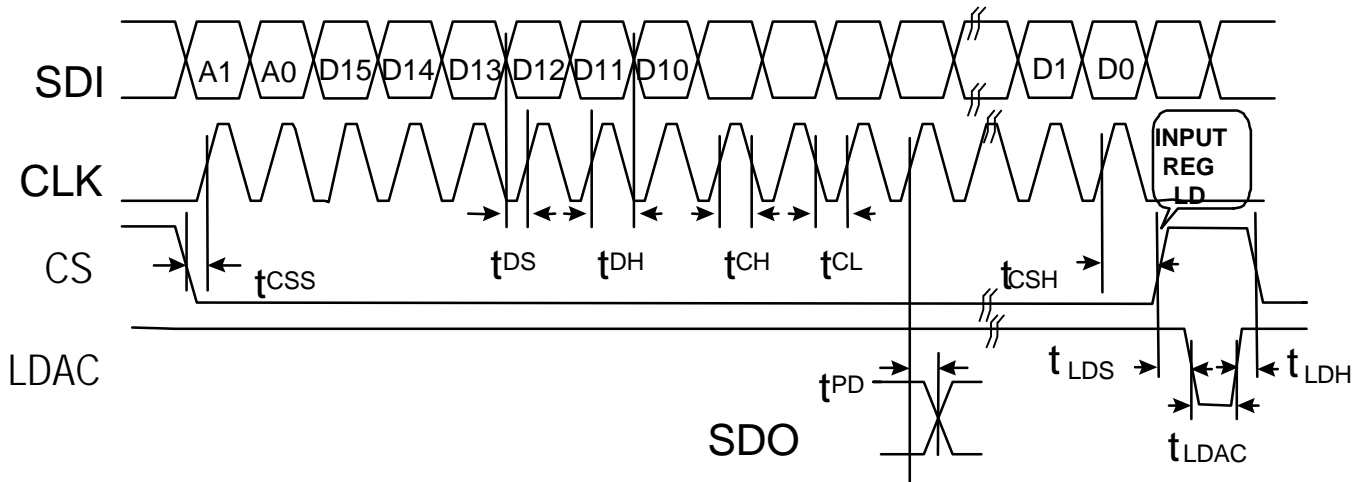


Figure 2. Timing Diagram

Table 1. Control-Logic Truth Table

CS	CLK	LDAC	RS	MSB	Serial Shift Register Function	Input Register Function	DAC Register
H	X	H	H	X	No Effect	Latched	Latched
L	L	H	H	X	No Effect	Latched	Latched
L	↑+	H	H	X	Shift-Register-Data advanced one bit	Latched	Latched
L	H	H	H	X	No Effect	Latched	Latched
↑+	L	H	H	X	No Effect	Selected DAC Updated with current SR contents	Latched
H	X	L	H	X	No Effect	Latched	Transparent
H	X	H	H	X	No Effect	Latched	Latched
H	X	↑+	H	X	No Effect	Latched	Latched
H	X	H	L	0	No Effect	Latched Data = 0000 <sub>H</sub>	Latched Data = 0000 <sub>H</sub>
H	X	H	L	H	No Effect	Latched Data = 8000 <sub>H</sub>	Latched Data = 8000 <sub>H</sub>

Notes:

1. SR = Shift Register
2. ↑+ positive logic transition; X Don't Care
3. At power ON both the Input Register and the DAC Register are loaded with all zeros.
4. Data appears at the SDO pin 19 clock pulses after input at the SDI pin.

Table 2. AD5544 Serial Input Register Data Format, Data is loaded in the MSB-First Format.

Bit Position	MSB																	LSB
	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data Word	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Note: Only the last 18 bits of data clocked into the serial register (Address + Data) are inspected when the CS line's positive edge returns to logic high. At this point an internally generated load strobe transfers the serial register data contents (bits D15-D0) to the decoded DAC-Input-Register address determined by bits A1 and A0. Any extra bits clocked into the AD5544 shift register are ignored, only the last 18 bits clocked in are used. If double buffered data is not needed, the LDAC pin can be tied logic low to disable the DAC Registers.

Table 3. Address Decode:

A1	A0	DAC Decoded
0	0	DAC A
0	1	DAC B
1	0	DAC C
1	1	DAC D

## PIN DESCRIPTION

PIN#	Name	Function
1	AGNDA	DAC A analog ground.
2	IOUTA	DAC A current output.
3	VREFA	DAC A Reference voltage input terminal. Establishes DAC A Full-Scale output voltage. Pin can be tied to V <sub>DD</sub> pin.
4	RFB A	DAC A voltage output connection to external amplifier.
5	MSB	MSB bit set pin during a reset pulse (RS) or at system power ON if tied to ground or V <sub>DD</sub> .
6	$\overline{\text{RS}}$	Reset pin, active low input. Input registers and DAC registers are set to all zeros or half-scale code (8000 <sub>H</sub> ) determined by the voltage on the MSB pin. Register Data = 0000 <sub>H</sub> when MSB = 0, Register Data = 8000 <sub>H</sub> when MSB = 1.
7	V <sub>DD</sub>	Positive power supply input. Specified range of operation +5V±10%.
8	$\overline{\text{CS}}$	Chip Select, active low input. Disables shift register loading when high. Transfers Serial Register Data to the Input Register when CS/LD returns High. Does not effect LDAC operation.
9	CLK	Clock input, positive edge clocks data into shift register.
10	SDI	Serial Data Input, input data loads directly into the shift register.
11	RFB B	DAC B voltage output connection to external amplifier.
12	VREFB	DAC B Reference voltage input terminal. Establishes DAC B Full-Scale output voltage. Pin can be tied to V <sub>DD</sub> pin.
13	IOUTB	DAC B current output.
14	AGNDB	DAC B analog ground.
15	AGNDC	DAC C analog ground.
16	IOUTC	DAC C current output.
17	VREFC	DAC C Reference voltage input terminal. Establishes DAC C Full-Scale output voltage. Pin can be tied to V <sub>DD</sub> pin.
18	RFB C	DAC C voltage output connection to external amplifier.
19	NC	No Connect. Leave pin unconnected.
20	SDO	Serial Data Output, input data loads directly into the shift register. Data appears at SDO, 19 clock pulses after input at the SDI pin.
21	$\overline{\text{LDAC}}$	Load DAC Register strobe, level sensitive active low. Transfers all Input Register data to DAC registers. Asynchronous active low input. See Control Logic Truth Table for operation.
22	AGNDF	High current analog force ground.
23	V <sub>SS</sub>	Negative Bias power supply input. Specified range of operation -0.3 to -5.5V.
24	DGND	Digital Ground Pin.
25	RFB D	DAC D voltage output connection to external amplifier.
26	VREFD	DAC D Reference voltage input terminal. Establishes DAC D Full-Scale output voltage. Pin can be tied to V <sub>DD</sub> pin.
27	IOUTD	DAC D current output.
28	AGNDD	DAC D analog ground.

## CIRCUIT OPERATION

The AD5544 contains four, 16-bit, current-output, digital-to-analog converters. Each DAC has its own independent multiplying reference input. The AD5544 uses a 3-wire SPI compatible serial data interface, with a configurable asynchronous  $\overline{\text{RS}}$  pin for half-scale (MSB=1) or zero-scale (MSB=0) preset. In addition, a  $\overline{\text{LDAC}}$  strobe enables four channel simultaneous updates for hardware synchronized output voltage changes.

### D/A Converter Section

Each part contains four current-steering R-2R ladder DACs. Figure 3 shows a typical equivalent DAC. Each DAC contains a matching feedback resistor for use with an external I to V converter amplifier. The R<sub>FBX</sub> pin is connected to the output of the external amplifier. The I<sub>OUTX</sub> terminal is connected to the inverting input of the external amplifier. The A<sub>GNDX</sub> pin should be Kelvin connected to the load point in the circuit requiring the full 16-bit accuracy. These DACs are designed to operate with both negative or positive reference voltages. The V<sub>DD</sub> power pin is only used by the logic to drive the DAC switches ON and OFF. Note that a matching switch is used in series with the internal 5K-ohm feedback resistor. If users are attempting to measure the value of R<sub>FB</sub>, power must be applied to V<sub>DD</sub> in order to achieve continuity. An additional V<sub>SS</sub> bias pin is used to guard the substrate during high temperature

applications to minimize zero scale leakage currents that double every 10°C. The V<sub>REF</sub> input voltage and the digital data (D) loaded into the corresponding DAC register according to equation [1] determine the DAC output voltage:

$$V_{\text{OUT}} = -V_{\text{REF}} * D / 65,536 \quad \text{Equation 1}$$

Note that the output full-scale polarity is opposite to the V<sub>REF</sub> polarity for DC reference voltages.

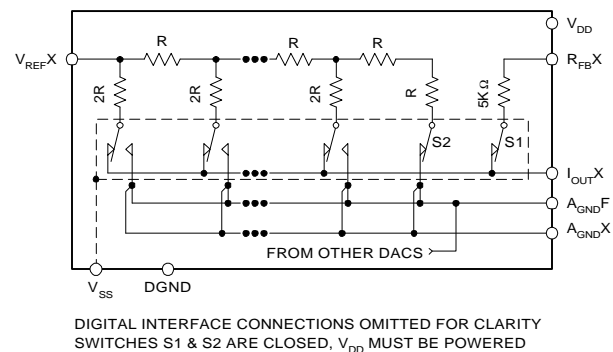


Figure 3. Typical Equivalent DAC Channel

These DACs are also designed to accommodate AC reference input signals. The AD5544 will accommodate input reference voltages in the range of -12 to +12 volts. The reference voltage

# Preliminary Technical Data

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inputs exhibit a constant nominal input-resistance value of 5K ohms,  $\pm 30\%$ . The DAC outputs  $I_{OUTA,B,C,D}$  are code-dependent producing various output resistances and capacitances. External amplifier choice should take into account the variation in impedance generated by the AD5544 on the amplifiers inverting input node. The feedback resistance in parallel with the DAC ladder resistance dominates output voltage noise. For multiplying mode applications an external feedback compensation capacitor  $C_{FB}$  may be needed to provide a critically damped output response for step changes in reference input voltages. Figure M shows the gain Vs frequency performance at various attenuation settings using an 15pF external feedback capacitor connected across the  $I_{OUTX}$  and  $R_{FBX}$  terminals. In order to maintain good analog performance, power supply bypassing of 0.01uF in parallel with 1uF is recommended. Under these conditions clean power supply voltages (low ripple, avoid switching supplies) appropriate for the application should be used. It is best to derive the AD5544's +5V supply from the systems analog supply voltages. (Don't use the digital 5V supply). See figure 4.

REF LEVEL 0.000dB /DIV 12.000dB  
AD5544 VDD = +5V, VREF = 100mVrms, TA = 25C

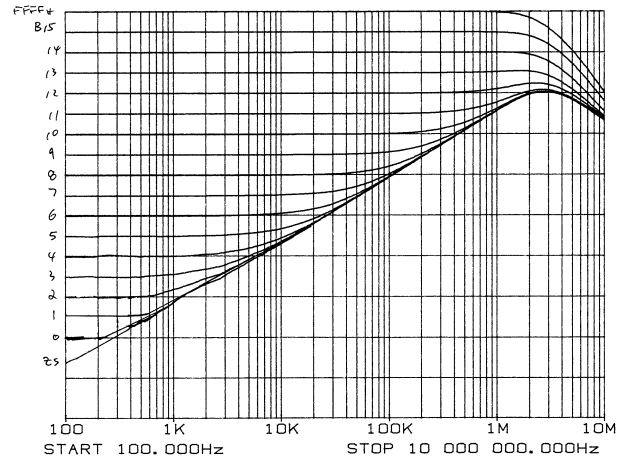


Figure M. Reference Multiplying Bandwidth Vs Code

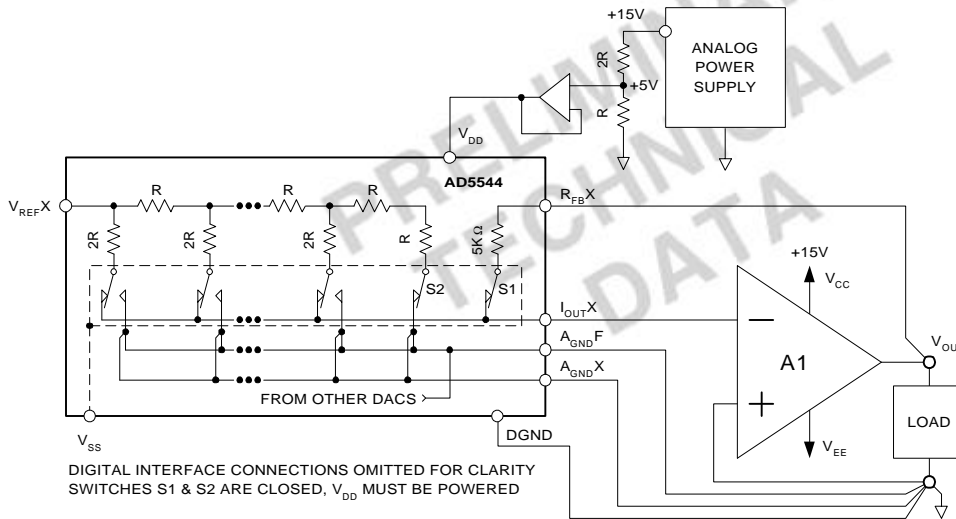


Figure 4. Recommended Kelvin Sensed hookup

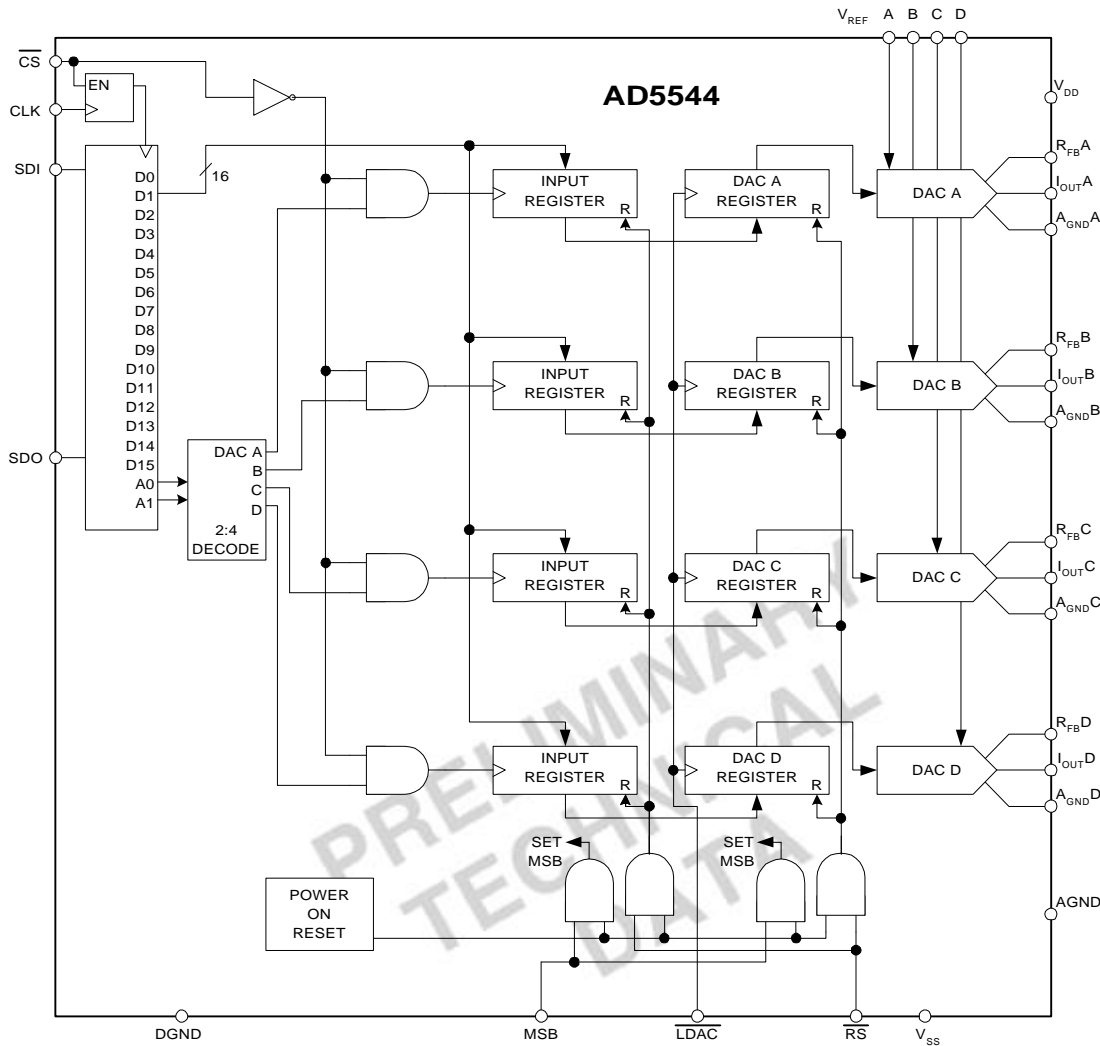


Figure 5. System Level Digital Interfacing

**SERIAL DATA INTERFACE**

The AD5544 uses a 3-wire ( $\overline{CS}$ , SDI, CLK) SPI compatible serial data interface. New serial data is clocked into the serial input register in a 18-bit data-word format. MSB bits are loaded first. Table 2 defines the 18 data-word bits. Data is placed on the SDI pin, and clocked into the register on the positive clock edge of CLK subject to the data setup and data hold time requirements specified in the INTERFACE TIMING SPECIFICATIONS. Data can only be clocked in while the CS chip select pin is active low. Only the last 18-bits clocked into the serial register will be interrogated when the CS pin returns to the logic high state, extra data bits are ignored. Since most micro controllers' output serial data in 8-bit bytes, three right justified data bytes can be written to the AD5544. Keeping the  $\overline{CS}$  line low between the first, second, and third byte transfer will result in a successful serial register update.

Once the data is properly aligned in the shift register the positive edge of the  $\overline{CS}$  initiates either the transfer of new data to the target DAC register determined by the decoding of address bits A1 & A0. Table 1, 2, 3 and Figure 2 defines the remaining characteristics of the software serial interface.

Figures 5 & 6 show the equivalent logic interface for the key digital control pins.

Two additional pins  $\overline{RS}$  and MSB provide hardware control over the preset function and DAC Register loading. If these functions are not needed, the  $\overline{RS}$  pin can be tied to logic high. The asynchronous input  $\overline{RS}$  pin forces all input and DAC registers to either the zero-code state (MSB=0), or the half-scale state (MSB=1).

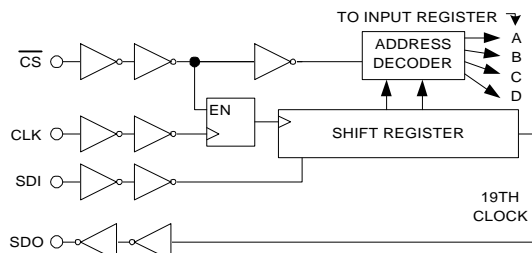


Figure 6. Equivalent Logic Interface

**POWER ON RESET**

When the  $V_{DD}$  power supply is turned ON an internal reset strobe forces all the Input and DAC registers to the zero-code

