+2.5V to 5.5V, 115μA Single Rail-to-Rail Voltage-Output DACs with Parallel Interface

Preliminary Technical Data AD5330/AD5331/AD5340/AD5341*

FEATURES

- **AD5330: Single 8-Bit DAC in 20-Lead TSSOP**
- **AD5331: Single 10-Bit DAC in 20-Lead TSSOP**
- **AD5340: Single 12-Bit DAC in 24-Lead TSSOP**
- **AD5341: Single 12-Bit DAC in 20-Lead TSSOP**
- **Micro-power Operation: 115μA @3V, 140μA @5V**
- **Power-Down to 80nA @3V, 200nA @5V**
- **+2.5V to +5.5V Power Supply**
- **Double-Buffered Input Logic**
- **Guaranteed Monotonic by Design Over All Codes**
- **Buffered/Unbuffered Reference Input Options**
- **0-V_{REF} or 0-2V_{REF} Output Range**
- **Power-On Reset to Zero Volts**
- **Simultaneous Update of DAC Outputs via LDAC**
- **Asynchronous CLR facility**
- **Low Power Parallel Data Interface**
- **On-Chip Rail-to-Rail Output Buffer Amplifiers**

APPLICATIONS

- **Portable Battery-Powered Instruments**
- **Digital Gain and Offset Adjustment**
- **Programmable Voltage and Current Sources**
- **Programmable Attenuators**
- **Industrial Process Control**

GENERAL DESCRIPTION

The AD5330/AD5331/AD5340/AD5341 are single 8-, 10- and 12- bit DACs. They operate from a +2.5V to +5.5V supply consuming just 115μA at 3V and feature a power-down mode which further reduces the current down to 80nA. These devices incorporate an on-chip output buffer which can drive the output to both supply rails, while the AD5330, AD5340 and AD5341 allow a choice of buffered or unbuffered reference input.

The AD5330/AD5331/AD5340/AD5341 have a parallel interface. $\overline{CS}$ selects the device and data is loaded into the input registers on the rising edge of $\overline{WR}$.

The GAIN pin allows the output range to be set at 0V to V_{REF} or 0V to $2 \times V_{REF}$.

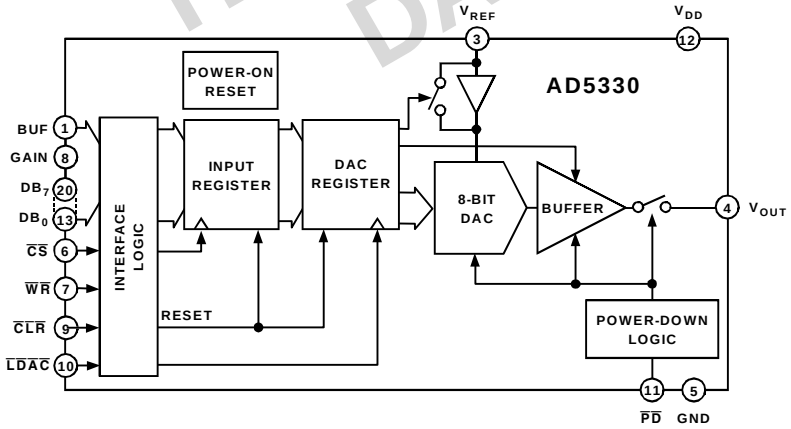
Input data to the DACs is double-buffered, allowing simultaneous update of multiple DACs in a system using the $\overline{LDAC}$ pin.

An asynchonous $\overline{CLR}$ input is also provided, which resets the contents of the Input Register and the DAC Register to all zeros. These devices also incorporate a power-on-reset circuit that ensures that the DAC output powers on to 0V and remains there until valid data is written to the device.

The AD5330/AD5331/AD5340/AD5341 are available in Thin Shrink Small Outline Packages (TSSOP).

AD5330 FUNCTIONAL BLOCK DIAGRAM

(Other Diagrams Inside)



***Protected by U.S. Patent Number 5684481; other patents pending.**

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AD5330/AD5331/AD5340/AD5341–SPECIFICATIONS

(V_{DD} = +2.5V to +5.5V, V_{REF} = +2V. DAC output unloaded. All specifications T_{MIN} to T_{MAX} unless otherwise noted).

Parameter[1]	B Version[2] Min	Typ	Max	Units	Conditions/Comments
DC PERFORMANCE[3]					
AD5330					
Resolution		8		Bits	
Relative Accuracy		±0.15	±1	LSB	
Differential Nonlinearity		±0.02	±0.25	LSB	Guaranteed Monotonic by design over all codes
AD5331					
Resolution		10		Bits	
Relative Accuracy		±0.5	±3	LSB	
Differential Nonlinearity		±0.05	±0.5	LSB	Guaranteed Monotonic by design over all codes
AD5340/AD5341					
Resolution		12		Bits	
Relative Accuracy		±2	±12	LSB	
Differential Nonlinearity		±0.2	±1	LSB	Guaranteed Monotonic by design over all codes
Offset Error		±0.4	±3	% of FSR	
Gain Error		±0.15	±1	% of FSR	
Lower Deadband[4]		10	60	mV	Lower Deadband exists only if offset error is negative
Offset Error Drift[5]		-12		ppm of FSR/°C	
Gain Error Drift[5]		-5		ppm of FSR/°C	
DC Power Supply Rejection Ratio[5]		-60		dB	ΔV_{DD} = ±10%
DAC REFERENCE INPUT[5]					
V_{REF} Input Range	1		V_{DD}	V	Buffered Reference (AD5330, AD5340 and AD5341)
	0		V_{DD}	V	Unbuffered Reference
V_{REF} Input Impedance		>10		MΩ	Buffered Reference (AD5330, AD5340 and AD5341)
		180		kΩ	Unbuffered Reference. Gain=1. Input Impedance=R_{DAC}
		90		kΩ	Unbuffered Reference. Gain=2. Input Impedance=R_{DAC}
Reference Feedthrough		-90		dB	Frequency=10kHz
OUTPUT CHARACTERISTICS[5]					
Minimum Output Voltage[6]		0.001		V min	Rail-to-rail operation.
Maximum Output Voltage[6]		V_{DD}-0.001		V max	
DC Output Impedance		0.5		Ω	
Short Circuit Current		50		mA	V_{DD} = +5V
		20		mA	V_{DD} = +3V
Power-Up Time		2.5		µs	Coming out of Power-Down Mode. V_{DD} = +5V
		5		µs	Coming out of Power-Down Mode. V_{DD} = +3V
LOGIC INPUTS[5]					
Input Current		±1		µA	
V_{IL}, Input Low Voltage			0.8	V	V_{DD} = +5V ±10%
			0.6	V	V_{DD} = +3V ±10%
			0.5	V	V_{DD} = +2.5V
V_{IH}, Input High Voltage	2.4			V	V_{DD} = +5V ±10%
	2.1			V	V_{DD} = +3V ±10%
	2.0			V	V_{DD} = +2.5V
Pin Capacitance		3.5		pF	
POWER REQUIREMENTS					
V_{DD}	2.5		5.5	V	
I_{DD} (Normal Mode)					Note: I_{DD} specification is valid for all DAC codes.
V_{DD}= +4.5V to +5.5V		140	250	µA	DAC is active in Unbuffered Mode and load current
V_{DD}= +2.5V to +3.6V		115	200	µA	is excluded. V_{IH} = V_{DD} and V_{IL} = GND.
					I_{DD} increases by 50µA at V_{REF} > V_{DD}-100mV.
					In Buffered Mode, extra current is typically x µA
I_{DD} (Full Power Down)					where x=5µA+V_{REF}/R_{DAC}
V_{DD} = +4.5V to +5.5V		0.2	1	µA	
V_{DD} = +2.5V to +3.6V		0.08	1	µA	

NOTES

[1]See Terminology (page 9)

[2]Temperature range: B Version: -40°C to +105°C.

[3]Linearity is tested using a reduced code range: AD5330 (code 8 to 255); AD5331 (code 28 to 1023); AD5340/AD5341 (code 115 to 4095)

[4]This corresponds to x codes. x = Deadband voltage/LSB size

[5]Guaranteed by Design and Characterization, not production tested.

[6]In order for the amplifier output to reach its minimum voltage, Offset Error must be negative. In order for the amplifier output to reach its maximum voltage, V_{REF}=V_{DD} and "Offset plus Gain" Error must be positive.

Specifications subject to change without notice.

AC CHARACTERISTICS[1]

(V_{DD} = +2.5V to +5.5V. R_L = 2kΩ to GND and 2kΩ to V_{DD}; C_L = 200pF to GND. All specifications T_{MIN} to T_{MAX} unless otherwise noted).

Parameter[2]	B Version[3] Min	Typ	Max	Units	Conditions/Comments
Output Voltage Settling Time					V_{REF} = +2V. See Figure x
AD5330		6	8	µs	1/4 Scale to 3/4 Scale change (40 H to C0 H)
AD5331		7	9	µs	1/4 Scale to 3/4 Scale change (100 H to 300 H)
AD5340		8	10	µs	1/4 Scale to 3/4 Scale change (400 H to C00 H)
AD5341		8	10	µs	1/4 Scale to 3/4 Scale change (400 H to C00 H)
Slew Rate		0.7		V/µs	
Major Code Transition Glitch Energy		12		nV-s	1 LSB change around major carry (011...11 to 100...00)
Digital Feedthrough		0.10		nV-s	
Multiplying Bandwidth		200		kHz	V_{REF}=2V±0.1Vpp. Unbuffered Mode
Total Harmonic Distortion		-70		dB	V_{REF}=2.5V±0.1Vpp . Frequency=10kHz.

NOTES:
[1]Guaranteed by design and characterization, not production tested.
[2]See Terminology
[3]B Version: Industrial temperature range -40°C. to +105°C.
Specifications subject to change without notice

TIMING CHARACTERISTICS[1]

(V_{DD} = +2.5V to +5.5 V; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[2,3]	Limit at T_{MIN}, T_{MAX} (B Version)[4]	Units	Conditions/Comments
t_1	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	20	ns min	$\overline{WR}$ Pulse Width
t_4	5	ns min	Data, GAIN, BUF, HBEN Setup Time
t_5	4.5	ns min	Data GAIN, BUF, HBEN Hold Time
t_6	5	ns min	Synchronous Mode. $\overline{WR}$ Falling to $\overline{LDAC}$ Falling
t_7	5	ns min	Synchronous Mode. $\overline{LDAC}$ Falling to $\overline{WR}$ Rising.
t_8	4.5	ns min	Synchronous Mode. $\overline{WR}$ Rising to $\overline{LDAC}$ Rising.
t_9	5	ns min	Asynchronous Mode. $\overline{LDAC}$ Rising to $\overline{WR}$ Rising
t_{10}	4.5	ns min	Asynchronous Mode. $\overline{WR}$ Rising to $\overline{LDAC}$ Falling.
t_{11}	20	ns min	$\overline{LDAC}$ Pulse Width
t_{12}	20	ns min	$\overline{CLR}$ Pulse Width
t_{13}	50	ns min	Time between $\overline{WR}$ cycles

NOTES:
[1]Guaranteed by design and characterization, not production tested.
[2]See Terminology
[3]See Figure 1
[4]B Version: Industrial temperature range -40°C. to +105°C.
Specifications subject to change without notice

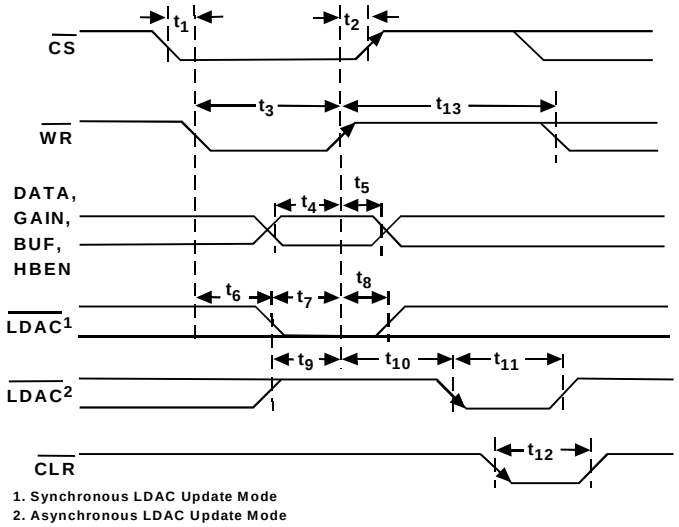


Figure 1. Parallel Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... -0.3 V to +7 V
Digital Input Voltage to GND ..... -0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND ..... -0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND . -0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND ..... -0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Industrial (B Version) ..... -40°C to +105°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
TSSOP Package
  Power Dissipation ..... (T_J max - T_A) / θ_{JA} mW
  Θ_{JA} Thermal Impedance (20-Lead TSSOP)... 143°C/W
  Θ_{JA} Thermal Impedance (24-Lead TSSOP)... 128°C/W
  Θ_{JC} Thermal Impedance (20-Lead TSSOP)... 45°C/W
  Θ_{JC} Thermal Impedance (24-Lead TSSOP)... 42°C/W
  Reflow Soldering
    Peak Temperature ..... 220 +5/-0 °C
    Time at Peak Temperature ..... 10 sec to 40 sec

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

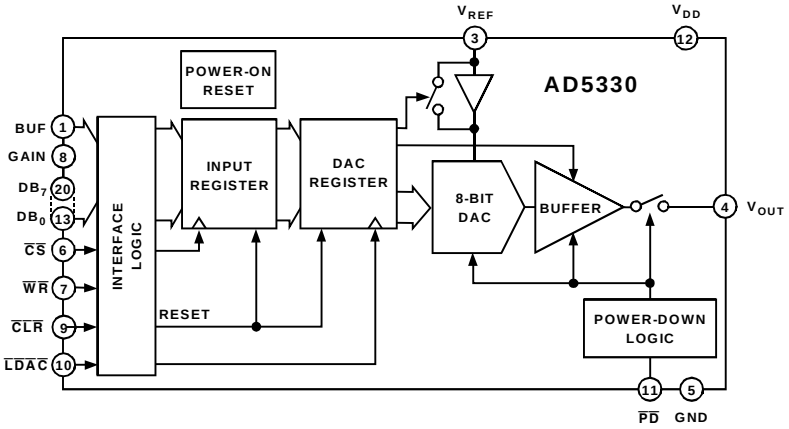
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD5330BRU	–40°C to +105°C	RU-20
AD5331BRU	–40°C to +105°C	RU-20
AD5340BRU	–40°C to +105°C	RU-24
AD5341BRU	–40°C to +105°C	RU-20

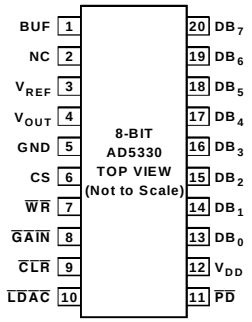
*RU = TSSOP (Thin Shrink Small Outline Package)

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5330/AD5331/AD5340/AD5341 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges.Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



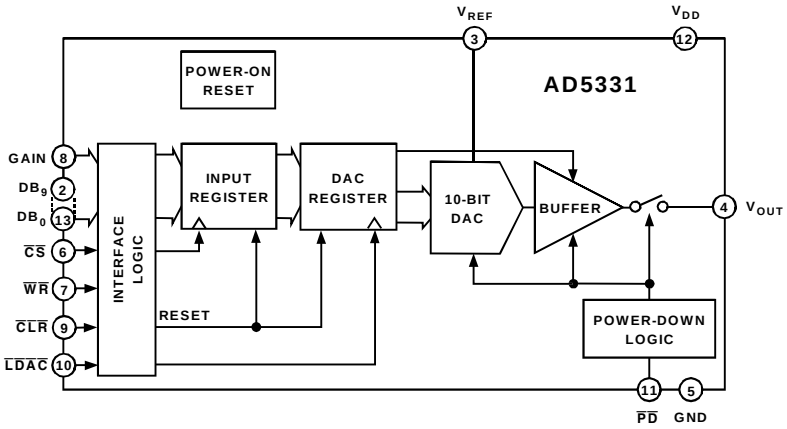
AD5330 FUNCTIONAL BLOCK DIAGRAM



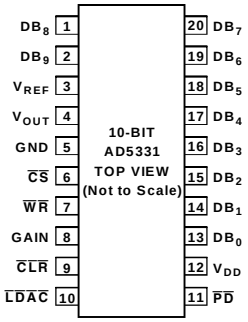
AD5330 PIN CONFIGURATION

AD5330 PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Function
1	BUF	Buffer control pin. This pin controls whether the reference input to the DAC is buffered or unbuffered.
2	NC	No Connect
3	V_{REF}	Reference input.
4	V_{OUT}	Output of DAC. Buffered output with rail-to-rail operation.
5	GND	Ground reference point for all circuitry on the part.
6	$\overline{CS}$	Active low Chip Select input. This is used in conjunction with $\overline{WR}$ to write data to the parallel interface.
7	$\overline{WR}$	Active low Write input. This is used in conjunction with $\overline{CS}$ to write data to the parallel interface.
8	GAIN	Gain control pin. This controls whether the output range from the DAC is 0-V_{REF} or 0-2$V_{REF.}$
9	$\overline{CLR}$	Asynchronous active-low control input which clears all input registers and DAC registers to zero.
10	$\overline{LDAC}$	Active-low control input which updates the DAC registers with the contents of the input registers.
11	$\overline{PD}$	Power-Down pin. This active low control pin puts the DAC into power-down mode.
12	V_{DD}	Power Supply pin. This part is operated from +2.5V to +5.5V.
13-20	DB_0-DB_7	8 Parallel Data Inputs. DB_7 is the MSB of these 8 bits.



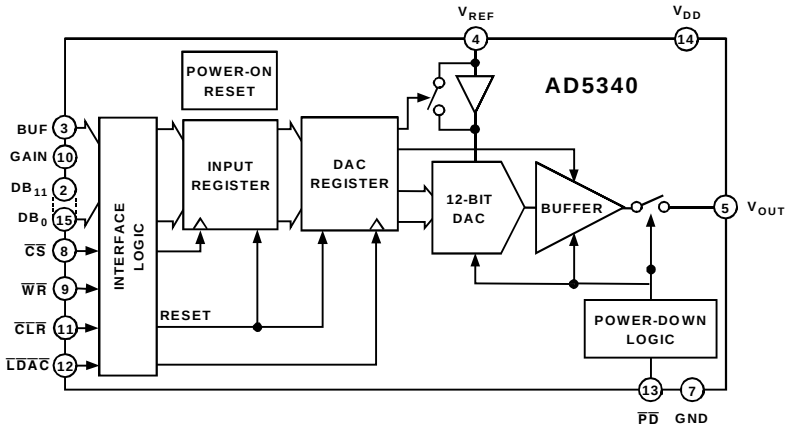
AD5331 FUNCTIONAL BLOCK DIAGRAM



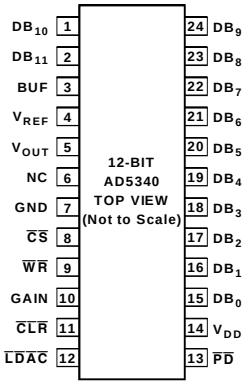
AD5331 PIN CONFIGURATION

AD5331 PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Function
1	DB_8	Parallel Data input.
2	DB_9	Most Significant Bit of Parallel Data input.
3	V_{REF}	Unbuffered reference input.
4	V_{OUT}	Output of DAC. Buffered output with rail-to-rail operation.
5	GND	Ground reference point for all circuitry on the part.
6	$\overline{CS}$	Active low Chip Select input. This is used in conjunction with $\overline{WR}$ to write data to the parallel interface.
7	$\overline{WR}$	Active low Write input. This is used in conjunction with $\overline{CS}$ to write data to the parallel interface.
8	GAIN	Gain control pin. This controls whether the output range from the DAC is 0-V_{REF} or 0-2$V_{REF.}$
9	$\overline{CLR}$	Active-low control input which clears all input registers and DAC registers to zero.
10	$\overline{LDAC}$	Active-low control input which updates the DAC registers with the contents of the input registers.
11	$\overline{PD}$	Power-Down pin. This active low control pin puts the DAC into power-down mode.
12	V_{DD}	Power Supply pin. This part operates from +2.5V to +5.5V.
13-20	DB_0-DB_7	8 Parallel Data Inputs.



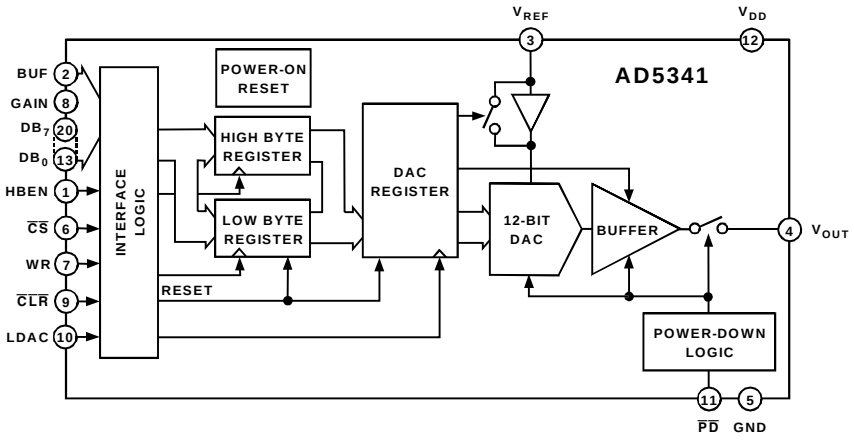
AD5340 FUNCTIONAL BLOCK DIAGRAM



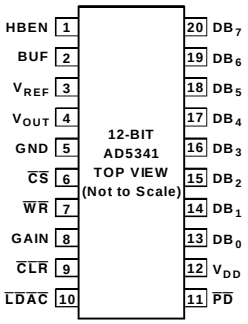
AD5340 PIN CONFIGURATION

AD5340 PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Function
1	DB_{10}	Parallel Data input.
2	DB_{11}	Most Significant Bit of Parallel Data input.
3	BUF	Buffer control pin. This pin controls whether the reference input to the DAC is buffered or unbuf fered.
4	V_{REF}	Reference input.
5	V_{OUT}	Output of DAC. Buffered output with rail-to-rail operation.
6	NC	No Connect.
7	GND	Ground reference point for all circuitry on the part.
8	$\overline{CS}$	Active low Chip Select input. This is used in conjunction with $\overline{WR}$ to write data to the parallel interface.
9	$\overline{WR}$	Active low Write input. This is used in conjunction with $\overline{CS}$ to write data to the parallel interface.
10	GAIN	Gain control pin. This controls whether the output range from the DAC is 0-V_{REF} or 0-2$V_{REF.}$
11	$\overline{CLR}$	Asynchronous active-low control input which clears all input registers and DAC registers to zero.
12	$\overline{LDAC}$	Active-low control input which updates the DAC registers with the contents of the input registers.
13	$\overline{PD}$	Power-Down pin. This active low control pin puts the DAC into power-down mode.
14	V_{DD}	Power Supply pin. This part operates from +2.5V to +5.5V.
15-24	DB_0-DB_9	10 Parallel Data Inputs.



AD5341 FUNCTIONAL BLOCK DIAGRAM



AD5341 PIN CONFIGURATION

AD5341 PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Function
1	HBEN	Hign Byte Enable pin. This pin is used when writing to the device to determine if data is written to the high byte register or the low byte register.
2	BUF	Buffer control pin. This pin controls whether the reference input to the DAC is buffered or unbuf fered.
3	V_{REF}	Reference input.
4	V_{OUT}	Output of DAC. Buffered output with rail-to-rail operation.
5	GND	Ground reference point for all circuitry on the part.
6	$\overline{CS}$	Active low Chip Select input. This is used in conjunction with $\overline{WR}$ to write data to the parallel interface.
7	$\overline{WR}$	Active low Write input. This is used in conjunction with $\overline{CS}$ to write data to the parallel interface.
8	GAIN	Gain control pin. This controls whether the output range from the DAC is 0-V_{REF} or 0-2$V_{REF.}$
9	$\overline{CLR}$	Asynchronous active-low control input which clears all input registers and DAC registers to zero.
10	$\overline{LDAC}$	Active-low control input which updates the DAC registers with the contents of the input registers.
11	$\overline{PD}$	Power-Down pin. This active low control pin puts the DAC into power-down mode.
12	V_{DD}	Power Supply pin. This part operates from +2.5V to +5.5V.
13-20	DB_0-DB_7	8 Parallel Data Inputs. DB_7 is the MSB of these 8 bits.

TERMINOLOGY

RELATIVE ACCURACY

For the DAC, Relative Accuracy or Integral Nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the actual endpoints of the DAC transfer function. A typical INL vs. Code plot can be seen in Figure X.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. Code plot can be seen in Figure X.

OFFSET ERROR

This is a measure of the offset error of the DAC and the output amplifier. It is expressed as a percentage of the full-scale range.

If the offset voltage is positive the output voltage will still be positive at zero input code. This is shown in Figure X. Because the DAC operates from a single supply, a negative offset cannot appear at the output of the buffer amplifier. Instead, there will be a code close to zero at which the amplifier output saturates (amplifier footroom). Below this code there will be a deadband over which the output voltage will not change. This is illustrated in Figure X.

GAIN ERROR

This is a measure of the span error of the DAC (including any error in the gain of the buffer amplifier). It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range. This is illustrated in Figure X.

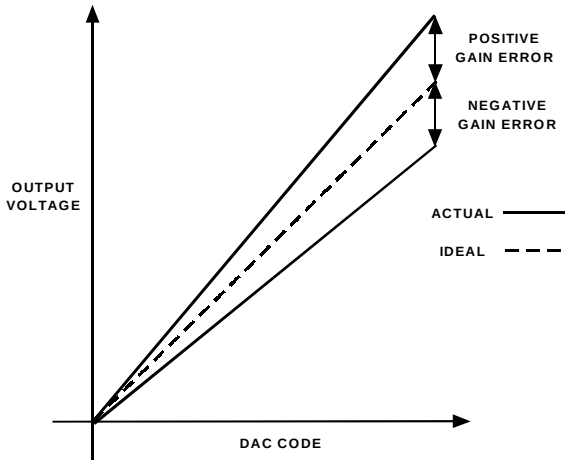


Figure X. Gain Error

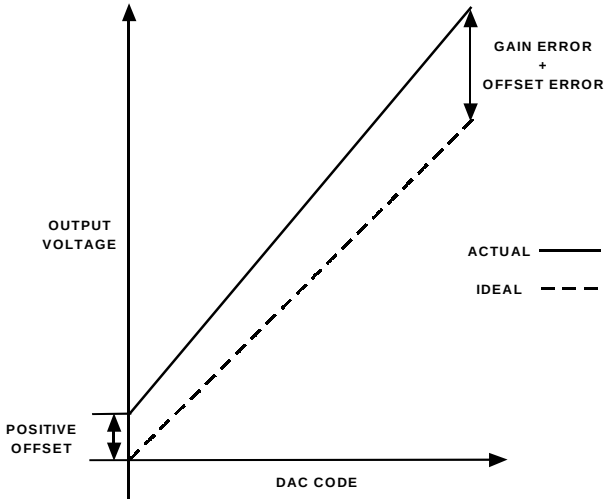


Figure X. Positive Offset Error And Gain Error

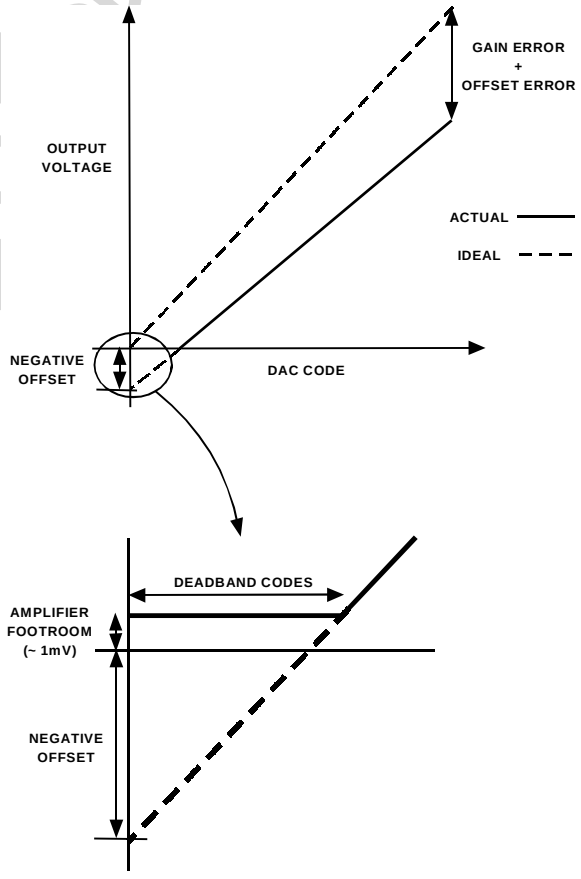


Figure X. Negative Offset Error And Gain Error

OFFSET ERROR DRIFT
This is a measure of the change in Offset Error with changes in temperature. It is expressed in (ppm of Full-Scale Range)/°C.

GAIN ERROR DRIFT
This is a measure of the change in Gain Error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

DC POWER-SUPPLY REJECTION RATIO (PSRR)
This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dBs. V_{REF} is held at +2V and V_{DD} is varied ± 10 %.

REFERENCE FEEDTHROUGH
This is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (i.e. $\overline{\text{LDAC}}$ is high). It is expressed in dBs.

MAJOR-CODE TRANSITION GLITCH ENERGY
Major-Code Transition Glitch Energy is the energy of the impulse injected into the analog output when the DAC changes state. It is normally specified as the area of the glitch in nV-secs and is measured when the digital code is chnged by 1LSB at the major carry transition (011...11 to 100...00 or 100...00 to 011...11).

DIGITAL FEEDTHROUGH
Digital Feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital input pins of the device but is measured when the DAC is not being written to ($\overline{\text{CS}}$ held high). It is specified in nV-secs and is measured with a full-scale change on the digital input pins, i.e. from all 0s to all 1s and vice versa.

MULTIPLYING BANDWIDTH
The amplifiers within the DAC have a finite bandwidth. The Multiplying Bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The Multiplying Bandwidth is the frequency at which the output amplitude falls to 3dB below the input.

TOTAL HARMONIC DISTORTION
This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC and the THD is a measure of the harmonics present on the DAC output.It is measured in dBs.

FUNCTIONAL DESCRIPTION

The AD5330/AD5331/AD5340/AD5341 are single resistor string DACs fabricated on a CMOS process with resolutions of 8, 10, 12 and 12 bits, respectively. They are written to using a parallel interface. They operate from single supplies of +2.5V to +5.5V and the output buffer amplifiers offer rail to rail output swing. The AD5330, AD5340 and AD5341 have a reference input that may be buffered to draw virtually no current from the reference source, or unbuffered to give a reference input range from ground to V_{DD}. The reference input of the AD5331 is unbuffered. The devices have a power-down feature that reduces current consumption to only 80nA @3V.

Digital-to-Analog Section

The architecture of one DAC channel consists of a reference buffer and a resistor-string DAC followed by an output buffer amplifier. The voltage at the V_{REF} pin provides the reference voltage for the DAC. Figure x shows a block diagram of the DAC architecture. Since the input coding to the DAC is straight binary, the ideal output voltage is given by:

$$V_{OUT} = V_{REF} \times \frac{D}{2^N} \times Gain$$

where:

D = decimal equivalent of the binary code which is loaded to the DAC register:

0-255 for AD5330 (8-bits)
0-1023 for AD5331 (10-bits)
0-4095 for AD5340/AD5341 (12-bits)

N = DAC resolution

Gain = Output Amplifier Gain (1 or 2)

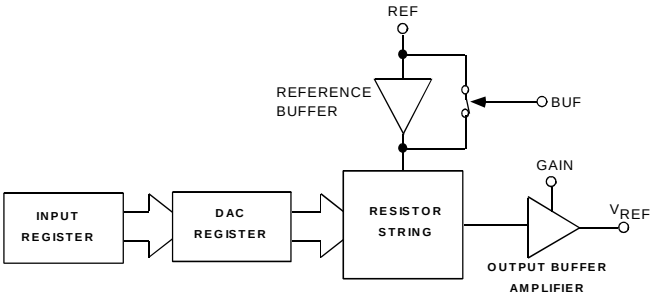


Figure 5. Single DAC Channel Architecture

Resistor String

The resistor string section is shown in Figure 6. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at what node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

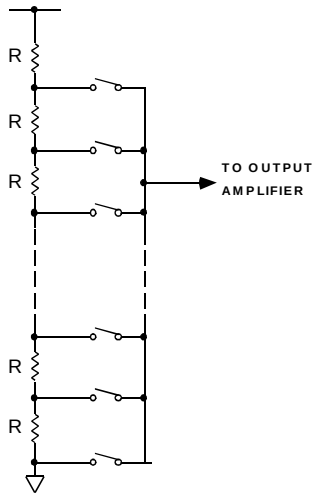


Figure 6. Resistor String

DAC Reference Input

There is a reference input pin for the DAC. The reference input is buffered on the AD5330/AD5340/AD5341 but can be configured as unbuffered also. The reference input of the AD5331 is unbuffered. The buffered/unbuffered option is controlled by the BUF pin.

In buffered mode (BUF=1) the current drawn from an external reference voltage is virtually zero, as the impedance is at least 10MΩ. The reference input range is 1V to 5V with a 5V supply.

In unbuffered mode (BUF=0) the user can have a reference voltage as low as GND and as high as V_{DD} since there is no restriction due to headroom and footroom of the reference amplifier. The impedance is still large at typically 180kΩ for 0-V_{REF} mode and 90kΩ for 0-2 V_{REF} mode.

If there is an external buffered reference (e.g. REF192) there is no need to use the on-chip buffer.

Output Amplifier

The output buffer amplifier is capable of generating output voltages to within 1mV of either rail. Its actual range depends on the value of the V_{REF}, GAIN and offset error. If a gain of 1 is selected (GAIN=0) the output range is 0.001 V to V_{REF}.

If a gain of 2 is selected (GAIN=1) the output range is 0.001 V to $2V_{REF}$. However because of clamping the maximum output is limited to V_{DD} - 0.001V.

The output amplifier is capable of driving a load of 2kΩ to GND and V_{DD}, in parallel with 500pF to an AC GND. The source and sink capabilities of the output amplifier can be seen in Figure x.

The slew rate is 0.7V/µs with a half-scale settling time to ±0.5 LSB (at 8 bits) of 6µs. See Figure x.

PARALLEL INTERFACE

The AD5330, AD5331 and AD5340 load their data as a single 8-, 10- or 12-bit word, while the AD5341 loads data as a low byte of 8 bits and a high byte containing 4 bits.

Double-Buffered Interface

The AD5330/AD5331/AD5340/AD5341 DACs all have double-buffered interfaces consisting of an input register and a DAC register. DAC data, BUF, and GAIN inputs are written to the input register under control of the Chip Select ($\overline{CS}$) and Write ($\overline{WR}$). LDAC is the signal which transfers data to the DAC register.

This feature allows data to be written sequentially to all DACs and peripherals without changing their outputs. Outputs of all DACs and peripherals may then be updated simultaneously using a common $\overline{LDAC}$ line. The gain and buffer control signals are also double buffered and are only updated when $\overline{LDAC}$ occurs.

Double-buffering is useful where the DAC data is loaded in two bytes, as in the AD5341, because it allows the whole data word to be assembled in parallel before updating the DAC register. This prevents spurious outputs that could occur if the DAC register was updated with only the high byte or the low byte.

Clear Input ($\overline{CLR}$)

$\overline{CLR}$ is an active-low, asynchronous clear that resets the input and DAC registers.

Chip Select Input ($\overline{CS}$)

$\overline{CS}$ is an active-low input that selects the device.

Write Input ($\overline{WR}$)

$\overline{WR}$ is an active-low input that controls writing of data to the device. Data is latched into the input register on the rising edge of $\overline{WR}$.

Load DAC Input ($\overline{LDAC}$)

LDAC transfers data from the input register to the DAC register (and hence updates the outputs). Use of the LDAC function enables double buffering of the DAC data, GAIN and BUF.

There are two $\overline{LDAC}$ modes:

Synchronous mode: In this mode the DAC register is updated after new data is read in on the rising edge of the $\overline{WR}$ input.

Asynchronous mode: In this mode the outputs are not updated at the same time that the input register is written to. When $\overline{LDAC}$ goes low the DAC register is updated with the contents of the input register.

High-Byte Enable Input (HBEN)

High-Byte Enable is a control input on the AD5341 only that determines if data is written to the high-byte input register or the low-byte input register.

The low data byte of the AD5341 consists of data bits 0 to 7 at data inputs DB_0 to DB_7, whilst the high byte consists of data bits 8 to 11 at data inputs DB_0 to DB_3. DB_4 to DB_7 are ignored during a high byte write, but they may be used for data to set up the reference input as buffered/ unbuffered, and buffer amplifier gain.

Figure 7. Data Format For AD5341

AD5330/AD5331/AD5340 TRUTH TABLE

$\overline{CLR}$	$\overline{LDAC}$	$\overline{CS}$	$\overline{WR}$	FUNCTION
1	1	1	X	No data transfer
1	1	X	1	No data transfer
0	X	X	X	Clear all registers
1	1	0	0→1	Load Input Register
1	0	0	0→1	Load Input Register and DAC Register, GAIN, BUF
1	0	X	X	Update DAC Register, GAIN, BUF

AD5341 TRUTH TABLE

$\overline{CLR}$	$\overline{LDAC}$	$\overline{CS}$	$\overline{WR}$	HBEN	FUNCTION
1	1	1	X	X	No data transfer
1	1	X	1	X	No data transfer
0	X	X	X	X	Clear all registers
1	1	0	0→1	0	Load Low Byte Input Register
1	1	0	0→1	1	Load High Byte Input Register
1	0	0	0→1	0	Load Low Byte Input Register and DAC Register, GAIN, BUF
1	0	0	0→1	1	Load High Byte Input Register and DAC Register, GAIN, BUF
1	0	X	X	X	Update DAC Register, GAIN, BUF

POWER-ON RESET

The A5330/AD5331/AD5340/AD5341 are provided with a power-on reset function, so that they power up in a defined state. The power-on state is:

- Normal operation
- Reference input unbuffered
- 0 - V_{REF} output range
- Output voltage set to 0V

Both input and DAC registers are filled with zeros and remain so until a valid write sequence is made to the device. This is particularly useful in applications where it is important to know the state of the DAC outputs while the device is powering-up.

POWER-DOWN MODE

The device can be put into a power-down mode by taking $\overline{PD}$ low. In this mode the DAC and output amplifier are powered down. The output of the buffer amplifier is disconnected which allows the output voltage to be tied to a defined voltage using an external resistor, if required. Note that the input register can be written to in power-down mode and holds it's value when $\overline{PD}$ is taken high. The current consumption in power-down mode is typically only 80nA @3V V_{DD} and 200nA @5V V_{DD}.

SUGGESTED DATABUS FORMATS

In most applications GAIN and BUF are hard-wired. However if more flexibility is required they can be included in a databus. This enables you to software program GAIN giving you the option to double the resolution in the lower half of the DAC range. In a bussed system GAIN and BUF may be treated as data inputs since they are written to the device during a write operation and take effect when $\overline{LDAC}$ is taken low. This means that the reference buffers and the output amplifier gain of multiple DAC devices can be controlled using common GAIN and BUF lines.

In the case of the AD5330 this means that the databus must be wider than 8 bits. The AD5331 and AD5340 databuses must be at least 10- and 12- bits wide respectively and are best suited to a 16-bit databus system.

Examples of data formats for putting GAIN and BUF on a 16-bit databus are shown in Figure x. Note that any unused bits above the actual DAC data may be used for BUF and GAIN.

Figure 8. Data format for GAIN and BUF data on a 16-bit Bus

The AD5341 is a 12-bit device that uses byte load, so only four bits of the high byte are actually used as data. Two of the unused bits can be used for GAIN and BUF data by connecting them to the GAIN and BUF inputs. e.g. bits 6 and 7, as shown in figures 9 and 10.

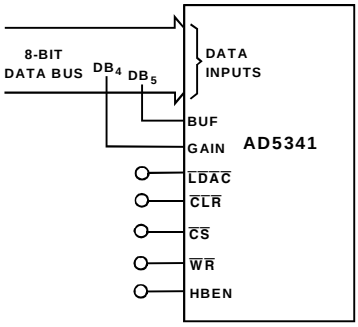


Figure 9. AD5341 With GAIN and BUF Data on 8-Bit Bus

In this case the low byte is written first in a write operation with HBEN=0. Bits 6 and 7 of DAC data will be written into GAIN nad BUF registers but will have no effect. The high byte is then written. Only the lower four bits of data are written into the DAC high byte register, so bits 6 and 7 can be GAIN and BUF data.

$\overline{LDAC}$ is used to update the DAC, GAIN and BUF values.

Figure 10. AD5341 Data Format for Byte Load with GAIN and BUF Data on 8-Bit Bus

APPLICATIONS INFORMATION

Power Supply Bypassing and Grounding

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5330/AD5331/AD5340/AD5341 is mounted should be designed so that the analog and digital sections are separated, and confined to certain areas of the board. If the device is in a system where multiple devices require an AGND to DGND connection, the connection should be made at one point only. The star ground point should be established as closely as possible to the DUT. The AD5330/AD5331/AD5340/AD5341 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on the supply located as closely to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the device should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

Typical Application Circuits

The AD5330/AD5331/AD5340/AD5341 can be used with a wide range of reference voltages, especially if the reference inputs are configured to be unbuffered, in which case the devices offer full, one-quadrant multiplying capability over a reference range of zero to V_{DD}. More typically, these devices may be used with a fixed, precision reference voltage. Figure x shows a typical setup for the devices when using an external reference connected to the unbuffered reference inputs. If the reference inputs are unbuffered, the reference input range is from 0 to V_{DD}, but if the on-chip reference buffers are used, the reference range is reduced. Suitable references for 5 V operation are the AD780 and REF192. For 2.5 V operation, a suitable external reference would be the AD589, a 1.23 V bandgap reference.

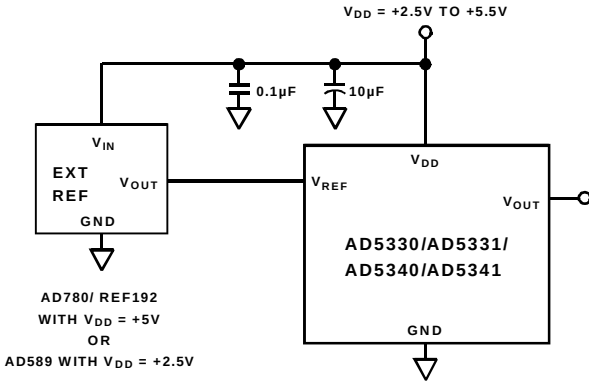


Figure 11. AD5330/AD5331/AD5340/AD5341 Using External Reference

If an output range of zero to V_{DD} is required when the reference inputs are configured as unbuffered (for example zero to +5V) then the simplest solution is to connect the reference inputs to V_{DD}. As this supply may not be very accurate and may be noisy, then the devices may be powered from the reference voltage, for example using a 5V reference such as the ADM663 or ADM666, as shown in figure 8.

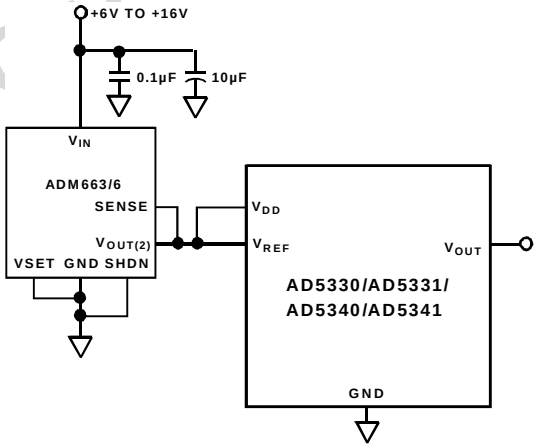


Figure 12 Using an ADM663/6 as Power and Reference to AD5330/AD5331/AD5340/AD5341

Bipolar Operation Using the AD5330/AD5331/AD5340/AD5341

The AD5330/AD5331/AD5340/AD5341 have been designed for single supply operation, but bipolar operation is achievable using the circuit shown in Figure x. The circuit shown has been configured to achieve an output voltage range of –5 V < V_O < +5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = [(1 + R4/R3) \times (R2/(R1 + R2) \times (2 \times V_{REF} \times D/2^N)] - V_{REF} \times R4/R3$$

where:

D is the decimal equivalent of the code loaded to the DAC, N is DAC resolution and V_{REF} is the reference voltage input.

With:

V_{REF} = 2.5 V

R1 = R3 = 10 kΩ

R2 = R4 = 20 kΩ and V_{DD} = 5 V.

$$V_{OUT} = 10 \times \frac{D}{2^N} - 5\ V$$

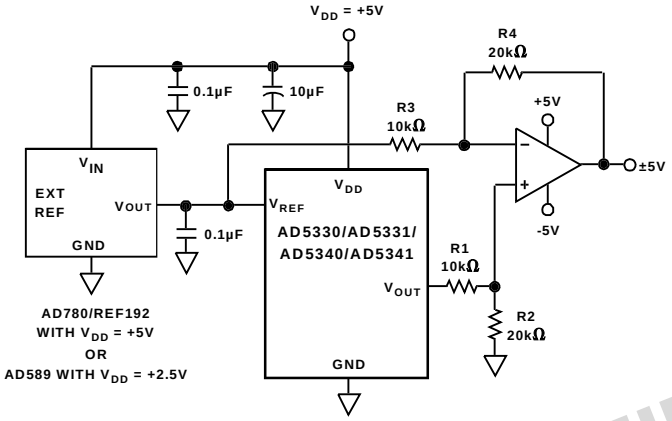


Figure 13. Bipolar Operation using the AD5330/AD5331/ AD5340/AD5341

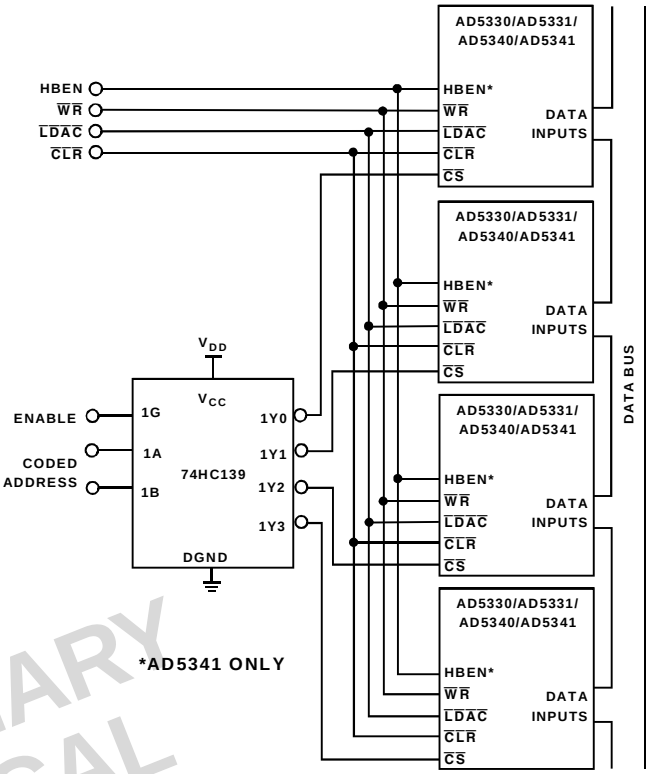


Figure 14.Decoding Multiple DAC devices

Decoding Multiple AD5330/AD5331/AD5340/AD5341

The $\overline{CS}$ pin on these devices can be used in applications to decode a number of DACs. In this application, all DACs in the system receive the same data and $\overline{WR}$ pulses, but only the $\overline{CS}$ to one of the DACs will be active at any one time, so data will only be written to the DAC whose $\overline{CS}$ is low. If multiple AD5341's are being used then a common HBEN line will also be required to determine if the data is written to the high byte- or low byte register of the selected DAC.

The 74HC139 is used as a 2- to 4-line decoder to address any of the DACs in the system. To prevent timing errors from occurring, the enable input should be brought to its inactive state while the coded address inputs are changing state. Figure 10 shows a diagram of a typical setup for decoding multiple devices in a system. Once data has been written sequentially to all DACs in a system, all the DACs can be updated simultaneously using a common $\overline{LDAC}$ line. A common $\overline{CLR}$ line can also be used to reset all DAC outputs to zero.

Programmable Current Source

Figure x shows the AD5332/AD5333/AD5342/AD5343 used as the control element of a programmable current source. In this example, the full-scale current is set to 1mA. The output voltage from the DAC is applied across the current setting resistor of 4.7kΩ in series with the 470Ω adjustment potentiometer, which gives an adjustment of about ±5%. Suitable transistors to place in the feedback loop of the amplifier include the BC107 and the 2N3904, which enable the current source to operate from a min V_{SOURCE} of 6 V. The operating range is determined by the operating characteristics of the transistor. Suitable amplifiers include the AD820 and the OP295, both having rail-to-rail operation on their outputs. The current for any digital input code and resistor value can be calculated as follows:

$$I = G \times V_{REF} \times \frac{D}{(2^N \times R)}\ mA$$

Where:

G is the gain of the buffer amplifier (1 or 2)

D is the decimal equivalent of the digital input code

N is the DAC resolution (8- 10- or 12-bits)

R is the sum of the resistor plus adjustment pot. in kΩ

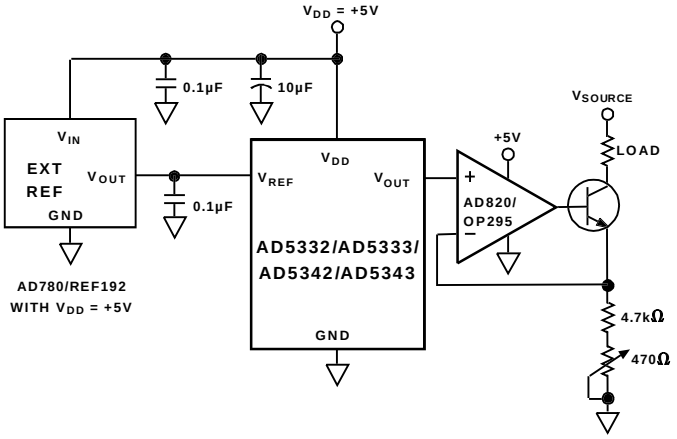
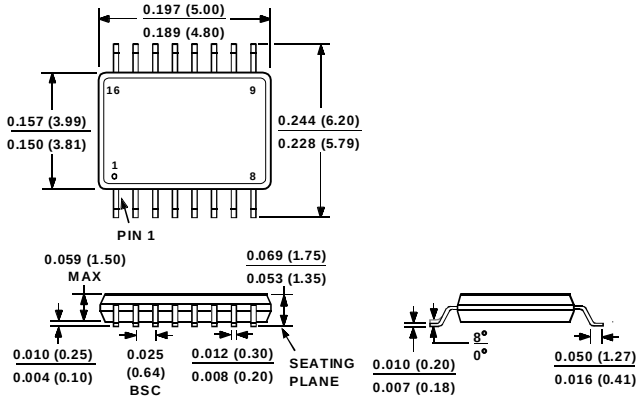


Figure 15. Programmable Current Source

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Pin TSSO Package (RU-20)



24-Pin TSSO Package (RU-24)