I²C Compatible Digital Potentiometers

Preliminary Technical Data

AD5241/AD5242

FEATURES
256 Position
Potentiometer Replacement
10K, 100K, 1M, Ohm
Internal Power ON Mid-Scale Preset
+2.7 to +5.5V Single-Supply; ±2.7V Dual-Supply Operation
I²C Compatible Interface

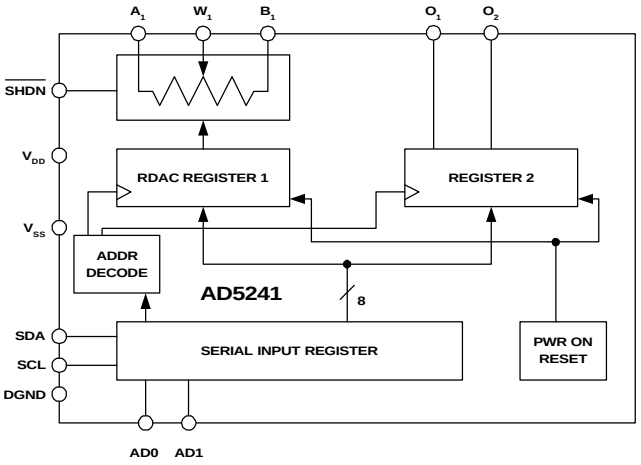
APPLICATIONS
Multi-Media, Video & Audio
Communications
Mechanical Potentiometer Replacement
Instrumentation: Gain, Offset Adjustment
Programmable Voltage to Current Conversion
Line Impedance Matching

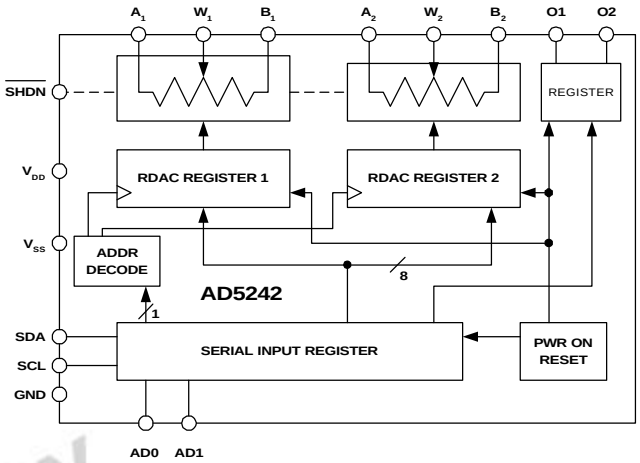
GENERAL DESCRIPTION

The AD5241/AD5242 provides a single/dual channel, 256 position digitally-controlled variable resistor (VR) device. These devices perform the same electronic adjustment function as a potentiometer, trimmer or variable resistor. Each VR offers a completely programmable value of resistance, between the A terminal and the wiper, or the B terminal and the wiper. The fixed A-to-B terminal resistance of 10, 100 or 1M ohms has a 1% channel-to-channel matching tolerance with a nominal temperature coefficient of 30 ppm/°C.

Wiper Position programming defaults to midscale at system power ON. Once powered the VR wiper position is programmed by a I²C compatible 2-wire serial data interface. An asynchronous reset (PR) pin forces the VR wiper to the midscale position. Both parts have two programmable logic outputs available to drive digital loads, gates, LED drivers, analog switches, etc.

FUNCTIONAL BLOCK DIAGRAMS





The AD5241/AD5242 are available in the surface mount (SO-14/-16) packages. For ultra compact solutions selected models are available in the thin TSSOP-14/-16 packages. All parts are guaranteed to operate over the extended industrial temperature range of -40°C to +85°C. For 3-wire, SPI compatible interface applications, see the AD5203/AD5204/AD5206/AD7376/AD8400/AD8402/AD8403 products.

ORDERING GUIDE

Model	Kilo Ohms	Temp	Package Description	Package Option
AD5241BR10	10	-40/+85°C	SO-14	R-14
AD5241BRU10	10	-40/+85°C	TSSOP-14	RU-14
AD5241BR100	100	-40/+85°C	SO-14	R-14
AD5241BRU100	100	-40/+85°C	TSSOP-14	RU-14
AD5241BR1M	1M	-40/+85°C	SO-14	R-14
AD5241BRU1M	1M	-40/+85°C	TSSOP-14	RU-14
AD5242BR10	10	-40/+85°C	SO-16	R-16
AD5242BRU10	10	-40/+85°C	TSSOP-16	RU-16
AD5242BR100	100	-40/+85°C	SO-16	R-16
AD5242BRU100	100	-40/+85°C	TSSOP-16	RU-16
AD5242BR1M	1M	-40/+85°C	SO-16	R-16
AD5242BRU1M	1M	-40/+85°C	TSSOP-16	RU-16

The AD5241/AD5242 die size is 69 mil X 78 mil, 5,382 sq. mil. Contains xxx transistors. Patent Number 5495245 applies.

PRELIMINARY TECHNICAL DATA

REV PrB 28 OCT 99

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ELECTRICAL CHARACTERISTICS 10K, 100K, 1M OHM VERSION (V_{DD} = +3V±10% or +5V±10%, V_A = +V_{DD}, V_B = 0V, -40°C < T_A < +85°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
DC CHARACTERISTICS RHEOSTAT MODE Specifications apply to all VRs						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A=NC R_{AB}=10KΩ	-1	±0.4	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A=NC R_{AB}=10KΩ	-1	±0.5	+1	LSB
Nominal resistor tolerance	ΔR	T_A = 25°C	-30		30	%
Resistance Temperature Coefficient	$R_{AB}/\Delta T$	V_{AB} = V_{DD}, Wiper = No Connect		30		ppm/°C
Wiper Resistance	R_W	I_W = V_{DD} /R, V_{DD} = +3V or +5V		40	100	Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE Specifications apply to all VRs						
Resolution	N		8			Bits
Integral Nonlinearity[4]	INL	R_{AB}=10KΩ	1	±0.5	+1	LSB
Integral Nonlinearity[4]	INL	R_{AB}=1MΩ	1	±0.5	+1	LSB
Differential Nonlinearity[4]	DNL	R_{AB}=10KΩ	1	±0.4	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 40_H		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = $7F_H$	1	-0.5	+0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00_H	0	+0.5	+1	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A,B,W}$		V_{SS}		V_{DD}	V
Capacitance[6] A, B	$C_{A,B}$	f = 1 MHz, measured to GND, Code = 40_H		45		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Code = 40_H		60		pF
Common Mode Leakage	I_{CM}	V_A = V_B = V_W		1		nA
DIGITAL INPUTS						
Input Logic High	V_{IH}	SDA & SCL	0.7V_{DD}		V_{DD}+0.5	V
Input Logic Low	V_{IL}	SDA & SCL	-0.5		0.3V_{DD}	V
Input Logic High	V_{IH}	AD0 & AD1	3.0		V_{DD}	V
Input Logic Low	V_{IL}	AD0 & AD1	0		1.0	V
Input Current	I_{IL}	V_{IN} = 0V or +5V			±1	µA
Input Capacitance[6]	C_{IL}			3		pF
DIGITAL Output						
Output Logic Low	V_{OL}	I_{OL} = 6mA SDA			0.4	V
Three-State Leakage Current	I_{OZ}	V_{IN} = 0V or +5V			±1	µA
Output Capacitance[6]	C_{OZ}			3	8	pF
POWER SUPPLIES						
Power Single-Supply Range	$V_{DD\ RANGE}$	V_{SS} = 0V	+2.7		+5.5	V
Power Dual-Supply Range	$V_{DD/SS\ RANGE}$		±2.3		±2.7	V
Positive Supply Current	I_{DD}	V_{IH} = +5V or V_{IL} = 0V		0.1	5	µA
Negative Supply Current	I_{SS}	V_{SS} = -2.5V, V_{DD} = +2.7V		0.1	5	µA
Power Dissipation[10]	P_{DISS}	V_{IH} = +5V or V_{IL} = 0V, V_{DD} = +5V		0.5	25	µW
Power Supply Sensitivity	PSS			0.05	0.015	%/%
DYNAMIC CHARACTERISTICS[6,9,11]						
Bandwidth 3dB	BW_10K	R_{AB} = 10KΩ, Code = 40_H		650		kHz
	BW_50K	R_{AB} = 50KΩ, Code = 40_H		142		kHz
	BW_100K	R_{AB} = 100KΩ, Code = 40_H		69		kHz
Total Harmonic Distortion	THD_W	V_A =1Vrms + 2V dc, V_B = 2V DC, f=1KHz		0.005		%
V_W Settling Time	t_S	V_A= V_{DD}, V_B=0V, ±1 LSB error band		2		µs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 5KΩ, f = 1KHz		14		nV√Hz

PRELIMINARY TECHNICAL DATA

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Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
INTERFACE TIMING CHARACTERISTICS applies to all parts(Notes 6,12)						
SCL Clock Frequency	f_{SCL}		0		100	KHz
t_{BUF} Bus free time between STOP & START	t_1		4.7			µs
$t_{HD;STA}$ Hold Time (repeated START)	t_2	After this period the first clock pulse is generated	4			µs
t_{LOW} Low Period of SCL Clock	t_3		4.7			µs
t_{HIGH} High Period of SCL Clock	t_4		4.0		50	µs
$t_{SU;STA}$ Setup Time For START Condition	t_5		4.7			µs
$t_{HD;DAT}$ Data Hold Time	t_6		300			ns
$t_{SU;DAT}$ Data Setup Time	t_7		250			ns
t_F Fall Time of both SDA & SCL signals	t_8				300	ns
t_R Rise Time of both SDA & SCL signals	t_9				1000	ns
$t_{SU;STO}$ Setup time for STOP Condition	t_{10}		4.0			µs

NOTES:

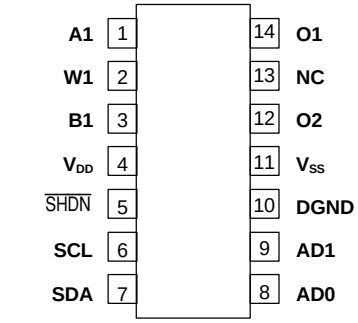
1. Typicals represent average readings at +25°C, V_{DD} = +5V.
2. Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. See figure 20 test circuit.
4. INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. V_A = V_{DD} and V_B = 0V. DNL specification limits of ±1LSB maximum are Guaranteed Monotonic operating conditions. See Figure 19 test circuit.
5. Resistor terminals A,B,W have no limitations on polarity with respect to each other.
6. Guaranteed by design and not subject to production test.
9. Bandwidth, noise and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value result in the minimum overall power consumption.
10. P_{DISS} is calculated from (I_{DD} x V_{DD}). CMOS logic level inputs result in minimum power dissipation.
11. All dynamic characteristics use V_{DD} = +5V.
12. See timing diagram for location of measured values.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted)

V_{DD} to GND ..... -0.3, +7V
V_{SS} to GND ..... 0V, -7V
V_{DD} to V_{SS} ..... +7V
V_A, V_B, V_W to GND ..... V_{SS}, V_{DD}
A_X – B_X, A_X – W_X, B_X – W_X ..... ±20mA
Digital Input Voltage to GND 0V, 7V
Operating Temperature Range ..... -40°C to +85°C
Package Power Dissipation ..... (T_{JMAX} - T_A) / θ_{JA}
Thermal Resistance θ_{JA},
SOIC (SO-14) ..... 158°C/W
SOIC (SO-16) ..... 73°C/W
TSSOP-14 ..... 206°C/W
TSSOP-16 ..... 180°C/W
Maximum Junction Temperature ($T_{J\,MAX}$) ..... +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature
R-14, R-16, RU-14, RU-16 (Vapor Phase, 60 sec) .. +215°C
R-14, R-16, RU-14, RU-16 (Infrared, 15 sec) ..... +220°C

AD5241 PIN CONFIGURATION



AD5242 PIN CONFIGURATION

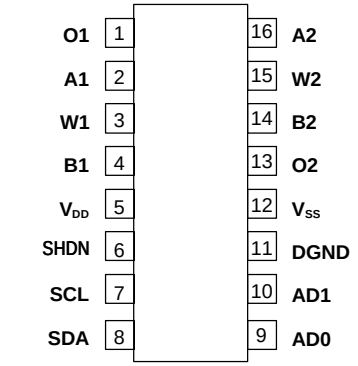


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TABLE 1: AD5241 PIN Function Descriptions

Pin	Name	Description
1	A_1	Resistor terminal A_1
2	W_1	Wiper terminal W_1
3	B_1	Resistor terminal B_1
4	V_{DD}	Positive power supply, specified for operation from +2.2 to +5.5V.
5	SHDN	Active Low, Asynchronous connection of the wiper W to terminal B, and open circuit of terminal A. RDAC register contents unchanged.
6	SCL	Serial Clock Input
7	SDA	Serial Data Input/Output
8	AD0	Programmable address bit for multiple package decoding. Bits AD0 & AD1 provide 4 possible addresses.
9	AD1	Programmable address bit for multiple package decoding. Bits AD0 & AD1 provide 4 possible addresses.
10	DGND	Common Ground
11	V_{SS}	Negative power supply, specified for operation from 0 to -2.7V
12	O2	Logic Output terminal O2
13	NC	No Connect
14	O1	Logic Output terminal O1

TABLE 2: AD5242 PIN Function Descriptions

Pin	Name	Description
1	O1	Logic Output terminal O1
2	A_1	Resistor terminal A_1
3	W_1	Wiper terminal W_1
4	B_1	Resistor terminal B_1
5	V_{DD}	Positive power supply, specified for operation from +2.2 to +5.5V.
6	SHDN	Active Low, Asynchronous connection of the wiper W to terminal B, and open circuit of terminal A. RDAC register contents unchanged.
7	SCL	Serial Clock Input
8	SDA	Serial Data Input/Output
9	AD0	Programmable address bit for multiple package decoding. Bits AD0 & AD1 provide 4 possible addresses.
10	AD1	Programmable address bit for multiple package decoding. Bits AD0 & AD1 provide 4 possible addresses.
11	DGND	Common Ground
12	V_{SS}	Negative power supply, specified for operation from 0 to -2.7V
13	O2	Logic Output terminal O2
14	B_2	Resistor terminal B_2
15	W_2	Wiper terminal W_2
16	A_2	Resistor terminal A_2

PRELIMINARY TECHNICAL DATA

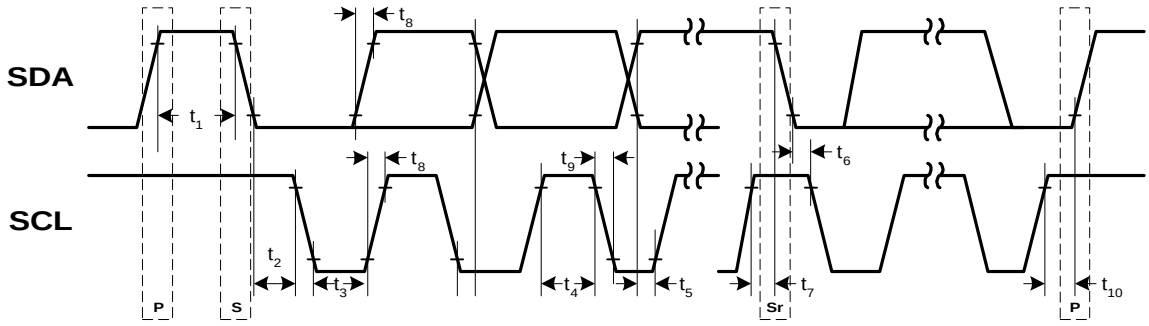

Figure 2. Detail Timing Diagram

The AD5241/AD5242 I²C-bus interface is a receive only slave. Data is accepted from the I²C bus in the following serial format:

S	0	1	0	1	1	AD1	AD0	0	A	A/$\overline{B}$	RS	SD	O2	O1	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

Where:
S = Start Condition
P = Stop Condition
A = Acknowledge
X = Don't Care
AD1, **AD0** = Package pin programmable address bits
A/$\overline{B}$ = RDAC sub address select
RS = Midscale reset
SD = Shutdown, same as $\overline{SHDN}$ pin operation
O2, **O1** = Output logic pin latched values
D7,D6,D5,D4,D3,D2,D1,D0 = Data Bits

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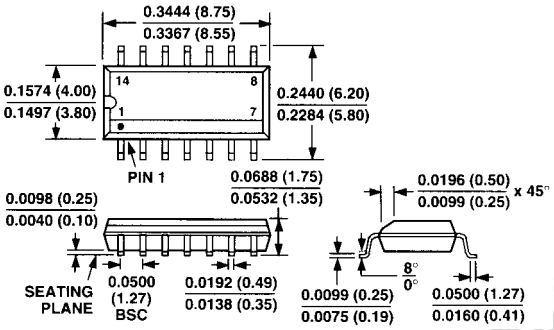
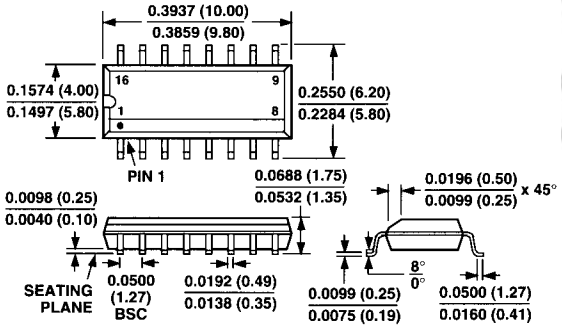
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

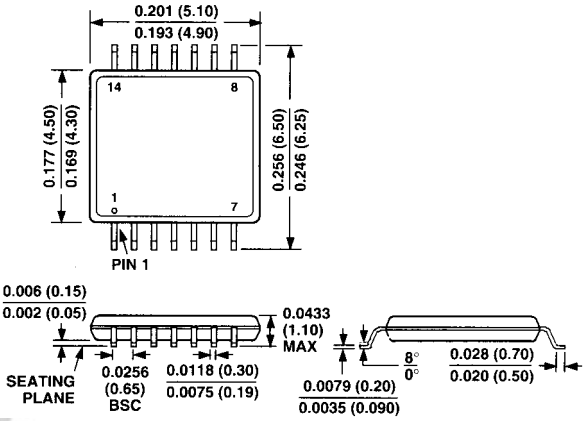
14-Lead Narrow Body SOIC (SO-14)



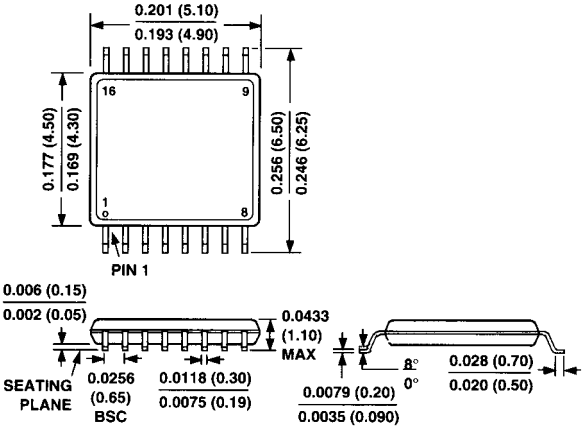
16-Lead Narrow SOIC (R-16N)



14-Lead TSSOP (RU-14)



16-Lead TSSOP (RU-16)



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