ANALOG DEVICES

24-Bit Σ-Δ ADC

PRELIMINARY TECHNICAL DATA AD1555/AD1556

FEATURES:

AD1555
- **4th Order Σ-Δ Modulator**
- **Large Dynamic Range:**
  - **118 dB min, 121 dB typical @ 1 ms**
  - **118 dB typical @ 0.5 ms**
- **Low Distortion: -116 dB max, -120 dB typical**
- **Sampling Rate at 256 kSPS**
- **Very High Jitter Tolerance**
- **No External Anti-Alias Filter Required**
- **Programmable Gain Front End**
- **Input Range: ±2.25 V**
- **Robust Inputs**
- **Gain Settings: 0dB, 12dB, 24dB, 36dB, 48dB**
- **Low input noise: 56nVrms @ 4ms with 48dB gain**
- **Common mode rejection (DC to 1kHz):**
  - **92 dB min, 100 dB typical @ 0 dB Gain**
  - **100 dB min @ other Gains**
- **80 mW Typ Low Power Dissipation**
- **Standby Modes**

AD1556
- **FIR Digital Filter/Decimator**
- **Serial or parallel Selection of Configuration**
- **Output Word Rates: 250 SPS to 16 kSPS**
- **13 mW Typ Low Power Dissipation**
- **5 μW in Standby Mode**

Evaluation Board with Software available

APPLICATIONS
- **Seismic Data Acquisition Systems**

GENERAL DESCRIPTION

The AD1555 is a complete sigma-delta modulator, combined with a programmable gain amplifier intended for low frequency, high dynamic range measurement applications. The AD1555 outputs a ones-density bit stream proportional to the analog input. When used in conjunction with the AD1556 digital filter/decimator, a high performance ADC is realized.

The continuous-time analog modulator input architecture avoids the need for an external anti-alias filter. The programmable gain front end simplifies system design, extends the dynamic range, and reduces system board area. Low operating power and standby modes makes the AD1555 ideal for remote battery-powered data acquisition systems.

The AD1555 is fabricated on Analog Devices BiCMOS process which has high performance bipolar devices along with CMOS transistors. The AD1555 and AD1556 are packaged respectively in 28-Pin PLCC and 44-Pin MQFP packages and are specified from -55°C to +85°C.

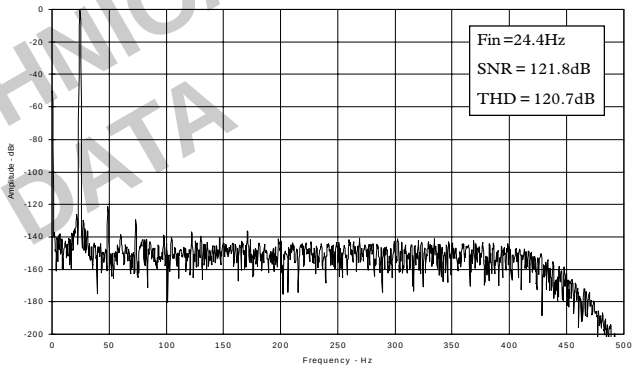
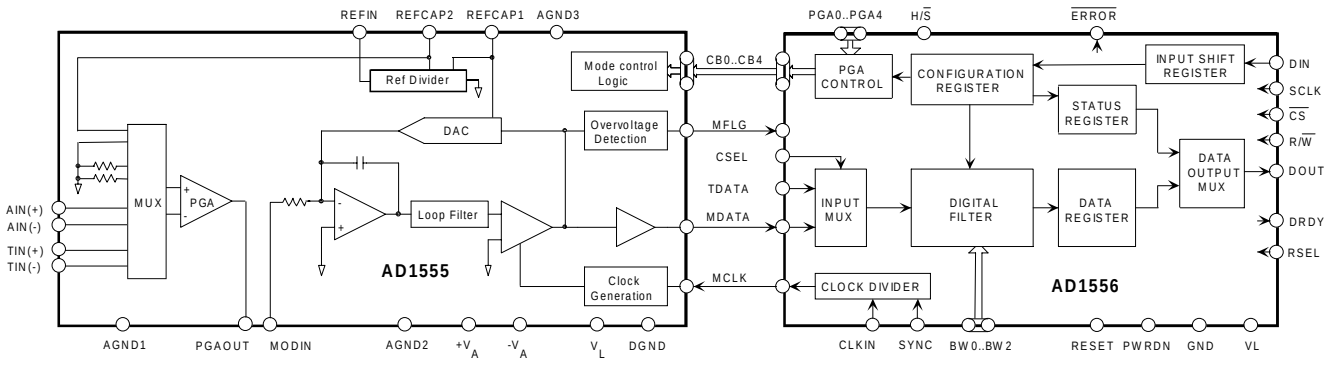


Figure 1. FFT plot, Full Scale AIN Input, 0dB gain.

AD1555/AD1556 FUNCTIONAL BLOCK DIAGRAM



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AD1555-SPECIFICATIONS

($+V_A$= +5 V ± 5%; $-V_A$= -5 V ± 5%; V_L= +3 V to 5.25 V; AGND = DGND = 0 V; MCLK = 256 kHz; $T_A = T_{MIN}$ to T_{MAX}; unless otherwise noted.)

Parameter	Notes	AD1555AP Min	Typ	Max	Units
PGA Gain Settings	0, 12, 24, 36, and 48 dB				
AC ACCURACY					
Dynamic Range					
Modulator only	F_O = 1 kHz[1]	118	121		dB
	other F_O[1]		see Table I		
PGA and Modulator	all PGA Gain settings		see Table I		
Total Harmonic Distortion[2]					
Modulator only			-120	-116	dB
PGA and Modulator			-116	-112	dB
Jitter Tolerance				300	ps
Intermodulation Distortion[3]	PGA Gain = 0 dB		TBD		dB
DC ACCURACY					
Absolute Gain Error[4]					
PGA Gain settings at 0, 12, 24 dB			1	TBD	%
PGA Gain settings at 36, 48 dB				TBD	%
Gain Stability over temperature[4]			±TBD		%
Channel-to-Channel Gain Matching			±TBD		%
Offset[4,5]	all PGA Gain settings	-100	-70	-40	mV
Offset Drift[4,5]			TBD		µV
ANALOG INPUT					
Full-Scale non-differential Input	MODIN			±2.25	V
Full-Scale Differential Input	PGA Gain = 0 dB			±2.25	V
	other PGA Gain settings		see Table I		
Over-Load Recovery Time			TBD		ms
Common Mode Range				±2.25	V
Common Mode Rejection Ratio	V_{CM}= ±2.25V, f_{IN}= 200Hz				
	PGA Gain = 0 dB	92	100		dB
	other PGA Gain settings	100			dB
Power Supply Rejection Ratio[6]		TBD			dB
AIN to TIN crosstalk isolation	f_{IN}= 200Hz	130			dB
REFERENCE INPUT[7]					
input voltage range		2.990	3.0	3.010	V
input current			130		µA
DIGITAL INPUTS OUTPUTS					
V_{IL}		-0.3		+0.8	V
V_{IH}		+2.0		V_L+0.3	V
I_{IL}		-10		+10	µA
I_{IH}		-10		+10	µA
V_{OL}	I_{sink} = 1.6 mA			+0.4	V
V_{OH}	I_{source} = 500 µA	VL-0.6			V

NOTES
1. Fo is the AD1556 Output Word Rate, the inverse of the sampling rate.
2. Tested with a full scale input signal at approximately 24 Hz.
3. Tested at the output word rate F_O =1 kHz with input signals of 30Hz and 50Hz, each 6dB down full scale.
4. This specification is for the AD1555 only and does not include the errors from external components as, for instance, the external reference.
5. This offset specification is refer to the modulator output.
6. Characterized with a 100mVpp sine wave applied separately to each supply.
7. Recommended Reference: AD780BR.

Specifications subject to change without notice.

AD1555-SPECIFICATIONS

($+V_A$= +5 V ± 5%; $-V_A$= -5 V ± 5%; V_L= +3 V to 5.25 V; AGND = DGND = 0 V; MCLK = 256 kHz; $T_A = T_{MIN}$ to T_{MAX}; unless otherwise noted.)

Parameter	Notes	AD1555AP Min	Typ	Max	Units
POWER SUPPLIES					
Specified Performance					
$+V_A$		4.75	5	5.25	V
$-V_A$		-5.25	-5	-4.75	V
V_L		3		5.25	V
Quiescent Currents[8]					
$I(+V_A)$			8	9.6	mA
$I(-V_A)$			8	9.6	mA
$I(V_L)$			30	42	µA
Power Dissipation[8]					
			80	97	mW
	PGA in standby mode[9]		60	68	mW
	In power-down mode[9,10]:				
	Reference input = 3V		650	850	µW
	Reference input = 0V		250	350	µW
TEMPERATURE RANGE[11]					
Specified Performance, T_{MIN} to T_{MAX}		-55		85	°C

TABLE I. DYNAMIC AND NOISE TYPICAL PERFORMANCES

INPUT and Gain	MODIN	PGA 0dB	PGA 12dB	PGA 24dB	PGA 36dB	PGA 48dB
Input Range	1.6Vrms	1.6Vrms	400mVrms	100mVrms	25mVrms	6.5mVrms
Dynamic Range						
F_O = 16 kHz (1/16ms)	TBD	TBD	TBD	TBD	TBD	TBD
F_O = 8 kHz (1/8ms)	TBD	TBD	TBD	TBD	TBD	TBD
F_O = 4 kHz (1/4ms)	105.5dB	105.5dB	105.5dB	105dB	99dB	89dB
F_O = 2 kHz (1/2ms)	118dB	118dB	117.5dB	113dB	102dB	92dB
F_O = 1 kHz (1ms)	121dB	121dB	120.5dB	116dB	105dB	95dB
F_O = 500 Hz (2ms)	124dB	124dB	123.5dB	119dB	108dB	98dB
F_O = 250Hz (4ms)	127dB	127dB	126.5dB	122dB	111dB	101dB
Equivalent input noise						
F_O = 16 kHz (1/16ms)	TBD	TBD	TBD	TBD	TBD	TBD
F_O = 8 kHz (1/8ms)	TBD	TBD	TBD	TBD	TBD	TBD
F_O = 4 kHz (1/4ms)	8.5µVrms	8.5µVrms	2.1µVrms	562nVrms	281nVrms	222nVrms
F_O = 2 kHz (1/2ms)	2.0µVrms	2.0µVrms	533nVrms	224nVrms	199nVrms	157nVrms
F_O = 1 kHz (1ms)	1.4µVrms	1.4µVrms	378nVrms	158nVrms	141nVrms	111nVrms
F_O = 500 Hz (2ms)	1.0µVrms	1.0µVrms	267nVrms	112nVrms	100nVrms	79nVrms
F_O = 250Hz (4ms)	715nVrms	715nVrms	189nVrms	79nVrms	70nVrms	56nVrms

NOTES
8. Specified with $+V_A$=+5V, $-V_A$=-5V, V_L=+3.3V and with analog inputs grounded.
9. See Table III for configuration conditions.
10. Specified with $+V_A$=+5V, $-V_A$=-5V, V_L=+3.3V and MCLK input grounded.
11. Contact factory for extended temperature range.

Specifications subject to change without notice.

AD1556-SPECIFICATIONS

(V_L= +3 V to 5.25 V; MCLKIN = 1.024 MHz; $T_A = T_{MIN}$ to T_{MAX}; unless otherwise noted.)

Parameter	Notes	AD1556AS Min	Typ	Max	Units
FILTER PERFORMANCES					
Passband Ripple		-0.05		+0.05	dB
Stopband attenuation	all filters except F_0=16kHz			-135	dB
Stopband attenuation	F_0=16kHz			-86	dB
Filters characteristics			see Table II		
DIGITAL INPUTS OUTPUTS					
V_{IL}		-0.3		+0.8	V
V_{IH}		+2.0		V_L+0.3	V
I_{IL}		-10		+10	µA
I_{IH}		-10		+10	µA
V_{OL}	I_{sink} = 4 mA			+0.5	V
V_{OH}	I_{source} = 4 mA	V_L-0.6			V
POWER SUPPLIES					
Specified Performance					
V_L		3		5.25	V
Quiescent Currents					
$I(V_L)$			4	TBD	mA
Power Dissipation					
	V_L = 3.3V, F_0=500Hz		13		mW
	In power-down mode		TBD		µW
TEMPERATURE RANGE[12]					
Specified Performance, T_{MIN} to T_{MAX}		-55		85	°C

TABLE II. FILTER CHARACTERISTICS

OUTPUT WORD RATE F_o (Sampling Rate in ms)	PASSBAND (Hz)	-3 dB Freq. (Hz)	STOP-BAND (Hz)	GROUP DELAY (ms)
16000 Hz (1/16 ms)	6000	6480	8000	0.984
8000 Hz (1/8 ms)	3000	3267.5	4000	3
4000 Hz (1/4 ms)	1500	1634	2000	6
2000 Hz (1/2 ms)	750	816.9	1000	12
1000 Hz (1 ms)	375	408.5	500	24
500 Hz (2 ms)	187.5	204.2	250	48
250 Hz (4 ms)	93.75	101.4	125	93

NOTES
12. Contact factory for extended temperature range.

Specifications subject to change without notice.

TIMING SPECIFICATIONS

($+V_A$= +5 V ± 5%; $-V_A$= -5 V ± 5%; V_L=+5 V ± 5%; AGND=DGND = 0 V; C_L = 50 pF $T_A = T_{MIN}$ to T_{MAX}; unless otherwise noted.)

	Symbol	Min	Typ	Max	Units
CLKIN Frequency	F_{CLKIN}	TBD	1.024	TBD	MHz
CLKIN Period (t_{CLKIN} = 1/F_{CLK})	t_{CLKIN}				ns
CLKIN Duty Cycle Error		45		55	%
MCLK output Frequency			F_{CLKIN}/4		
SYNC Setup Time	t_1	10			ns
SYNC Hold Time	t_2	10			ns
CLKIN rising to MCLK output falling on SYNC	t_3			20	ns
CLKIN falling to MCLK output rising	t_4			20	ns
CLKIN falling to MCLK output falling	t_5			20	ns
MCLK input falling to MDATA falling	t_6			30	ns
MCLK input rising to MDATA and MFLG valid	t_7			100	ns
TDATA Setup Time after SYNC	t_8	5			ns
TDATA Hold Time	t_9	5			ns
RESET Setup Time	t_{10}	15			ns
RESET Hold Time	t_{11}	15			ns
CLKIN falling to DRDY rising	t_{12}			20	ns
CLKIN rising to DRDY falling*	t_{13}			20	ns
CLKIN rising to $\overline{\text{ERROR}}$ falling	t_{14}			50	ns
RSEL to Data Valid	t_{15}			25	ns
RSEL Setup to SCLK falling	t_{16}	10			ns
DRDY to Data Valid	t_{17}			25	ns
DRDY High Setup to SCLK falling	t_{18}	10			ns
R/$\overline{W}$ to Data Valid	t_{19}			25	ns
R/$\overline{W}$ High Setup to SCLK falling	t_{20}	10			ns
$\overline{CS}$ to Data Valid	t_{21}			25	ns
$\overline{CS}$ Low Setup to SCLK falling	t_{22}	10			ns
SCLK rising to DOUT Valid	t_{23}			25	ns
SCLK High Pulse Width	t_{24}	25			ns
SCLK Low Pulse Width	t_{25}	25			ns
SCLK Period	t_{26}	50			ns
SCLK falling to DRDY falling*	t_{27}			20	ns
$\overline{CS}$ high or R/$\overline{W}$ low to DOUT Hi-Z	t_{28}			20	ns
R/$\overline{W}$ Low Setup to SCLK falling	t_{29}	10			ns
$\overline{CS}$ Low Setup to SCLK falling	t_{30}	10			ns
Data Setup Time to SCLK falling	t_{31}	10			ns
Data Hold Time after SCLK falling	t_{32}	10			ns
R/$\overline{W}$ Hold Time after SCLK falling	t_{33}	10			ns

* with DRDYBUF low only. When DRDYBUF is high, this timing also depends on the value of the external pull-down resistor.

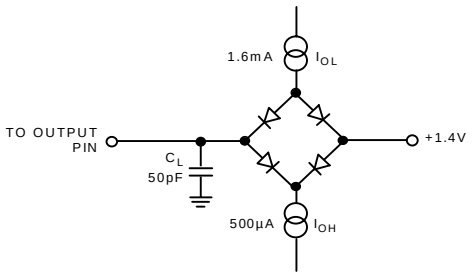


Figure 2. Load Circuit for Digital Interface Timing.

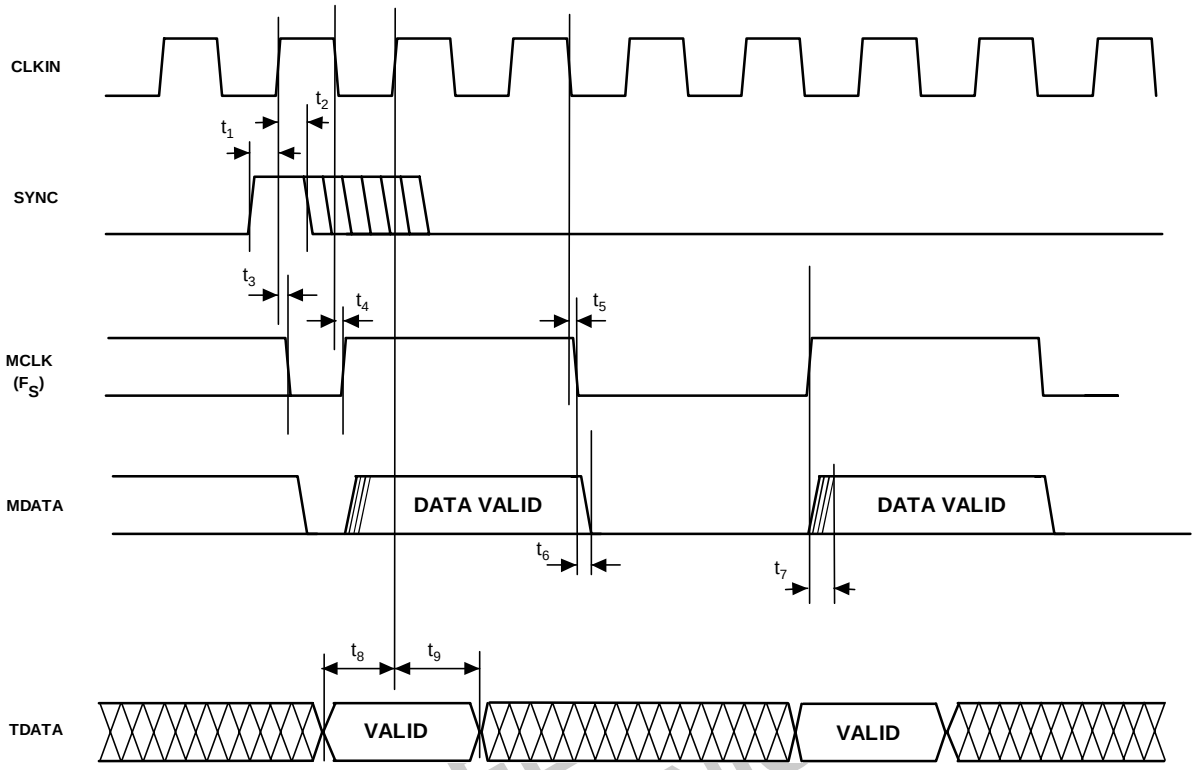


Figure 3. AD1555/AD1556 Interface Timing

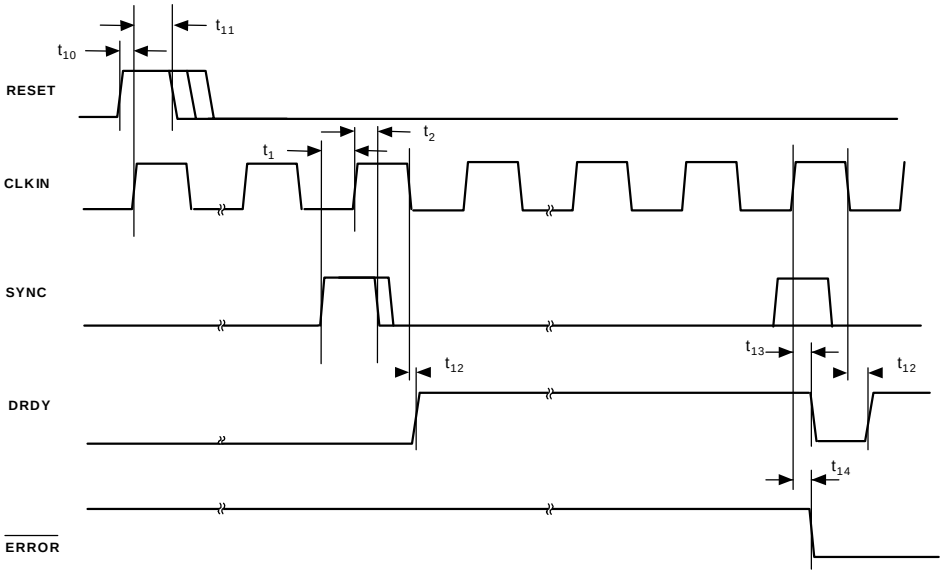


Figure 4. AD1556 RESET, DRDY and Overwrite Timings

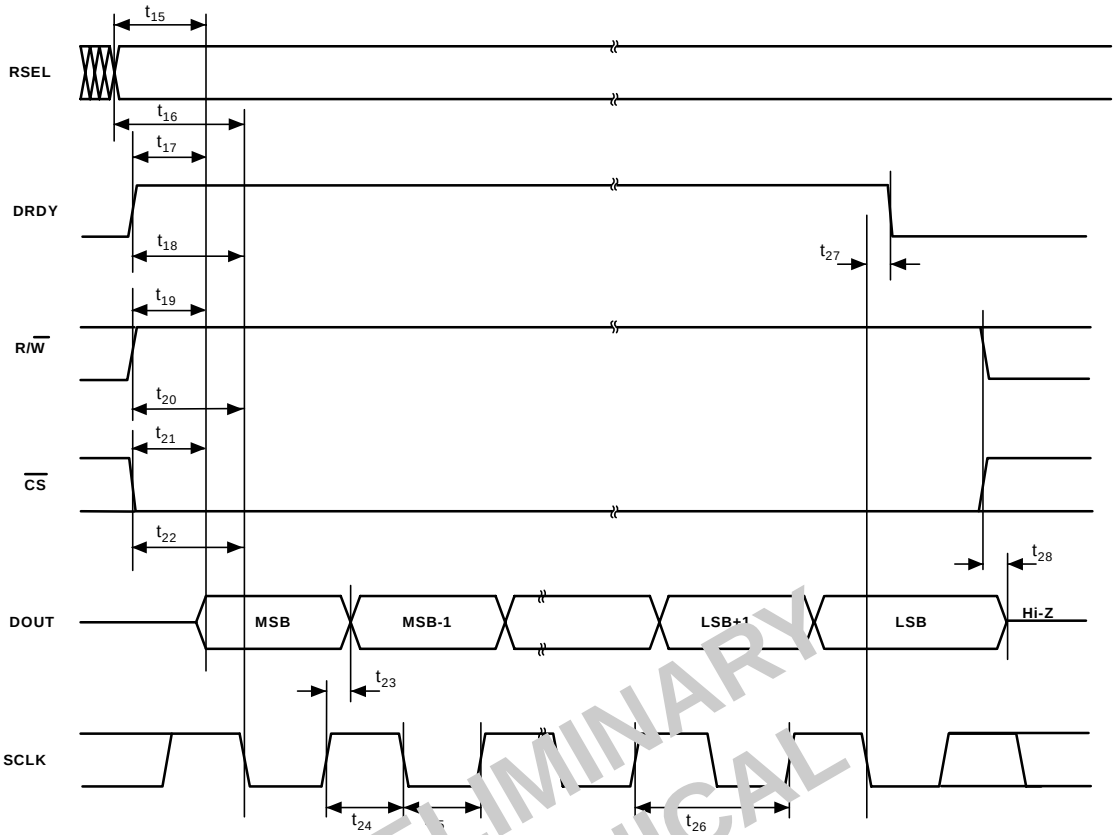


Figure 5. Serial Read Timing.

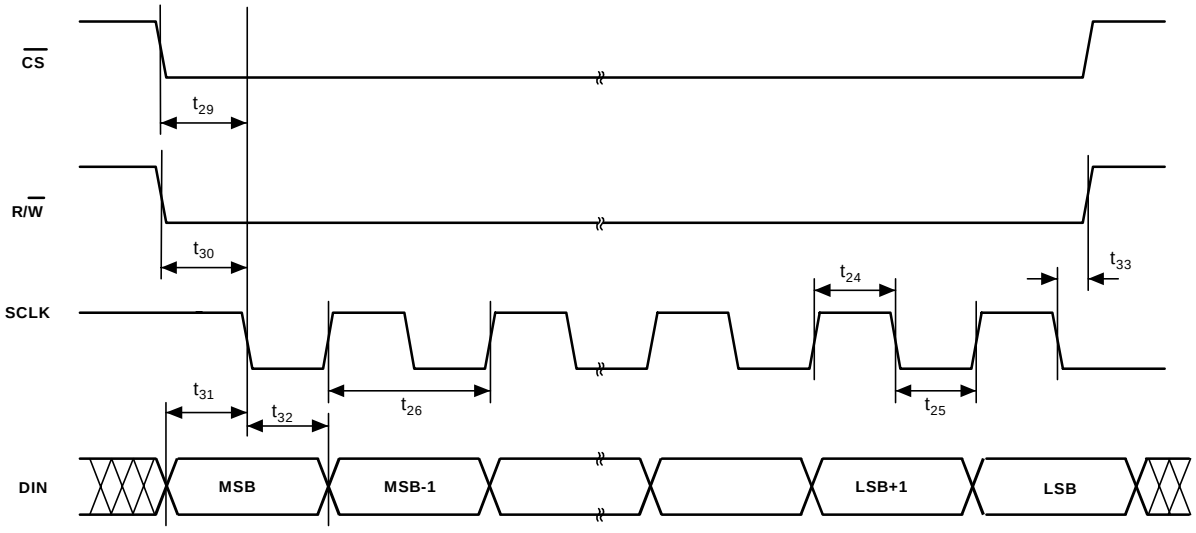


Figure 6. Serial Write Timing

ABSOLUTE MAXIMUM RATINGS[1]

Analog Inputs
Pins 7, 8, 23, 24, 25, 28 ..... $-V_A - 0.3V$ to $+V_A + 0.3V$
AIN(+), AIN(-) DC input current ..... TBD mA
AIN(+), AIN(-) 2μs pulse input current ..... TBD mA
Supply Voltages
$+V_A$ to $-V_A$ ..... –0.3V to 14 V
$+V_A$ to AGND ..... –0.3V to +7 V
$-V_A$ to AGND ..... –7V to +0.3 V
V_L to DGND ..... –0.3V to +7 V
Ground Voltage Differences
DGND, AGND1, AGND2, AGND3 ..... ±0.3 V
Digital Inputs ..... –0.3 V to V_L+0.3 V
Internal Power Dissipation[2]
AD1555 ..... TBD mW
AD1556 ..... TBD mW
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature Range
(Soldering 10 sec) ..... +300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
28-PIN PLCC: θ_{JA} = 80°C/Watt, θ_{JC} = 37°C/Watt
44-PIN MQFP: θ_{JA} = TBD°C/Watt, θ_{JC} = TBD°C/Watt

ORDERING GUIDE

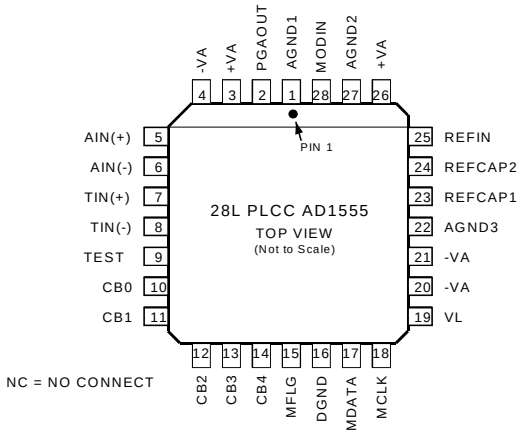
Model	Temperature Range*	Package Option
AD1555AP	-55°C to +85°C	P-28A
AD1556AS	-55°C to +85°C	S-44
EVAL-AD1555/56EB		Evaluation board

** Contact factory for extended temperature range*

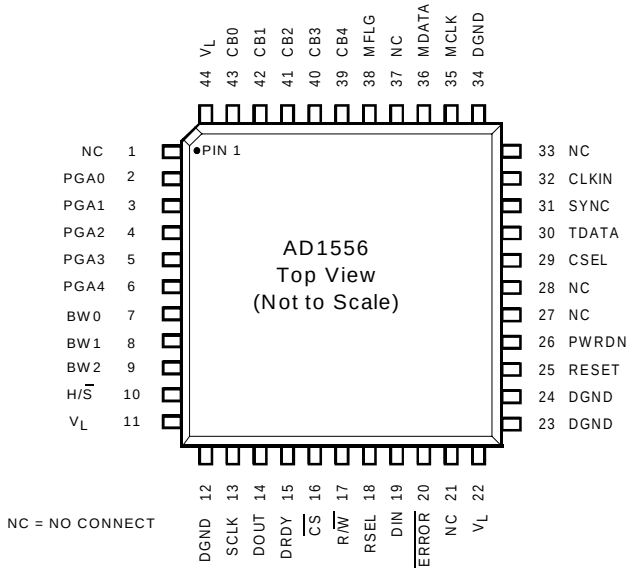
CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1555/AD1556 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

28-PIN PLCC
(P-28A)



44-PIN MQFP
(S-44)



AD1555 PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	DESCRIPTION
5	AIN(+)	Mux Input. Noninverting signal to the PGA mux input. Refer to table III for input selection.
6	AIN(-)	Mux Input. Inverting signal to the PGA mux input. Refer to table III for input selection.
7	TIN(+)	Mux Input. Noninverting test signal to the PGA mux input. Refer to table III for input selection.
8	TIN(-)	Mux Input. Inverting test signal to the PGA mux input. Refer to table III for input selection.
2	PGAOUT	Programmable Gain Amplifier Output. The output of the on-chip programmable gain amplifier is available at this pin. Refer to table III for PGA gain settings selection.
28	MODIN	Modulator Input. Analog input to the modulator. Normally, this input is directly tied to PGAOUT output.
17	MDATA	Modulator Output. The bitstream generated by the modulator is output in a Return-to-Zero data format. The data is valid for approximately one-half a MCLK cycle. Refer to Figure 3.
15	MFLG	Modulator Error. Digital output which set high if an over-range condition occurs in the modulator.
18	MCLK	Clock Input. The clock input signal, nominally 256 kHz, provides the necessary clock for the Σ-Δ modulator. When this input is static, AD1555 is in power-down mode.
10-14	CB0-CB4	Modulator Control. These input pins control the mux selection, the PGA gain settings and the stand-by modes of the AD1555. When used with the AD1556, these pins are generally directly tied to CB0-CB4 output pins of the AD1556. CB0-2 are generally used to set the PGA gain or cause it to enter in the PGA standby mode (Refer to Table III). CB3 and CB4 select the MUX input voltage applied to the PGA as described in Table III.
25	REFIN	Reference Input. This input accepts a 3 V level that is internally divided to provide the reference for the Σ-Δ modulator.
24	REFCAP2	Reference Filter. The reference input is internally divided and available at this pin.
23	REFCAP1	DAC Reference Filter. The reference input is internally divided and available at this pin to provide the reference for the Σ-Δ modulator. Connect an external 22μF (5V min) tantalum capacitor from REFCAP1 to AGND3 to filter the external reference noise.
9	Test	Test pin for factory use only. This pin must be kept not connected for normal operation.
3,26	$+V_A$	Positive Analog Supply voltage. +5 V nominal.
4,20,21	$-V_A$	Negative Analog Supply voltage. -5 V nominal.
1	AGND1	Analog Ground.
27	AGND2	Analog Ground.
22	AGND3	Analog Ground. Used as the ground reference for the REFIN pin.
19	V_L	Positive Digital Supply voltage. +3.3V or +5 V nominal.
16	DGND	Digital Ground.

AD1556 PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	DESCRIPTION
36	MDATA	Modulator Data. This input receives the ones-density bit stream from the AD1555 for input to the digital filter.
30	TDATA	Test Data. Input to digital filter for user test data.
29	CSEL	Filter Input Select. Selects the source for input to the digital filter. A logic high selects the TDATA input, a low selects MDATA as the filter input.
35	MFLG	Modulator Error. The MFLG input is used to detect if an over-range condition occurred in the modulator. Its logic level is sensed on the rising edge of CLKIN. When over-range condition detected, $\overline{\text{ERROR}}$ goes low and updates the status register.
32	CLKIN	Clock Input. The clock input signal, nominally 1.024 MHz, provides the necessary clock for the AD1556. This clock frequency is divided by four to generate the MCLK signal for the AD1555.
35	MCLK	Modulator Clock. Provides the modulator sampling clock frequency. The modulator always samples at one-fourth the CLKIN frequency.
31	SYNC	Synchronization Input. The SYNC input clears the AD1556 filter in order to synchronize the start of the filter convolutions. The SYNC event is initiated on the first CLKIN rising edge after the SYNC pin goes high. The SYNC input can also be applied synchronously to the AD1556 decimation rate without resetting the convolution cycles.

AD1556 PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	DESCRIPTION
25	RESET	Filter Reset. A logic high input clears any error condition in the status register, and sets the configuration register to the state of the corresponding hardware pins. On power-up this reset state is entered.
26	PWRDN	Power Down Hardware Control. A logic high input powers down the filter. The convolution cycles in the digital filter and the MCLK signal are stopped. All registers retain their data and the serial data interface remains active. The power-down mode is entered on the first falling edge of CLKIN after PWRDN is taken high. When exiting the power down mode a SYNC must be applied to resume filter convolutions.
16	$\overline{CS}$	Chip Select. When set low the serial data interface pins DIN, DOUT, R/$\overline{W}$, and SCLK are active; a logic high disables these pins and sets the DOUT pin to Hi-Z.
17	R/$\overline{W}$	Read/Write. A read operation is initiated if R/$\overline{W}$ is high and $\overline{CS}$ is low. A low sets the DOUT pin to Hi-Z and allows a write operation to the device via the DIN pin.
13	SCLK	Serial Data Clock. Synchronizes data transfer to either write data on the DIN input pin or read data on the DOUT output pin.
19	DIN	Serial Data Input. Used during a write operation. Loads the Configuration Register via the Input Shift Register. Data is loaded MSB first and must be valid on the falling edge of SCLK.
15	DRDY	Data ready. A logic high output indicates that data is ready to be accessed from the Output Data Register. DRDY goes low once a read operation is complete. When selected, the DRDY output pin has a type buffer that allows wired-OR connection of multiple AD1556s.
14	DOUT	Serial Data Output. DOUT is used to access the conversion results or the contents of the Status Register, depending on the logic state of the RSEL pin. At the beginning of a read operation the first data bit is output (MSB first). The data changes on the rising edge of SCLK and is valid on the SCLK falling edge.
18	RSEL	Register Select. When set high, the Conversion Data Register contents are output on a read operation. A low selects the Status Register.
20	$\overline{ERROR}$	Error flag. A logic low output indicates an error condition occurred in the modulator or digital filter. When $\overline{ERROR}$ goes low the ERROR bit in the status register is set high. The $\overline{ERROR}$ output pin has an open drain type buffer with an internal 100 kΩ typical pull-up that allows wired-OR connection of multiple AD1556s.
10	H/$\overline{S}$	Hardware/Software Mode Select. Determines how the device operation is controlled. In hardware mode, H/$\overline{S}$ is high, the state of hardware pins set the mode of operation. When H/$\overline{S}$ is low, a write sequence to the Configuration Register or a previous write sequence sets the device operation.
7-9	BW0-BW2	Output Rate Control Inputs. Sets the digital filter decimation rate and the state of the corresponding bit in the configuration register upon RESET or when in hardware mode. Refer to the Filter Specifications and Table VI.
2-6	PGA0-4	PGA and MUX Control Inputs. Sets the logic level of CB0-CB4 output pins respectively and the state of the corresponding bit in the configuration register upon RESET or when in hardware mode. Refer to Table III.
43-39	CB0-CB4	Modulator Control. These output control pins represent a portion of the data loaded into the AD1556 Configuration Register. CB0-2 are generally used to set the PGA gain or cause it to enter in the PGA standby mode (Refer to Table III). CB3 and CB4 select the MUX input voltage applied to the PGA as described in Table III.
11,22, 44	V_L	Positive Digital Supply voltage. +3.3V or +5 V nominal.
12,23, 24,34	DGND	Digital Ground.

TERMINOLOGY

DYNAMIC RANGE

Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs grounded in the bandwidth from 1Hz to the Nyquist frequency $F_0/2$. The value for dynamic range is expressed in decibels.

SIGNAL TO NOISE RATIO (SNR)

SNR is the ratio of the rms value of the full scale signal to the total rms noise in the bandwidth from 1Hz to the Nyquist frequency $F_0/2$. The value for SNR is expressed in decibels.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of all the harmonic components up to Nyquist frequency $F_0/2$ to the rms value of a full-scale input signal. The value for THD is expressed in decibels.

INTERMODULATION DISTORTION (IMD)

IMD is the ratio of the rms sum of 2 sine wave signals of 30 Hz and 50Hz which are each 6 dB down from full scale to the rms sum of all intermodulation components within the bandwidth from 1Hz to the Nyquist frequency $F_0/2$. The value for IMD is expressed in decibels.

OFFSET

The offset is the difference between the ideal midscale input voltage (0V) and the actual voltage producing the midscale output code (code 000000H) at the output of the AD1556. The offset specification is refer to the output. This offset is intentionally set at a nominal value of -70mV (see text sigma-delta modulator description). The value for offset is expressed in mV.

OFFSET ERROR DRIFT

The change of the offset over temperature. It is expressed in μV.

GAIN ERROR

The Gain Error is the ratio of the difference between the actual gain and the ideal gain to the ideal gain. The actual gain is the ratio of the output difference obtained with a full-scale analog input (±2.25V) to the full-scale span (4.5V) after correction of the effects of the external components. It is expressed in %.

GAIN ERROR STABILITY over TEMPERATURE

The change of the Gain Error over temperature. It is expressed in %.

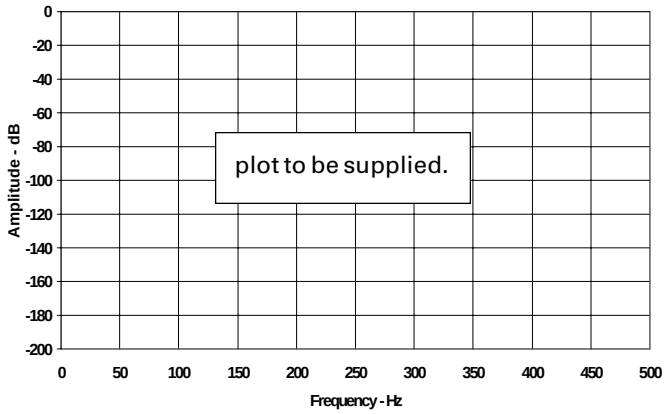


Figure 7. FFT(xxxx points) Full-scale AIN input, 0dB gain.

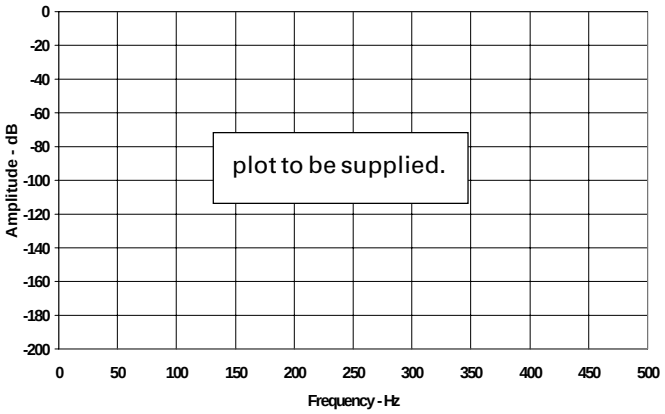


Figure 8. FFT(xxxx points) Full-scale MODIN input.

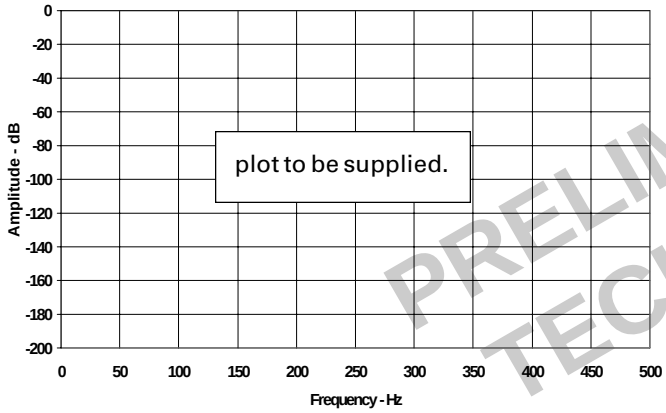


Figure 9. FFT(xxxx points) Full-scale AIN input, 24dB gain.

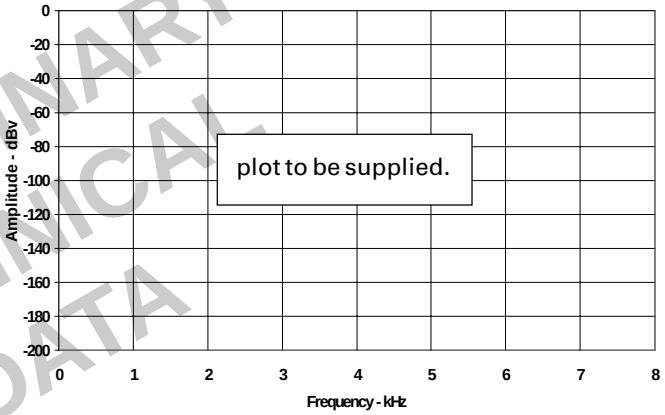


Figure 10. FFT(xxxx points) Full-scale AIN input, 0dB gain.

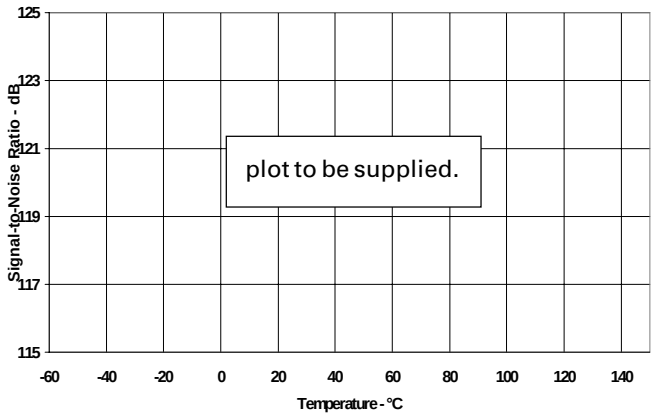


Figure 11. Dynamic Range Vs. Temperature.

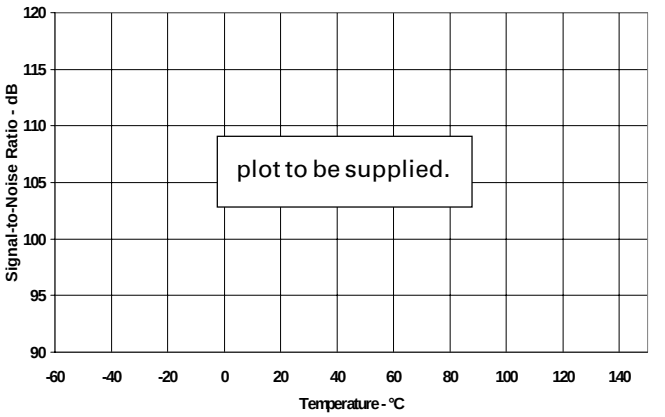


Figure 12. Dynamic Range Vs. Temperature.

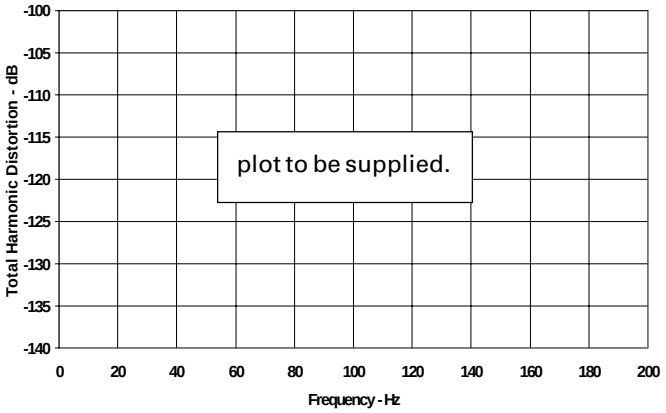


Figure 13. Total Harmonic Distortion Vs. frequency.

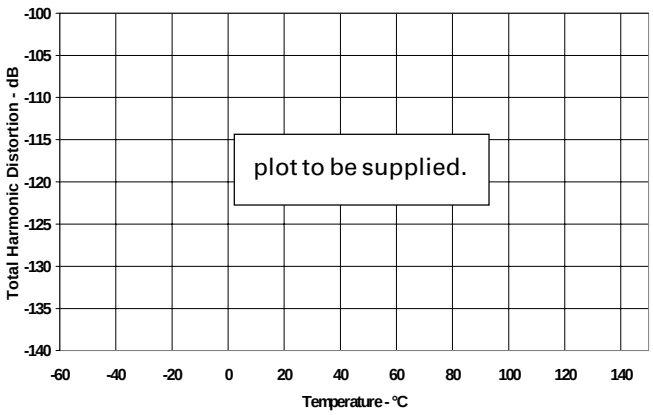


Figure 14. Total Harmonic Distortion Vs. Temperature.

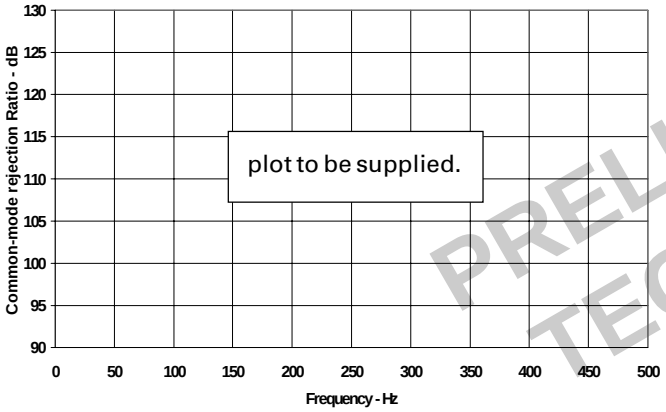


Figure 15. Common-mode rejection Vs. Frequency.

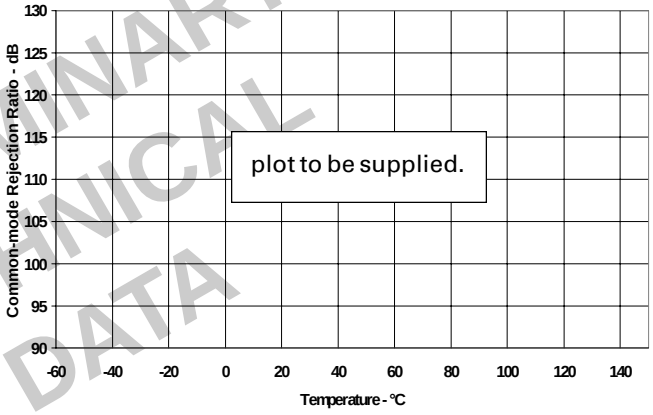


Figure 16. Common-mode rejection Vs. Temperature.

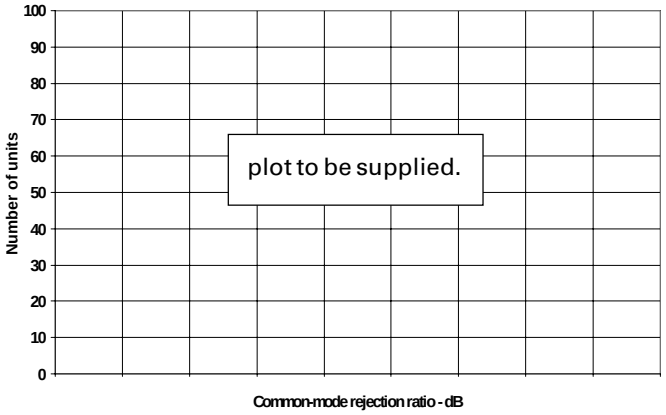


Figure 17. Common-mode rejection Distribution.

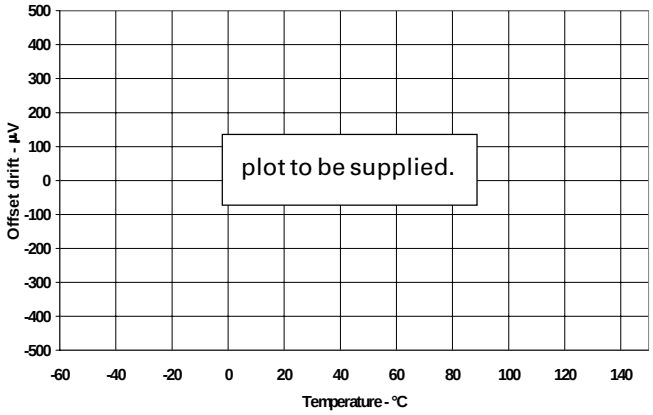


Figure 18. Offset drift.

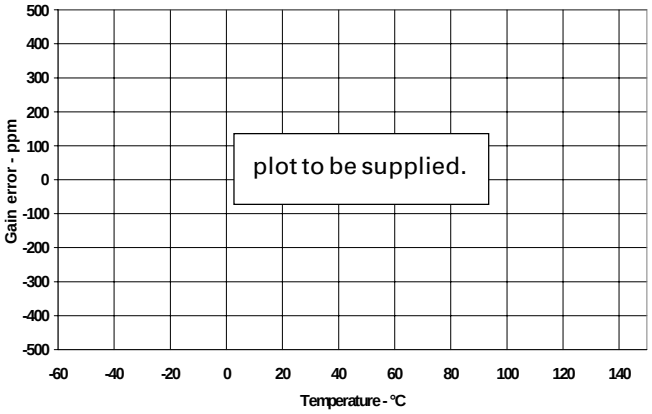


Figure 19. Gain Error Vs. Temperature.

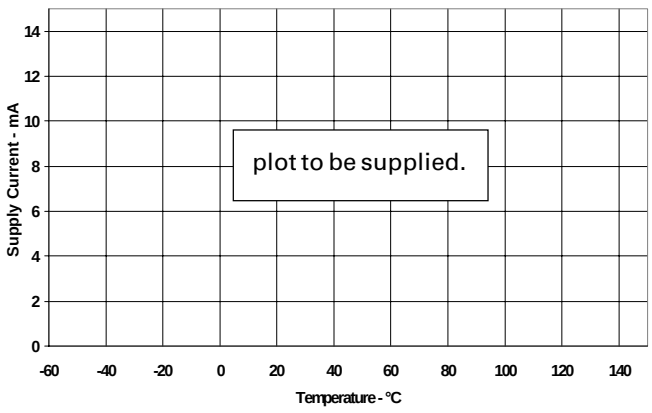


Figure 20. Supply Current Vs. Temperature.

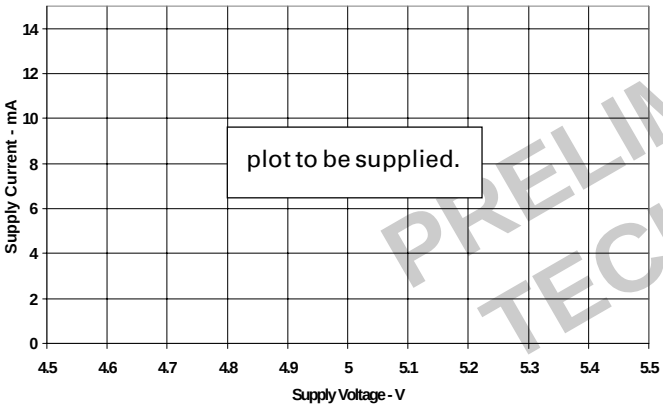


Figure 21. Supply Current Vs. Supply Voltage.

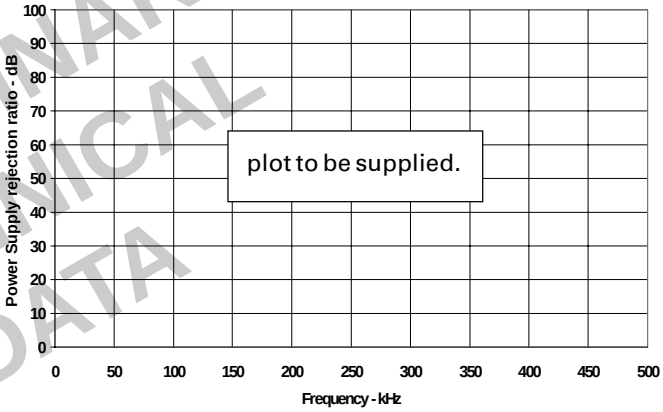


Figure 22. Power Supply Rejection Ratio Vs. Frequency.

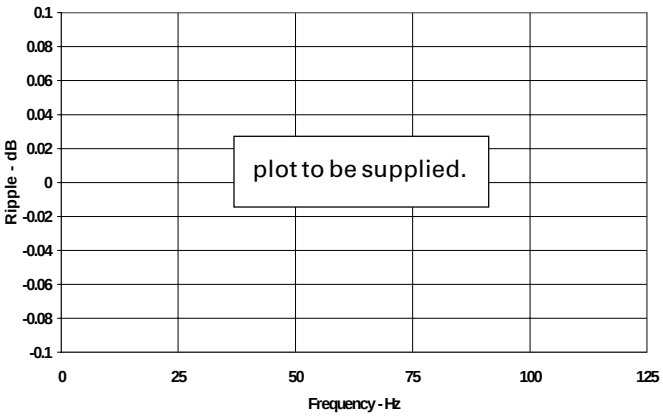


Figure 23. AD1556 Passband Ripple. F_0 = 250 Hz (4 ms).

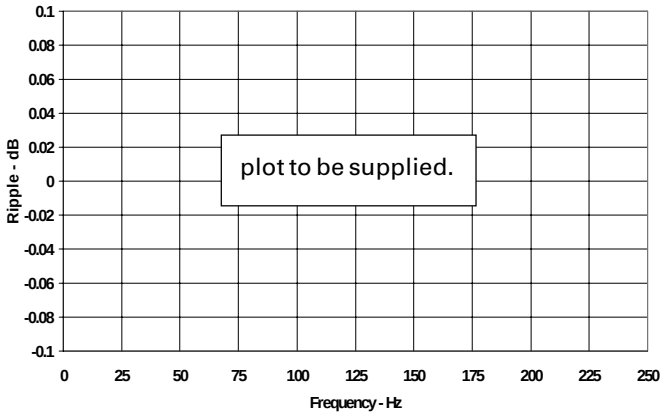


Figure 24. AD1556 Passband Ripple. F_0 = 500 Hz (2 ms).

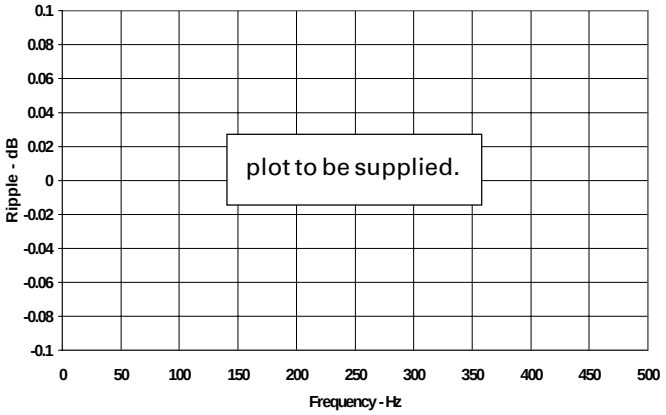


Figure 25. AD1556 Passband Ripple. F_0 = 1 kHz (1 ms).

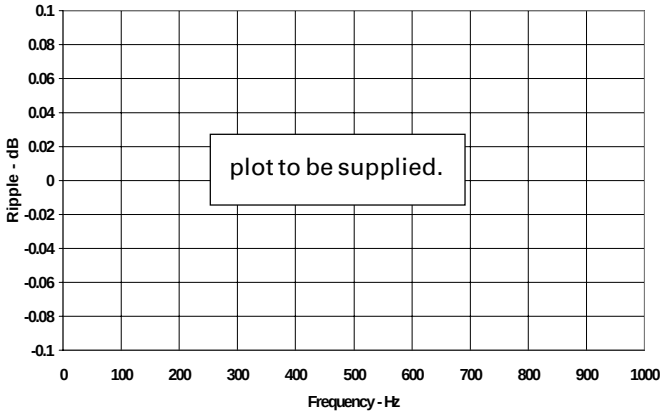


Figure 26. AD1556 Passband Ripple. F_0 = 2 kHz (1/2 ms).

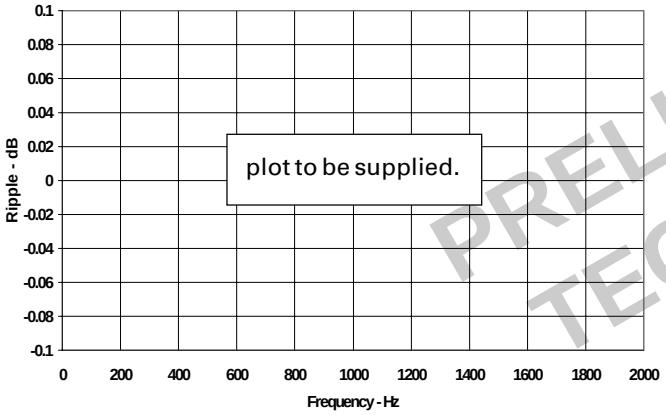


Figure 27. AD1556 Passband Ripple. F_0 = 4 kHz (1/4 ms).

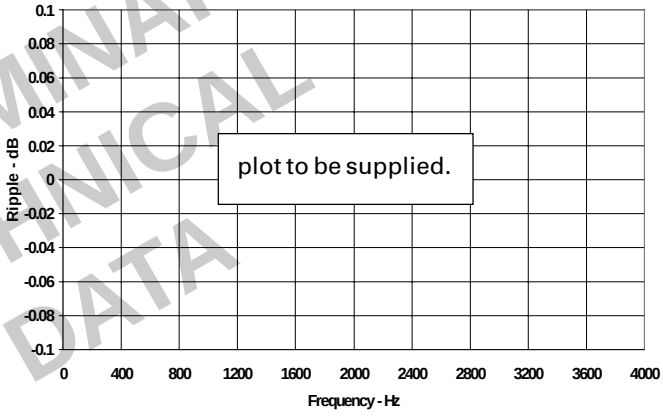


Figure 28. AD1556 Passband Ripple. F_0 = 8 kHz (1/8 ms).

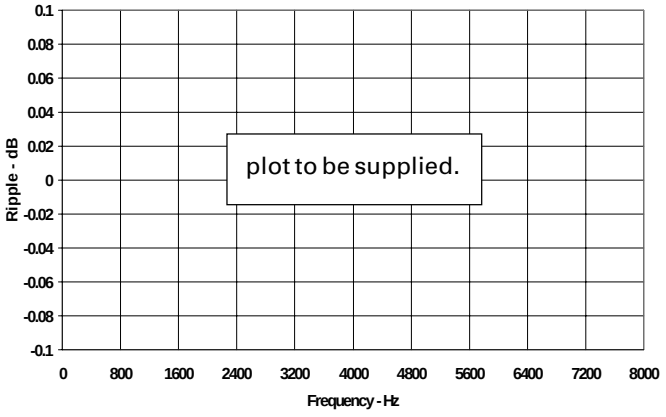


Figure 29. AD1556 Passband Ripple. F_0 =16kHz (1/16 ms).

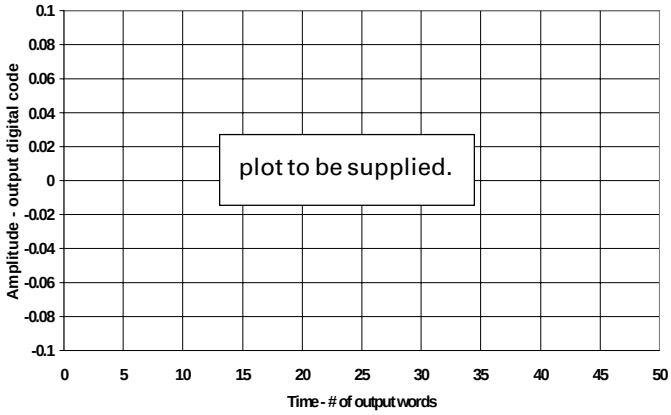


Figure 30. AD1556 Impulse response. F_0 = 1 kHz (1 ms).

CIRCUIT DESCRIPTION

The AD1555-AD1556 chipset is a complete sigma-delta 24 bit A/D converter with very high dynamic range intended for the measurement of low frequency signals up to a few kHz such as, for instance, those in seismic applications.

The AD1555 contains an analog multiplexer, a fully-differential programmable gain amplifier and a fourth order sigma-delta modulator. The analog multiplexer allows selection of one fully-differential input from 2 different external inputs, an internal ground reference or an internal fullscale voltage reference. The fully-differential programmable gain amplifier (PGA) has 5 gain settings 0dB, 12dB, 24dB, 36dB and 48dB which allow the part to handle a total of five different input ranges 1.6Vrms, 400mVrms, 100mVrms, 25mVrms and 6.5mVrms which are programmed via digital input pins (CB0 to CB4). The modulator which operates nominally at a sampling frequency of 256kHz, outputs a bitstream whose ones-density is proportional to its input voltage. This bitstream can be filtered using the AD1556, which is a digital finite impulse low-pass filter (FIR). The AD1556 outputs the data in a 24-bit word over a serial interface. The cutoff frequency and output rate of this filter can be programmed via an on-chip register or by hardware through digital input pins. The dynamic performance and the equivalent input noise vary with gain and output rate as shown in Table I. The use of the different PGA gain settings allows enhancement of the total system dynamic range up to 149dB (gain of 48dB and F_0 = 250Hz).

The AD1555 operates from a dual analog supply (±5V), while the AD1556 and the digital part of the AD1555 operate from a single +3.3V or +5V supply. Each device exhibits low power dissipation and can be configured for standby mode.

The Figure 31 illustrates a typical operating circuit.

MULTIPLEXER and PROGRAMMABLE GAIN AMPLIFIER (PGA)

Analog Inputs

The AD1555 has two sets of fully-differential inputs AIN and TIN. The common-mode rejection capability of these inputs generally surpasses the performance of conventional programmable gain amplifiers. The very high input impedance, typically higher than 100MΩ, allows direct connection of the sensor to the AD1555 inputs, even through serial resistances. Figure 31 illustrates such a configuration. The passive filter between the sensor and the AD1555 is shown here as an example. Other filter structures could be used depending on the specific requirements of the application. Also, the Johnson noise ($\sqrt{4kTRB}$) of the serial resistance should be taken into consideration. For instance, a 1kΩ serial resistance reduces by approximately 1.8dB the dynamic performance of a system using a gain setting of 48 dB at an output word rate F_0 = 500 Hz. For applications

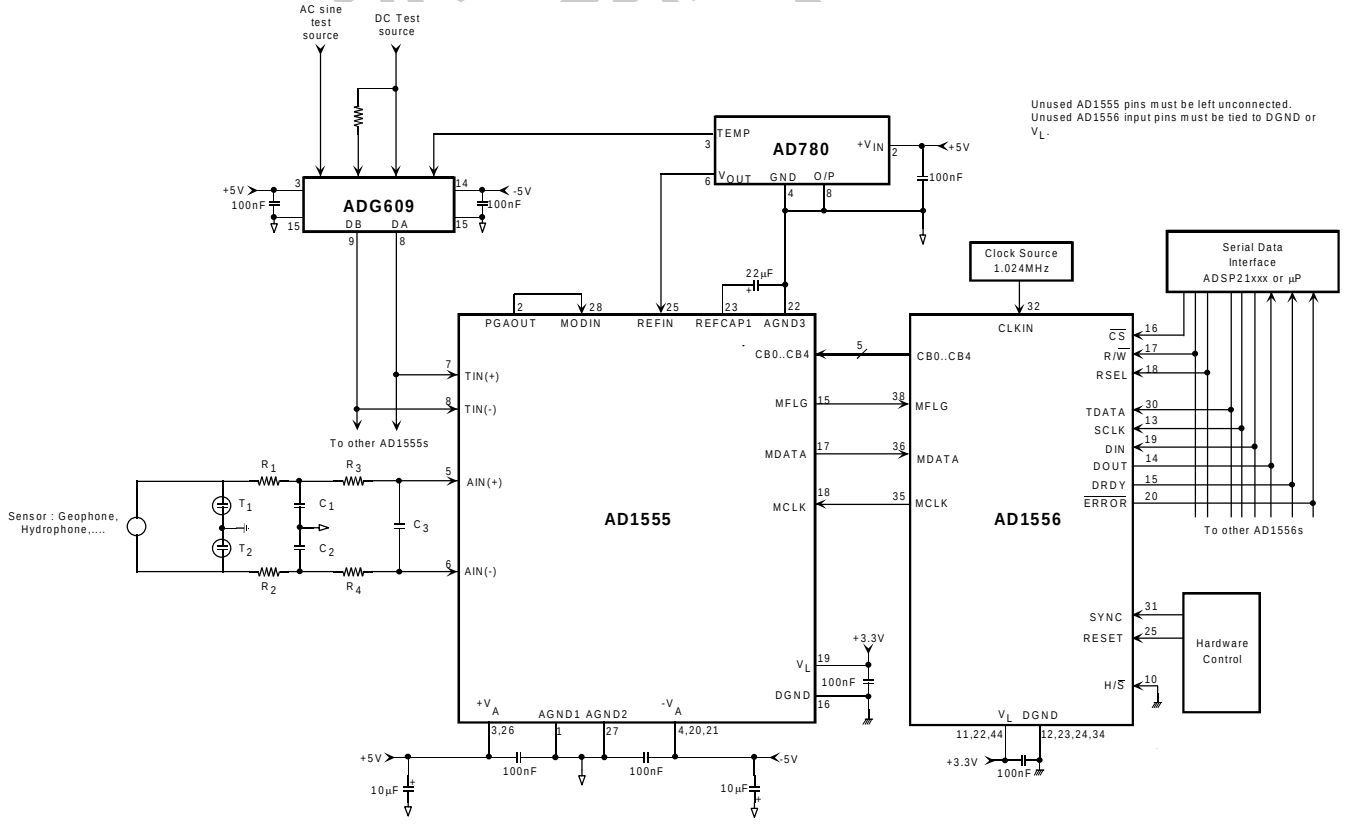


Figure 31. Typical operating circuit.

where the sensor inputs must be protected against severe external stresses as lightning, the inputs AIN are specifically designed to ease the design. The external voltage spike is generally clamped by devices T_1 and T_2 at about hundred volts (for instance, devices T_1 and T_2 can be gas discharge tubes) and, then, generates a pulsed current in the serial resistances (R_1,R_3 and R_2,R_4). The AD1555 AIN inputs, using robust internal clamping diodes to the analog supply rails, can handle this huge pulsed input current (TDB A during TBD μs) without experiencing any destructive damages or latch-up whether the AD1555 is powered on or not. Meanwhile, enough time should be left between multiple spikes in order to avoid excessive power dissipation.

Programming the AD1555

The different hardware events of the AD1555 as multiplexer inputs selection, programmable gain settings and power-down modes are selectable using the control pins bus CB0 to CB4 according to the Table III. This table is only valid when MCLK is toggling otherwise, the AD1555 is powered down. When used in combination with the AD1556, this control bus could be either loaded by hardware (H/$\overline{S}$ pin high) or via the serial interface of the AD1556 (H/$\overline{S}$ pin low).

The multiplexer which exhibits a break-before-make switching action, allows various combinations.

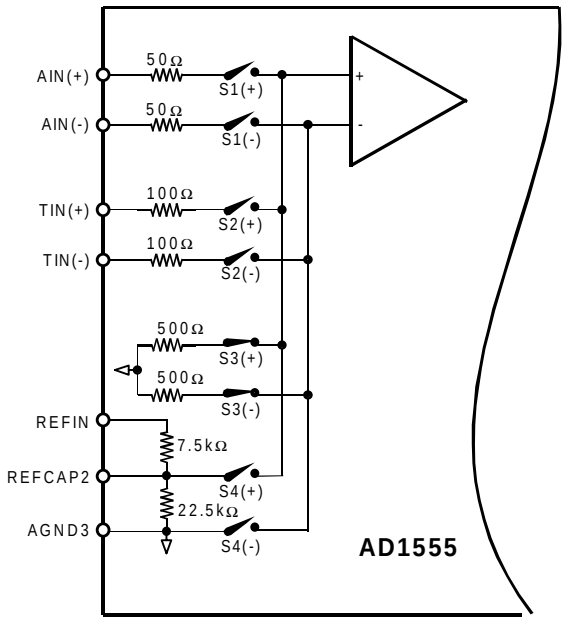


Figure 32. Simplified AD1555 input multiplexer.

TABLE III. PGA INPUT AND GAIN CONTROL

CB4	CB3	CB2	CB1	CB0	Description
0	0	0	0	0	Ground input with PGA Gain = 0 dB
0	0	0	0	1	Ground input with PGA Gain = 12 dB
0	0	0	1	0	Ground input with PGA Gain = 24 dB
0	0	0	1	1	Ground input with PGA Gain = 36 dB
0	0	1	0	0	Ground input with PGA Gain = 48 dB
0	1	0	0	0	Test inputs TIN(+) and TIN(-) with PGA Gain = 0 dB
0	1	0	0	1	Test inputs TIN(+) and TIN(-) with PGA Gain = 12 dB
0	1	0	1	0	Test inputs TIN(+) and TIN(-) with PGA Gain = 24 dB
0	1	0	1	1	Test inputs TIN(+) and TIN(-) with PGA Gain = 36 dB
0	1	1	0	0	Test inputs TIN(+) and TIN(-) with PGA Gain = 48 dB
1	0	0	0	0	Signal inputs AIN(+) and AIN(-) with PGA Gain = 0 dB
1	0	0	0	1	Signal inputs AIN(+) and AIN(-) with PGA Gain = 12 dB
1	0	0	1	0	Signal inputs AIN(+) and AIN(-) with PGA Gain = 24 dB
1	0	0	1	1	Signal inputs AIN(+) and AIN(-) with PGA Gain = 36 dB
1	0	1	0	0	Signal inputs AIN(+) and AIN(-) with PGA Gain = 48 dB
1	1	0	0	0	V_{REF} input with PGA Gain = 0 dB
1	1	0	0	1	Sensor Test1 : Signal inputs AIN(+) and AIN(-) with AIN(+) and AIN(-) inputs tied respectively to TIN(+) and TIN(-) inputs and with PGA Gain = 0 dB
1	1	0	1	0	Sensor Test2 : Signal inputs TIN(+) and TIN(-) with AIN(-) input tied to TIN(-) input and with PGA Gain = 0 dB
X	X	1	0	1	PGA powered down
X	X	1	1	X	Chip powered down

When the "Ground input" is selected, S3(+) and S3(-) are closed, all the other switches are opened and the inputs of the programmable gain amplifier are shorted through an accurate internal 1kΩ resistor. This combination allows accurate calibration of the offset of the AD1555 for each gain setting. Also, a system noise calibration can be done using the internal 1kΩ resistor as a noise reference.

When the "V_{REF} input" is selected, S4(+) and S4(-) are closed, all the other switches are opened and a reference voltage (2.25V) equal to half of the full scale range is sampled. In this combination, the gain setting is forced to be the 0dB gain.

When the "Signal input" is selected, S1(+) and S1(-) are closed, all the other switches are opened and the differential input signal between AIN(+) and AIN(-) is sampled. This is the main path for signal acquisition.

When the "Test input" is selected, S2(+) and S2(-) are closed, all the other switches are opened and the differential input signal between TIN(+) and TIN(-) is sampled. This combination allows acquisition of a test signal or a secondary channel with the same level of performance as with AIN inputs. By applying known voltages to these inputs, it is also possible to calibrate the gain for each gain setting.

When the "Sensor Test1" is selected, S1(+), S1(-), S2(+), S2(-) are closed, all the other switches are opened and the gain setting is forced to be the 0dB gain. In this configuration, a source between TIN(+) and TIN(-) may be applied to the sensor to determine its impedance or other characteristics. The total internal serial resistance between each AIN inputs and the PGA inputs, nominally 66 Ω, slightly affects these measurements. The total internal serial resistance between each TIN inputs and the PGA inputs is nominally 116 Ω.

When the "Sensor Test2" is selected, S1(+), S2(+) and S2(-) are closed, all the other switches are opened. This configuration could be used to test the sensor isolation.

Power-down modes of the AD1555

The AD1555 has 2 power-down modes. The multiplexer and programmable gain amplifier can be powered down by the CB2-CB0 setting of "101". The entire chip is powered-down by either CB2-CB1 set to "11" or by keeping the clock input MCLK at a fixed level high or low. Less shutdown current flows with MCLK low. The least power dissipation is achieved when the external reference is shut down eliminating the current through the 30kΩ nominal load at REFIN. When in power-down, the multiplexer is switched to the "ground input".

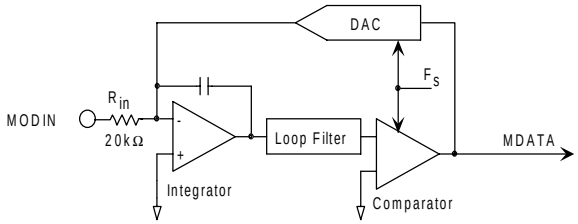


Figure 33. Sigma-Delta Modulator block diagram.

SIGMA-DELTA MODULATOR

The AD1555 sigma-delta modulator achieves its high level of performance, notably in dynamic range and distortion, through the use of a switched-capacitor feedback DAC in an otherwise continuous-time design. Novel circuitry eliminates the subtle distortion normally encountered when these disparate types are connected together. As a result, the AD1555 enjoys many of the benefits of both design techniques.

Because of the switched-capacitor feedback, this modulator is much less sensitive to timing jitter than is the usual continuous-time design which relies on the duty cycle of the clock to control a switched-current feedback DAC.

Unlike its fully switched-capacitor counterparts, the modulator input circuitry is non-sampling, consisting simply of an internal, low temperature coefficient resistor connected to the summing node of the input integrator. Among the advantages of this continuous-time architecture is a relaxation of requirements for the anti-alias filter; in fact, the output of the programmable gain amplifier, PGAOUT, may be tied directly to the input of the modulator MODIN without any external filter. Another advantage is that the gain may be adjusted to accommodate a higher input range by adding an external series resistor at MODIN.

The modulator of the AD1555 is fourth order which very efficiently shapes the quantization noise so that it is pushed toward the higher frequencies (above 1kHz) as shown in the figure 10. This high frequency noise is attenuated by the AD1556 digital filter. However, when the output word rate of the AD1556 is higher than 4kHz (-3dB frequency is higher than 1634Hz), the efficiency of this filtering is limited and slightly reduces the dynamic range, as shown in the Table I. Hence, when possible, an OWR of 2kHz or lower is generally preferred.

Sigma-delta modulators have the potential to generate “idle tones” which occur for DC inputs close to ground. To prevent this undesirable effect, the AD1555 modulator offset is set to about -70mV. In this manner, any existing idle tones are moved out of the band of interest and are filtered out by the digital filter.

Also, sigma-delta modulators may oscillate when the analog input is overranged. To avoid any instability, the modulator of the AD1555 includes circuitry to detect a string of 16 identical bits (“0” or “1”). Upon this event, the modulator is reset by discharging the integrator and loop filter capacitors and MFLG is forced high. After 1.5 MCLK cycles, MFLG returns low.

DIGITAL FILTERING

The AD1556 is a digital finite impulse response (FIR) low-pass filter and serves as the decimation filter for the AD1555. It takes the output bitstream of the AD1555, filters and decimates it by a user-selectable choice of seven different filters associated with seven decimation ratios, in power of 2 from 1/16 to 1/1024. With a nominal bit rate of 256 kbits/s at the AD1556 input, the output word rate OWR (the inverse of the sampling rate) ranges from 16 kHz (1/16ms) to 250 Hz (4 ms) in powers of 2. The AD1556 filter achieves a maximum passband flatness of +/-0.05 dB for each decimation ratio and an out-of-band attenuation of -135 dB maximum for each decimation ratio except 1/16 (OWR = 16 kHz) at which the out-of-band attenuation is -86 dB maximum. Table II gives for each filter the passband frequency, the -3 dB frequency, the stopband frequency and the group delay. The passband frequency is 37.5 % of the output word rate and the -3 dB frequency is approximately 41% of the output word rate. The noise generated by the AD1556 even that due to the word truncation, has a negligible impact on the dynamic range performance of the AD1555-AD1556 chip-set.

Architecture

The functional block diagram of the filter portion of the AD1556 is given in figure 34. The basic architecture is a 2 stage filter. The second stage has a decimation ratio of 4 for all filters except at the output word rate of 250 Hz where the decimation ratio is 8. Each filter is a linear phase equiripple FIR implemented by summing symmetrical pairs of data samples and then convoluting by multiplication and accumulation.

The input bitstream at 256 kHz enters the first filter and is multiplied by the 26-bit-wide coefficients tallied in Table IV. Due to the symmetry of the filter, only half of the coefficients are stored in the internal ROM and each is used twice per convolution. Because the multiplication uses a one bit input data, the convolution for the first stage is implemented with a single accumulator 29 bits wide to avoid any truncation in the accumulation process. The output of the first stage filter is decimated with the ratios given in Table IV and then are stored in an internal RAM which truncates the accumulator result to 24 bits.

The second stage filter architecture is similar to the first stage. The main difference is the use of a true multiplier. The multiplier, the accumulator and the output register which are respectively 32 bits, 35 bits and 24 bits wide introduce some truncation which do not affect the overall dynamic performance of the AD1555-AD1556 chip-set.

Filter coefficients

As indicated before, each stage for each filter uses different set of coefficients. These coefficients are provided with the EVAL-AD1555/56EB, the evaluation board for the AD1555 and the AD1556.

Reset operation

The RESET pin initializes the AD1556 in a known state. RESET is active on the next CLKIN rising edge after the

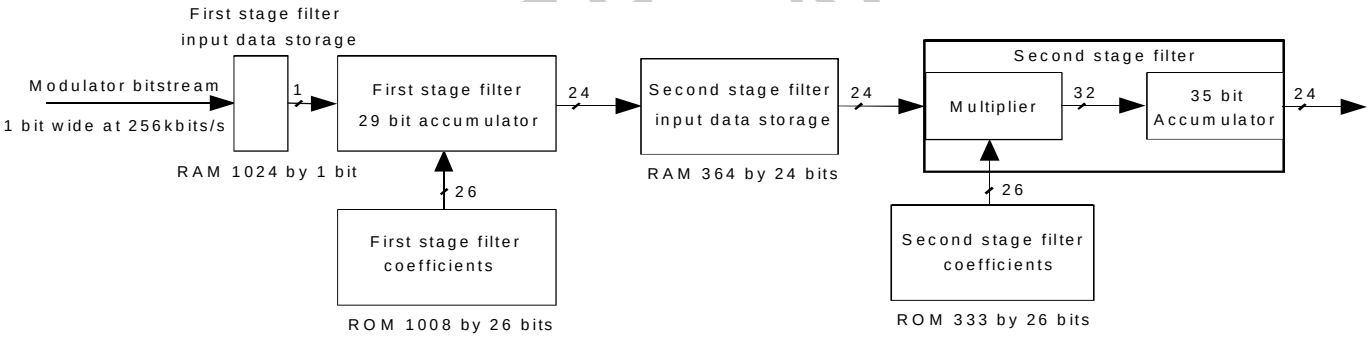


Figure 34. AD1556 Filter functional block diagram.

TABLE IV. FILTER DEFINITION

Output Word Rate F_o(Hz) [Sampling Rate (ms)]	Decimation ratio		Number of Coefficients	
	First stage	Second stage	First stage	Second stage
16000 [1/16 ms]	4	4	32	118
8000 [1/8 ms]	8	4	64	184
4000 [1/4 ms]	16	4	128	184
2000 [1/2 ms]	32	4	256	184
1000 [1 ms]	64	4	512	184
500 [2 ms]	128	4	1024	184
250 [4 ms]	128	8	1024	364

RESET input is brought high as shown in the Figure 4. The reset value of each bit of the configuration and the status registers are indicated in Table V and Table VIII. The filter memories are not cleared by the reset. Filter convolutions begin on the next CLKIN rising edge after the RESET input is returned low.A RESET operation is done on power-up, independent of the RESET pin state.

Power-down operation

The PWRDN pin puts the AD1556 in a power-down state. PWRDN is active on the next CLKIN rising edge after the PWRDN input is brought high. While in this state, MCLK is held at a fixed level and the AD1555 is, therefore, powered-down too. The serial interface remains active allowing read and write operations of the AD1556. The configuration and status registers maintain their content during the power-down state.

SYNC operation

SYNC is used to create a relationship between the analog input signal and the output samples of the AD1556. The SYNC event does 2 things :

- It synchronizes the AD1555 clock MCLK to the AD1556 clock CLKIN as shown in Figure 3.
- It clears the filter and then initiates the filter convolution.

Exactly one sampling rate delay later, the DRDY pin goes high. A SYNC event occurs on the next CLKIN rising edge after the SYNC input is brought high as shown in the Figure 3. The DRDY output goes high on the next falling edge of CLKIN. SYNC may be applied once or kept high or applied synchronously at the output word rate, all with the same effect.

Configuring the AD1556

The AD1556 configuration can be loaded either by hardware (H/$\overline{S}$ pin high) or via the serial interface of the AD1556 (H/$\overline{S}$ pin low). Table V gives the description of each bit of the configuration register and Table VI defines the selection of the filter bandwidth. When the software mode is selected (H/$\overline{S}$ pin Low), the configuration register is loaded using the pins DIN, SCLK, $\overline{CS}$ and R/$\overline{W}$. In this mode, when RESET is active, the configuration register mimics the selection of the hardware pins. The AD1556 and the AD1555 can be put in power-down by software.

The DRDYBUF bit controls the operating mode of the DRDY output pin. When the DRDYBUF bit is low, the DRDY is a conventional CMOS push-pull output buffer as shown in Figure 35. When the DRDYBUF bit is high, the DRDY output pin is an open drain PMOS pull-up as shown in Figure 35. Many DRDY pins may be connected with an external pull-down resistor in a wired OR to minimize the interconnection between the AD1556s and the microprocessor in multichannel applications. The DRDY pin is protected against bit contention.

TABLE VI. FILTER BANDWIDTH SELECTION

BW2	BW1	BW0	Output Rate (ms)
0	0	0	4
0	0	1	2
0	1	0	1
0	1	1	1/2
1	0	0	1/4
1	0	1	1/8
1	1	0	1/16
1	1	1	Reserved

TABLE V. CONFIGURATION REGISTER DATA BITS

Bit Number	Name	Description	RESET State
DB15(MSB)	X		X
DB14	X		X
DB13	X		X
DB12	X		X
DB11	PWRDN	Power down mode	PWRDN
DB10	CSEL	Select TDATA input	CSEL
DB9	X		X
DB8	BW2	Filter bandwidth selection	BW2
DB7	BW1	Filter bandwidth selection	BW1
DB6	BW0	Filter bandwidth selection	BW0
DB5	DRDYBUF	DRDY output mode	0 (push-pull)
DB4	CB4	PGA Input select	PGA4
DB3	CB3	PGA Input select	PGA3
DB2	CB2	PGA Gain select	PGA2
DB1	CB1	PGA Gain select	PGA1
DB0(LSB)	CB0	PGA Gain select	PGA0

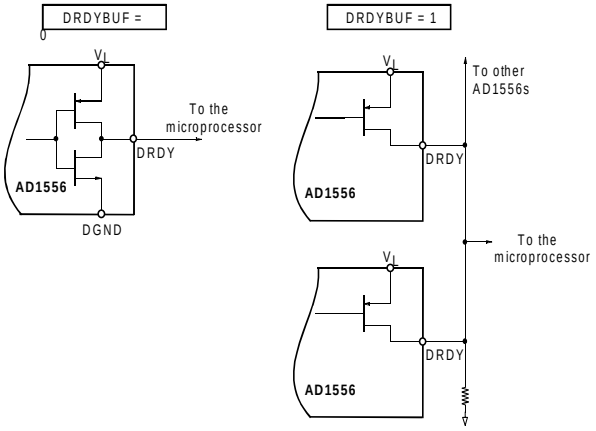


Figure 35. DRDY output pin configuration.

Analog Input and Digital output Data Format
When operating with a nominal MCLK frequency of 256 kHz, the AD1555 is designed to output a ones-density bit stream from 0.16607 to 0.83393 on its MDATA output pin corresponding to an input voltage from -2.25 V to +2.25 V on the MODIN pin.

The AD1556 computes a 24-bit 2's complement output whose codes range from decimal -5,602,416 to 5,602,415 as shown in Table VII.

TABLE VII. OUTPUT CODING

Analog input MODIN	output code	
	Hexa	Decimal
approx. +2.5V*	5EFC0A	+6224906
approx. +2.25V	557C6F	+5602415
approx. +2V	46FCD4	+4979924
approx. 0V	000000	0
approx. -2V	B40326	-4979925
approx. -2.25V	AA8390	-5602416
approx. -2.5V*	A103F5	-6224907

** input out of range.*

STATUS register
The AD1556 status register contains 24 bits that capture potential error conditions and readback the configuration settings. The status register mapping is defined in Table VIII.

The ERROR bit is the logical OR of the other error bits, OVWR, MFLG, and ACC. ERROR and the other error bits are reset low after completing a status register read operation or upon RESET. The ERROR bit is the inverse of the $\overline{\text{ERROR}}$ output pin.

The OVWR bit indicates if an unread conversion result is overwritten in the output data register. If a data read was started but not completed when a new data is loaded into the output data register, the OVWR bit is set high.

The MFLG status bit is set to the state of the MFLG input pin on the rising edge of CLKIN. MFLG will remain set high as long as the MFLG bit is set. The MFLG status bit will not change during power-down or RESET.

The ACC bit is set high and the data output is clipped to either +FS (0111...) or -FS (1000...) if an underflow or overflow has occurred in the digital filter.

The FLSTL bit indicates the digital filter has settled and the conversion results are an accurate representation of the analog input. FLSTL is set low on RESET and at power-up, and upon exiting the power-down state. FLSTL also goes low when SYNC sets the start of the filter's convolution cycle, when changes are made to the device setting with the hardware pins CB0-CB4, BW0-BW2, or CSEL, and when the MFLG status bit is set high. When FLSTL is low the OVWR, MFLG, ACC and DRNG status bits will not change.

The DRNG bit is used to indicate if the analog input to the AD1555 is outside its specified operating range. The DRNG bit is set high whenever the AD1556 digital filter computes four consecutive output samples that are greater than decimal 5,602,415 or all less than -5,602,416.

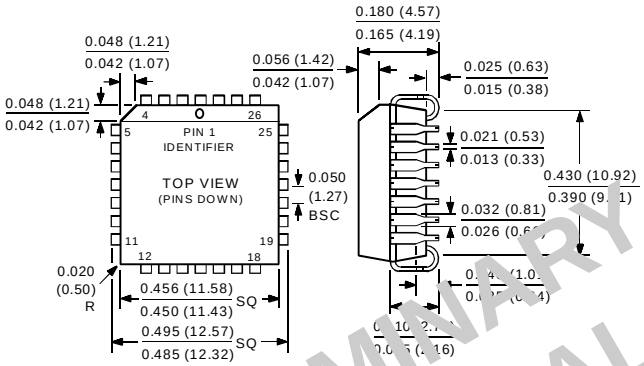
TABLE VIII. STATUS REGISTER DATA BITS

Bit Number	Name	Description	RESET State
DB23 (MSB)	ERROR	Detects one of the following Errors	0
DB22	OVWR	Read Sequence Overwrite Error	0
DB21	MFLG	Modulator Flag Error	MFLG
DB20	X		X
DB19	ACC	Accumulator Error	0
DB18	DRDY	Data Ready	0
DB17	FLSTL	Filter Settled	0
DB16	DRNG	Output Data not within AD1555 range	0
DB15	X		X
DB14	X		X
DB13	X		X
DB12	X		X
DB11	PWRDN	Power down mode	PWRDN
DB10	CSEL	Select TDATA input	CSEL
DB9	X		X
DB8	BW2	Filter bandwidth selection	BW2
DB7	BW1	Filter bandwidth selection	BW1
DB6	BW0	Filter bandwidth selection	BW0
DB5	X		X
DB4	CB4	PGA Input select	PGA4
DB3	CB3	PGA Input select	PGA3
DB2	CB2	PGA Gain select	PGA2
DB1	CB1	PGA Gain select	PGA1
DB0 (LSB)	CB0	PGA Gain select	PGA0

NOTE: The status register bits are set high when the description of the condition exists.

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

28-LEAD PLCC (P-28A)



OUTLINE DIMENSIONS
Dimensions shown in mm and (inches).

44-LEAD MQFP (S-44)