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Defense Electronics Supply Center
Dayton, Ohio

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REV D

MILITARY DRAWING
This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, DIGITAL, CMOS, DUAL 12-BIT, DIGITAL-TO-ANALOG CONVERTER, MONOLITHIC SILICON

DWG NO. 5962-87763

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5962-E695

1. SCOPE

1.1 Scope. This drawing describes requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices.

1.2 Part number. The completepart number shall be as shown in the following example:

5962	-	87763	01	L	X
Drawing number			Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	7537	8 + 4 loading structure, dual 12-bit CMOS D/A converter, 11-bit linearity, ±6 LSB's of gain error.
02	7537	8 + 4 loading structure, dual 12-bit CMOS D/A converter, 12-bit linearity, ±3 LSB's of gain error.
03	7537	8 + 4 loading structure, dual 12-bit CMOS D/A converter, 12-bit linearity, ±2 LSB's of gain error.

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and s follows:

Outline letter	Case outline
L	D-9(24 lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28 terminal, .460" x .460" x .100"), square chip-carrier package

1.3 Absolute maximum ratings.

VDD to DGND	-0.3 V, +17 V
V_{REFA}, V_{REFB} to AGNDA, AGNDB	±25 V
V_{RFBA}, V_{RFBB} to AGNDA, AGNDB	±25 V
Digital input voltage to DGND)	-0.3 V, V_{DD}+0.3 V
V_{IOUTA}, V_{IOUTB} to DGND	-0.3 V, V_{DD}+0.3 V
AGNDA, AGNDB to DGND	-0.3 V, V_{DD}+0.3 V
Power dissipation:	
Up to +75°C	450 mW
Derate above +75°C	6mW/°C
Thermal resistance (Θ_{JC}):	
Cases L and 3	See MIL-M-38510, appendix C
Thermal resistance (Θ_{JA})	120°C/W

1.4 Recommended operating conditions.

Ambient operating temperature range	-55°C to +125°C
Supply voltage range (V_{DD})	10.8 V dc to 16.5 V dc
Minimum high level input voltage	2.4 V dc
Maximum low level input voltage	0.8 V dc
V_{REFA}, V_{REFB}	10 V dc
V_{AGNDA}, V_{IOUTA}	0 V dc
V_{AGNDB} V_{IOUTB}	8 ns/V
Output amplifiers	AD644 or equivalent

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections and function descritions. The terminal connections and function descriptions shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics . Unless otherwise specified,, the electrical performance characteristics are as specified in table I andl apply over the full ambient operating temperature range.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution					12		Bits
Input low voltage	V_{IL}	V_{DD} = 10.8 and 16.5 V	1, 2, 3	All		0.8	V
Input high voltage	V_{IH}	V_{DD} = 10.8 and 16.5 V	1, 2, 3	All	2.4		V
Input current	I_{IN}	$V_{IN} = V_{DD}$ = 16.5 V	1	All		1.0	μA
			2, 3			10.0	
Supply current	I_{DD}	V_{DD} = 16.5 V	1, 2, 3	All		2.0	mA
Relative accuracy	RA	V_{DD} = 10.8 V and 16.5 V	1	All	-1.0	+1.0	LSB
			2, 3	01	-1.0	+1.0	
			2, 3	02, 03	-0.5	+0.5	
			12	02, 03	-0.5	+0.5	
Differential nonlinearity	DNL	All grades guaranteed monotonic to 12 bits over -55°C to +125°C range. V_{DD} = 10.8 V and 16.5 V	1,2,3	All	-1.0	+1.0	LSB
Gain error	A_E	Measured using R_{FA} and R_{FB}; Both DAC registers loaded with all 1's. V_{DD} = 10.8 V	1	All	-6.0	+6.0	LSB
			2, 3	01	-6.0	+6.0	
			2, 3	02	-3.0	+3.0	
			2, 3	03	-2.0	+2.0	
			12	02	-3.0	+3.0	
			12	03	-2.0	+2.0	
Gain temperature 2/ coefficient	TCA_E/dt		4	All	-5.0	+5.0	ppm /°C
Output leakage current	I_{OUTA}	DAC A register loaded with all 0's V_{DD} = 16.5 V	1	All	-10	+10	nA
			2, 3	All	-250	+250	
Output leakage current	I_{OUTB}	DAC B register loaded with all 0's V_{DD} = 16.5 V	1	All	-10	+10	nA
			2, 3	All	-250	+250	
Reference input resistance	R_I	V_{DD} = 10.8 V	1, 2, 3	All	9	20	kΩ
Reference input resistance match. V_{REFA}, V_{REFB}	R_{IN}	V_{DD} = 10.8 V	1	All	-3	+3	%
			2, 3	01, 02	-3	+3	
			2, 3	03	-1	+1	
			12	03	-1	+1	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output current 2/ 3/ settling time	t_{SL}		4	All		1.5	μS
AC feedthrough V_{REFA} to I_{OUTA} and V_{REFB} to I_{OUTB} 2/	FT	V_{REFA}, V_{REFB} = 20 V P-P 10 kHZ sinewave. DAC register loaded with all 0's.	4	All		-65	dB
Power supply rejection ratio	PSRR	$V_{DD} = V_{DD}$ max - V_{DD} min V_{DD} = 10.8 V	1	All	-0.01	+0.01	%%
			2, 3	All	-0.02	+0.02	
Output capacitance for DAC A and DAC B	C_{OUT}	DAC A, DAC B loaded with 0's	4	All		70	pF
		DAC A, DAC B loaded with 1's	4			140	
Functional test		See 4.3.1c	7	All			
Address valid to write setup time, t_1	t_{AWS}	See figure 4	9, 10, 11	All	30		ns
Address valid to write hold time, t_2	t_{AWH}		9, 10, 11	All	25		
Data setup time, t_3	t_{OS}		9, 10, 11	All	80		
Data hold time, t_4	t_{OH}		9, 10, 11	All	25		
Chip select or update to write setup time, t_5	t_{CWS}		9, 10, 11	All	0		
Chip select or update to write hold time, t_6	t_{CWH}		9, 10, 11	All	0		
Write pulse width, t_7	t_{WR}		9, 10, 11	All	100		
Clear pulse width, t_8	t_{CL}		9, 10, 11	All	100		

1/ V_{DD} = 10.8 V to 16.5 V except where otherwise specified; $V_{REFA} = V_{REFB}$ = 10 V (see 1.4). $V_{AGNDA} = V_{AGNDB}$ = 0 V, $V_{IOUTA} = V_{IOUTB}$ = 0 V.

2/ Guaranteed if not tested to the limits as specified on table I.

3/ To 0.01 percent of full-scale range. I_{OUT} = 100Ω; C_{EXT} = 13 pF. DAC output measured from rising edge of $\overline{WR}$.

Device types 01, 02, and 03

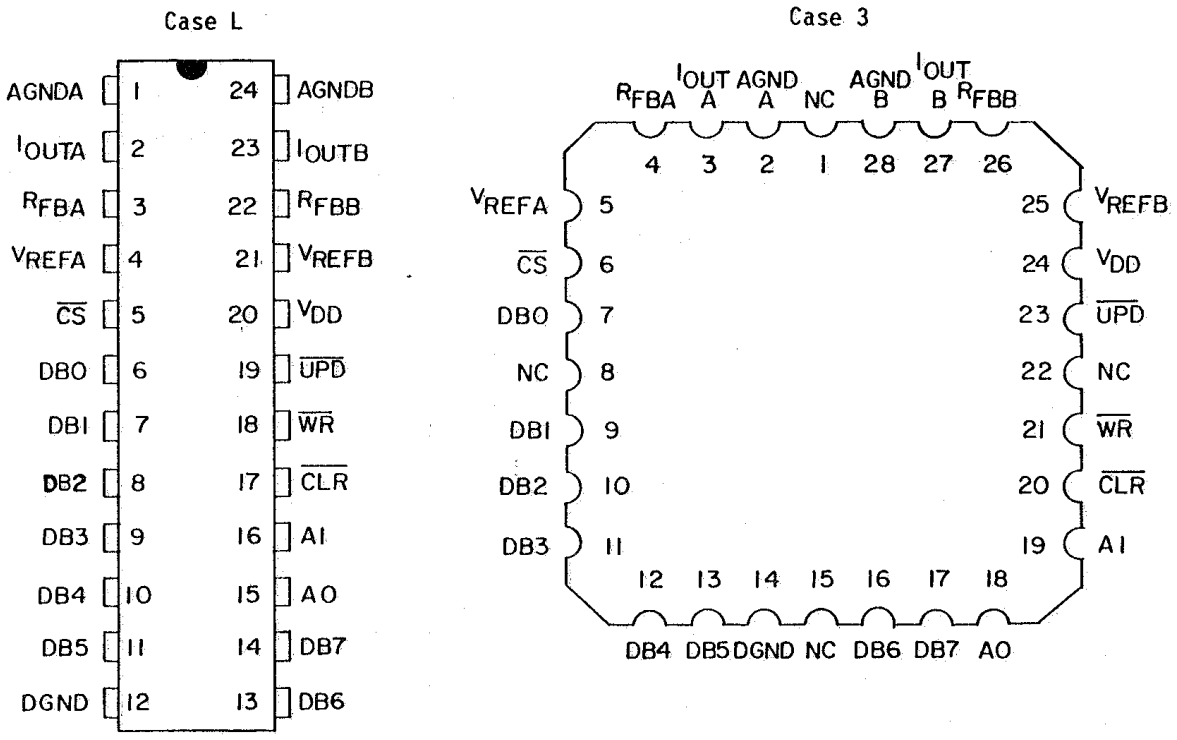

FIGURE 1. Terminal connections and function descriptions.

Pin function description

Mnemonic	Description
AGNDA	Analog ground for DAC A.
I_{OUTA}	Current output terminal of DAC A.
R_{FBA}	Feedback resistor for DAC A.
V_{REFA}	Reference input to DAC A.
$\overline{CS}$	Chip select input. Active low.
DB0-DB7	Eight data inputs, DB0-DB7
DGND	Digital ground.
A0	Address line 0.
A1	Address line 1.
$\overline{CLR}$	Clear input. Active low. Clears all registers.
$\overline{WR}$	Write input. Active low.
$\overline{UPD}$	Updates DAC registers from inputs registers.
V_{DD}	Power supply input. Nominally +12 V to +15 V, with ±10 percent tolerance.
V_{REFB}	Reference input to DAC B.
R_{FBB}	Feedback resistor for DAC B.
I_{OUTB}	Currentoutput terminal of DAC B.
AGNDB	Analog ground for DAC B.

FIGURE 1. Terminal connections and function descriptions - Continued.

$\overline{CLR}$	$\overline{UPD}$	$\overline{CS}$	$\frac{W}{R}$	A1	A∅	Function
1	1	1	X	X	X	No data transfer
1	1	X	1	X	X	No data transfer
0	X	X	X	X	X	All registers cleared
1	1	0	0	0	0	DAC C LS input register Loaded with DB7 - DB0
1	1	0	0	0	1	DAC A MS input register Loaded with DB7 - DB0
1	1	0	0	1	0	DAC B LS input register Loaded with DB7 - DB0
1	1	0	0	1	1	DAC B MS input register Loaded with DB3 - DB0
1	0	1	0	X	X	DAC A, DAC B registers Updated simutaneously from input registers
1	0	0	0	X	X	DAC A, DAC B registers are transparent

NOTE: X = Don't care.

FIGURE 2. Truth table.

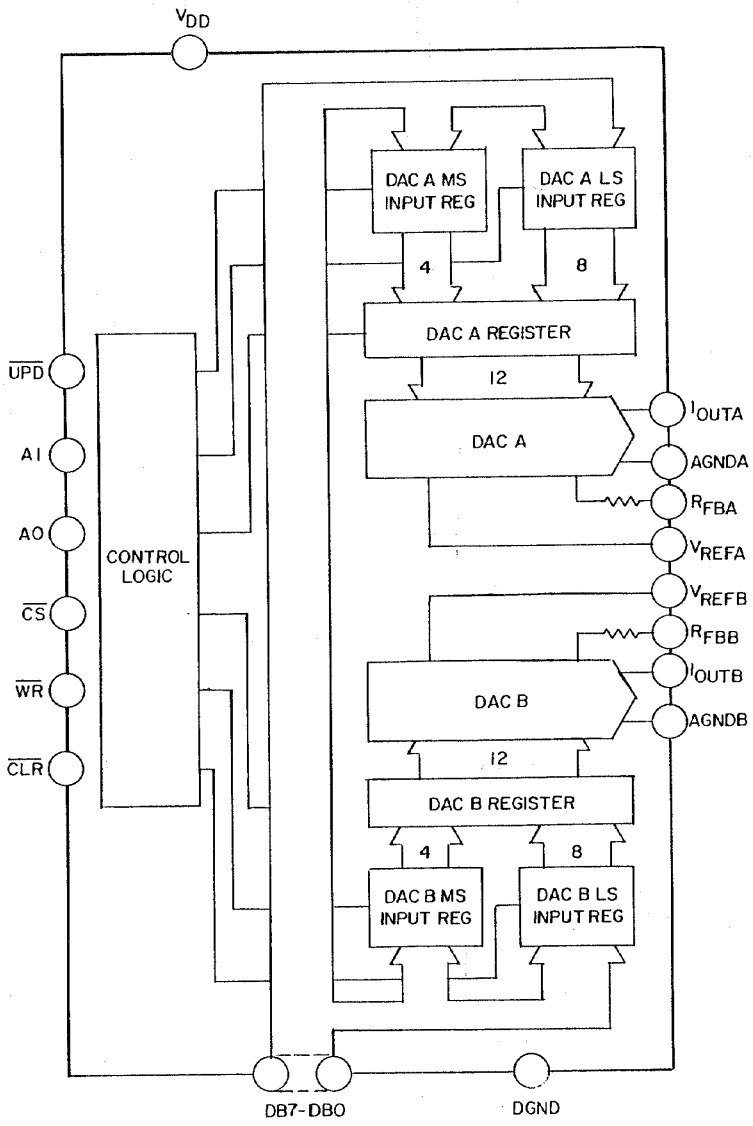

FIGURE 3. Logic diagram.

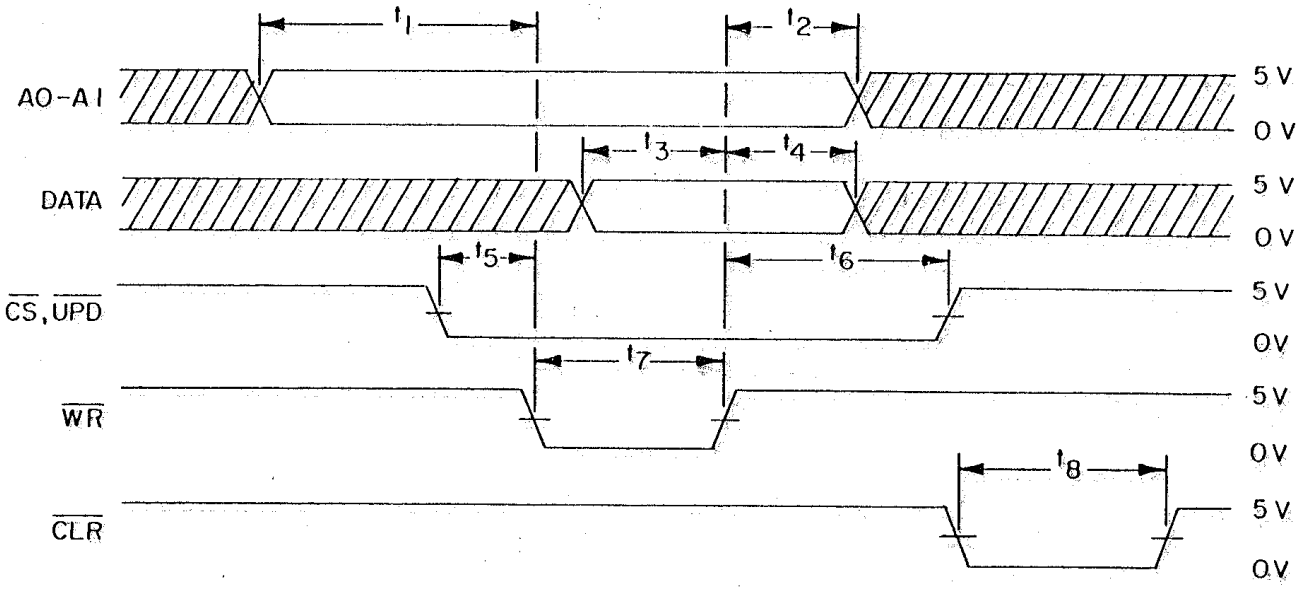

FIGURE 4. Timing diagram.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufactuer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance . A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the rquirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the aquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. Optional subgroup 12 is used for grading and part selection at 25°C, not included in PDA.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 shall verify the truth table (see figure 2).

d. Optional subgroup 12 is used for grading and part selection at +25°C.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters, method 5004	1
Final electrical parameters, method 5004	1*,2,3,4,7,12
Group A test requirements, method 5005	1,2,3,4,7,9,10**,11**,12
Groups C and D end-point electrical parameters,method 5005	1,12

*PDA applies to subgroup 1.
**Subgroups 10 and 11 shall be guaranteed if not tested.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Tesr duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use whewn military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified
for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item
for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-8776301LX		AD7537SQ/883B
5962-87763013X	24355	AD7537SE/883B
5962-8776302LX		AD7537TQ/883B
5962-87763023X	24355	AD7537TE/883B
5962-8776303LX		AD7537UQ/883B
5962-87763033X	24355	AD7537UE/883B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24335	Analog Devices 1 Technology Way Norwood, MA 02062