

**REVISIONS**

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Made changes to 3.3, 4.2, 4.3.1, and 4.3.2. Made changes to table I. Editorial changes throughout.	90-03-08	M. A. Frye
B	Add device type 07. Add vendors CAGES 1ES66 and 54186. Editorial changes throughout.	93-01-22	M. A. Frye

REV																				
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REV	B	B																		
SHEET	15	16																		

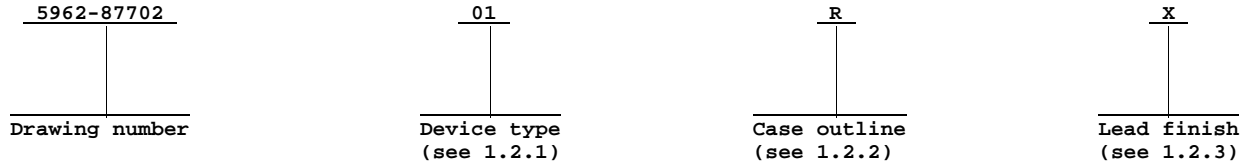
<b>REV STATUS OF SHEETS</b>	<b>REV</b>	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	<b>SHEET</b>	1	2	3	4	5	6	7	8	9	10	11	12	13	14			

<b>PMIC N/A</b>	PREPARED BY Sandra Rooney	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444		
<b>STANDARDIZED MILITARY DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE  AMSC N/A	CHECKED BY Charles E. Besore	<b>MICROCIRCUIT, CMOS, 12-BIT MULTIPLYING DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON</b>		
	APPROVED BY M. A. Frye			
	DRAWING APPROVAL DATE 88-01-28			
	REVISION LEVEL B			
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;"><b>SIZE</b> A</td> <td style="width: 30%;"><b>CAGE CODE</b> 67268</td> <td style="width: 40%; text-align: center;"><b>5962-87702</b></td> </tr> </table>		<b>SIZE</b> A	<b>CAGE CODE</b> 67268
<b>SIZE</b> A	<b>CAGE CODE</b> 67268	<b>5962-87702</b>		
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1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	7545S	CMOS 12-bit buffered DAC
02	7545T	CMOS 12-bit buffered DAC
03	7545U	CMOS 12-bit buffered DAC
04	7545GU	CMOS 12-bit buffered DAC
05	7545B	CMOS 12-bit buffered DAC
06	7545A	CMOS 12-bit buffered DAC
07	7545S	CMOS 12-bit buffered DAC

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish shall be as specified in MIL-M-38510. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Supply voltage range ( $V_{DD}$ )	- - - - -	+5 V dc to +15 V dc
$V_{REF}$ to GND	- - - - -	-0.3 V dc to +17 V dc
Digital input voltage to DGND	- - - - -	-0.3 V dc to $V_{DD}$
$V_{RFB}$ , $V_{REF}$ to DGND	- - - - -	$\pm 25$ V dc
V pin 1 to DGND	- - - - -	-0.3 V dc to $V_{DD}$
AGND to DGND	- - - - -	-0.3 V dc to $V_{DD}$
Power dissipation ( $P_D$ ):		
Up to +75°C	- - - - -	450 mW
Derates above +75°C	- - - - -	6 mW/°C
Storage temperature range	- - - - -	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	- - - - -	+300°C
Thermal resistance junction-to-case ( $\theta_{JC}$ )	- - - - -	See MIL-STD-1835
Thermal resistance junction-to-ambient ( $\theta_{JA}$ ):		
Case R	- - - - -	+120°C/W
Case 2	- - - - -	+120°C/W
Junction temperature ( $T_J$ )	- - - - -	+175°C

1.4 Recommended operating conditions.

Operating ambient temperature range ( $T_A$ )	- - - - -	-55°C to +125°C
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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.  
 MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawing (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Mode selection. The mode selection shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified <u>1/</u>	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Resolution	RES	V <sub>DD</sub> = +5 V	1,2,3	All	12		Bits
		V <sub>DD</sub> = +15 V	1,2,3	All	12		
Relative accuracy	RA	V <sub>DD</sub> = +5 V	1,2,3	01,07		±2	LSB
			1	02		±2	
			2,3			±1	
		V <sub>DD</sub> = +5 V T <sub>A</sub> = +25°C <u>2/</u>	12			±1	
		V <sub>DD</sub> = +5 V	1	03,04		±2	
				05,06		±.5	
			2,3	03,04 05,06		±.5	
		V <sub>DD</sub> = +5 V T <sub>A</sub> = +25°C <u>2/</u>	12			±.5	
		V <sub>DD</sub> = +15 V	1,2,3	01,07		±2	
			1	02		±2	
			2,3			±1	
						±1	
V <sub>DD</sub> = +15 V T <sub>A</sub> = +25°C <u>2/</u>	12				±1		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified <u>1/</u>	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Relative accuracy	RA	V <sub>DD</sub> = +15 V	1	03,04		±2	LSB
				05,06		±.5	
		V <sub>DD</sub> = +15 V <u>2/</u>	2,3	03,04 05,06		±.5	
			12			±.5	
Differential nonlinearity	DNL	V <sub>DD</sub> = +5 V 10-bit monotonic	1,2,3	01,07		±4	LSB
		V <sub>DD</sub> = +5 V 12-bit monotonic	1	02,03 04		±4	
				05,06		±1	
		V <sub>DD</sub> = +5 V <u>2/</u> 12-bit monotonic	2,3	02,03 04,05 06		±1	
			12			±1	
		V <sub>DD</sub> = +15 V 10-bit monotonic	1,2,3	01,07		±4	
		V <sub>DD</sub> = +15 V 12-bit monotonic	1	02,03 04		±4	
				05,06		±1	
V <sub>DD</sub> = +15 V <u>2/</u> 12-bit monotonic	2,3	02,03 04,05 06		±1			
	12			±1			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified <u>1/</u>		Group A subgroups	Device types	Limits		Unit		
						Min	Max			
Power supply rejection	PSRR	ΔV <sub>DD</sub> = ±5%	V <sub>DD</sub> = +5 V	1	01,02 03,04 07		.015	±%/%		
				2,3		.03				
				1	05,06		.002			
				2,3		.004				
				1	01,02 03,04 07		.01			
				2,3		.02				
			V <sub>DD</sub> = +15 V	1	01,02 03,04 07		.01			
				2,3			.02			
				1	05,06		.002			
				2,3			.004			
Gain error <u>3/</u>	AE	Dac register loaded with 1111 1111 1111	V <sub>DD</sub> = +5 V	1,2,3	01,07		±20	LSB		
				1	02		±20			
				2,3			±10			
			<u>2/</u>							
			V <sub>DD</sub> = +5 V	12		±10				
			T <sub>A</sub> = +25°C							
			V <sub>DD</sub> = +5 V	1	03		±20			
					05		±3			
				2,3	03		±6			
					05		±4			
<u>2/</u>										
V <sub>DD</sub> = +5 V	12	03		±5						
T <sub>A</sub> = +25°C		05		±3						

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified <u>1/</u>		Group A subgroups	Device types	Limits		Unit	
						Min	Max		
Gain error <u>3/</u>	AE	Dac register loaded with 1111 1111 1111	V <sub>DD</sub> = +5 V	1	04		±20	LSB	
					06		±1		
				2,3	04,06		±2		
				<u>2/</u> V <sub>DD</sub> = +5 V	12		±1		
				V <sub>DD</sub> = +15 V	1,2,3	01,07			±25
					1	02			±25
					2,3				±15
				<u>2/</u> V <sub>DD</sub> = +15 V	12		±15		
				V <sub>DD</sub> = +15 V	1	03			±25
						05			±3
					2,3	03			±10
						05			±4
				<u>2/</u> V <sub>DD</sub> = +15 V	12	03			±10
						05			±3

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified <u>1/</u>		Group A subgroups	Device types	Limits		Unit					
						Min	Max						
Gain error <u>3/</u>	AE	Dac register loaded with 1111 1111 1111	V <sub>DD</sub> = +15 V	1	04		±25	LSB					
					06		±1						
				2,3	04		±7						
					06		±2						
				<u>2/</u> V <sub>DD</sub> = +15 V T <sub>A</sub> = +25°C	12	04			±6				
						06			±1				
Output leakage current Pin 1	I <sub>OUT1</sub>	DB0 to DB11 = 0 V, WR, CS = 0 V	V <sub>DD</sub> = +5 V	1	All		±10	nA					
				2,3			±200						
				V <sub>DD</sub> = +15 V	1	All			±10				
					2,3				±200				
				Referenced input resistance Pin 19 to ground	R <sub>IN</sub>		V <sub>DD</sub> = +5 V		1,2,3	01,02 03,04 07	7	25	kΩ
										05,06	7	15	
V <sub>DD</sub> = +15 V		01,02 03,04 07	7				25						
		05,06	7				15						
Digital input high voltage	V <sub>IH</sub>		V <sub>DD</sub> = +5 V	1,2,3	All	2.4		V					
			V <sub>DD</sub> = +15 V	1,2,3	All	13.5							

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified <u>1/</u>	Group A subgroups	Device types	Limits		Unit		
					Min	Max			
Digital input low voltage	V <sub>IL</sub>		V <sub>DD</sub> = +5 V	1,2,3	All		0.8	V	
			V <sub>DD</sub> = +15 V	1,2,3	All		1.5		
Digital input leakage current	I <sub>IN</sub>		V <sub>DD</sub> = +5 V	1	All		±1	μA	
				2,3			±10		
			V <sub>DD</sub> = +15 V	1	All		±1		
				2,3			±10		
Supply current from V <sub>DD</sub>	I <sub>DD</sub>	All digital inputs V <sub>IL</sub> or V <sub>IH</sub>	V <sub>DD</sub> = +5 V	1,2,3	All		2	mA	
				1,2,3			2		
			V <sub>DD</sub> = +5 V	1	01,02 03,04 07		100		μA
				2,3			500		
		1,2,3		05,06		100			
		V <sub>DD</sub> = +15 V	1	01,02 03,04 07		100			
			2,3			500			
			1,2,3		05,06	100			
Gain temperature coefficient	TCAE	<u>4/</u>	V <sub>DD</sub> = +5 V	1,2,3	All		±5	ppm/°C	
			V <sub>DD</sub> = +15 V	1,2,3		01,02 03,04 07			±10
		05,06					±5		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified <u>1/</u>	Group A subgroups	Device types	Limits		Unit	
					Min	Max		
Feedthrough error	F <sub>T</sub>	V <sub>REF</sub> = ±10 V, 10 kHz sinewave <u>4/ 5/</u>	V <sub>DD</sub> = +5 V	4,5,6	All		10	mV p-p
			V <sub>DD</sub> = +15 V	4,5,6	All		10	
Digital input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V <u>6/</u> DB0 to DB11	V <sub>DD</sub> = +5 V T <sub>A</sub> = +25°C	4	01,02 03,04 07		5	pF
					05,06		8	
					All		20	
		<u>WR</u> , <u>CS</u>	V <sub>DD</sub> = +15 V T <sub>A</sub> = +25°C	4	01,02 03,04 07		5	
					05,06		8	
					All		20	
Output capacitance	C <sub>OUT1</sub>	DB0 to DB11 <u>4/</u> = 0 V <sub>I</sub> <u>WR</u> , <u>CS</u> = 0 V T <sub>A</sub> = +25°C	V <sub>DD</sub> = +5 V	4	All		70	pF
			V <sub>DD</sub> = +15 V	4	All		70	
Output capacitance	C <sub>OUT2</sub>	DB0 to DB11 <u>4/</u> = V <sub>DD</sub> <u>WR</u> , <u>CS</u> = 0 V T <sub>A</sub> = +25°C	V <sub>DD</sub> = +5 V	4	All		200	pF
			V <sub>DD</sub> = +15 V	4	All		200	
Chip select to write setup time	t <sub>CS</sub>	<u>7/</u>	V <sub>DD</sub> = +5 V	9,10,11	01,02 03,04	170		ns
					05,06 07	280		
			V <sub>DD</sub> = +15 V	9,10,11	01,02 03,04	95		
					05,06 07	180		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified <u>1/</u>	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Chip select to write hold time	t <sub>CH</sub>	<u>2/</u>	V <sub>DD</sub> = +5 V	9,10,11	All	0	ns
			V <sub>DD</sub> = +15 V	9,10,11	All	0	
Write pulse width	t <sub>WR</sub>	t <sub>CS</sub> ≥ t <sub>WR</sub> , t <sub>CH</sub> ≥ 0	V <sub>DD</sub> = +5 V	9,10,11	01,02 03,04	170	ns
					05,06 07	250	
		<u>2/</u>	V <sub>DD</sub> = +15 V	9,10,11	01,02 03,04	95	
				05,06 07	160		
Data setup time	t <sub>DS</sub>	<u>2/</u>	V <sub>DD</sub> = +5 V	9,10,11	ALL	150	ns
			V <sub>DD</sub> = +15 V	9,10,11	01,02 03,04	80	
					05,06 07	100	
Data hold time	t <sub>DH</sub>	<u>2/</u>	V <sub>DD</sub> = +5 V	9,10,11	01,02 03,04	5	ns
					05,06 07	10	
			V <sub>DD</sub> = +15 V	9,10,11	01,02 03,04	5	
					05,06 07	10	

1/ V<sub>OUT1</sub> = 0 V, V<sub>REF</sub> = +10 V, AGND = DGND, unless otherwise specified.

2/ See 4.3.1c.

3/ Measured using internal feedback resistor and includes effect of 5 ppm maximum gain T<sub>C</sub>.

4/ These parameters may be guaranteed, if not tested, to the limits specified in table I herein.

5/ Feedthrough error can be reduced by connecting the metal lid to ground.

6/ Subgroup 4 (C<sub>IN</sub> measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance.

7/ Timing in accordance with figure 4.

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Device types	01 through 07	
Case outlines	R	2
Terminal number	Terminal symbol	
1	OUT1	OUT1
2	AGND	AGND
3	DGND	DGND
4	DB11(MSB)	DB11(MSB)
5	DB10	DB10
6	DB9	DB9
7	DB8	DB8
8	DB7	DB7
9	DB6	DB6
10	DB5	DB5
11	DB4	DB4
12	DB3	DB3
13	DB2	DB2
14	DB1	DB1
15	DB0(LSB)	DB0(LSB)
16	$\overline{\text{CS}}$	$\overline{\text{CS}}$
17	$\overline{\text{WR}}$	$\overline{\text{WR}}$
18	V <sub>DD</sub>	V <sub>DD</sub>
19	V <sub>REF</sub>	V <sub>REF</sub>
20	RFB	RFB

FIGURE 1. Terminal connections.

<b>STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	SIZE <b>A</b>		<b>5962-87702</b>
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Write mode:

$\overline{CS}$  and  $\overline{WR}$  low, DAC responds to data bus (DB0 to DB11) inputs.

Hold mode:

Either  $\overline{CS}$  or  $\overline{WR}$  high, data bus (DB0 to DB11) is locked out; DAC holds last data present when  $\overline{WR}$  or  $\overline{CS}$  assumed high state.

FIGURE 2. Mode selection.

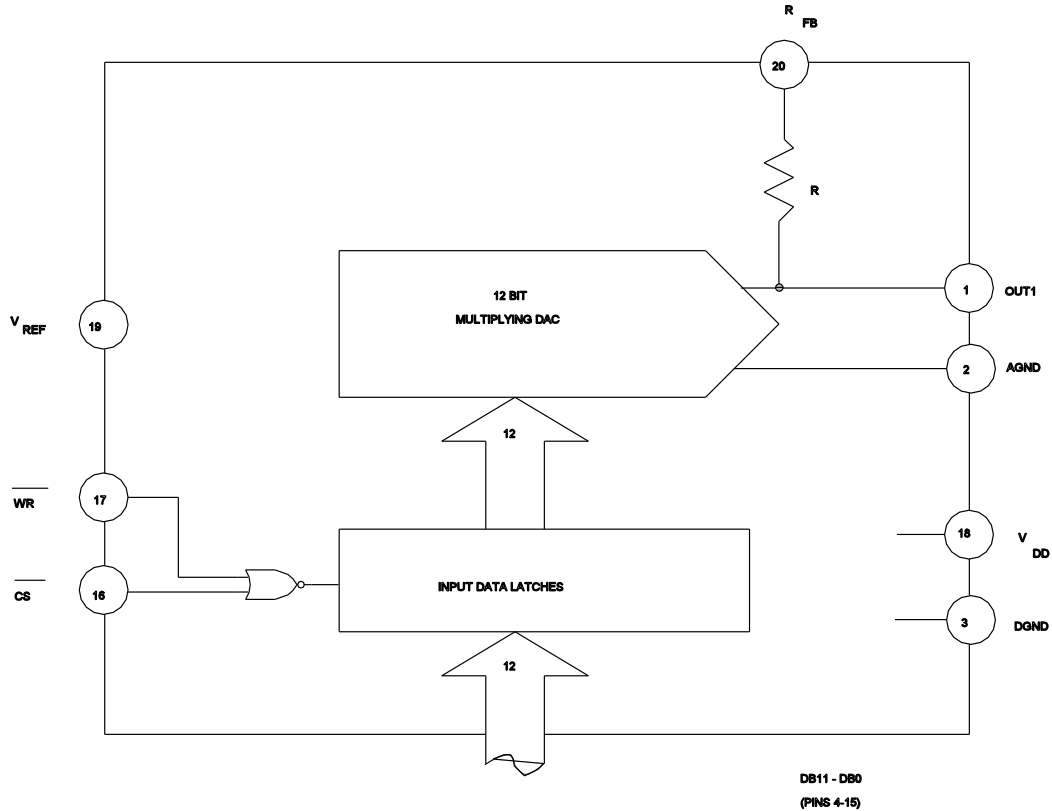


FIGURE 3. Logic diagram.

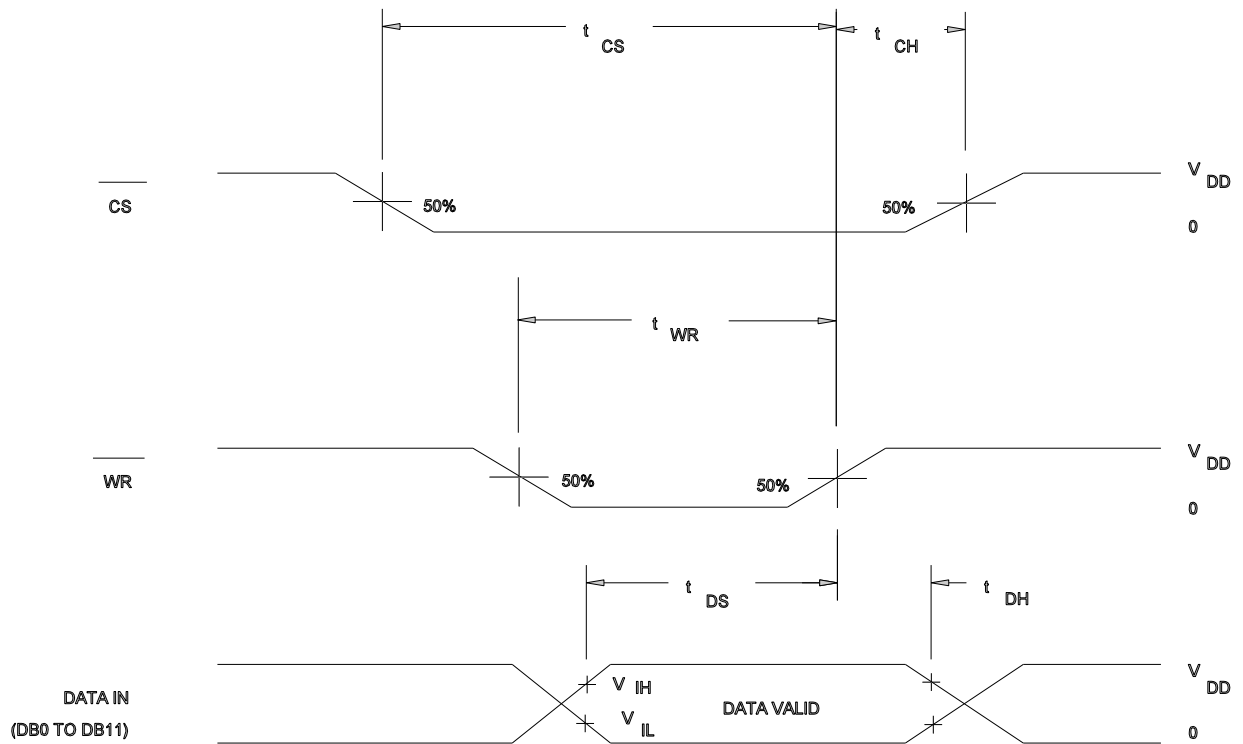
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NOTES:

$V_{DD} = +5 \text{ V}; t_r = t_f = 20 \text{ ns}$

$V_{DD} = +15 \text{ V}; t_r = t_f = 40 \text{ ns}$

All input signal rise and fall times measured from 10 to 90 percent of  $V_{DD}$ .

Timing measurement reference level is  $(V_{IH} + V_{IL})/2$ .

FIGURE 4. Write cycle timing diagram.

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3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2)  $T_A = +125^\circ\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. Optional subgroup 12 is used for grading and part selection at  $+25^\circ\text{C}$ . It is not included in PDA.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,12
Group A test requirements (method 5005)	1,2,3,4,5,6, 9**,10***,11***,12
Groups C and D end-point electrical parameters (method 5005)	1

\* PDA applies to subgroup 1.

\*\* Subgroup 9, if not tested, shall be guaranteed to the specified limits in table I for device type 07.

\*\*\* Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

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4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Optional subgroup 12 is used for grading and part selection at +25°C.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883:
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
  - (2)  $T_A = +125^\circ\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for original equipment manufacturer application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 93-01-22

Approved sources of supply for SMD 5962-87702 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1</u> /
5962-8770201RX	24355 1ES66	AD7545SQ/883B MX7545SQ/883B
5962-87702012X	24355 1ES66	AD7545SE/883B MX7545SE/883B
5962-8770202RX	24355 1ES66	AD7545TQ/883B MX7545TQ/883B
5962-87702022X	24355 1ES66	AD7545TE/883B MX7545TE/883B
5962-8770203RX	24355 1ES66	AD7545UQ/883B MX7545UQ/883B
5962-87702032X	24355 1ES66	AD7545UE/883B MX7545UE/883B
5962-8770204RX	24355	AD7545GUQ/883B
5962-87702042X	24355	AD7545GUE/883B
5962-8770205RX	06665	PM7545BR/883
5962-87702052X	06665	PM7545BRC/883
5962-8770206RX	06665	PM7545AR/883
5962-87702062X	06665	PM7545ARC/883
5962-8770207RX	54186	MP7545SD/883

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN - Continued.

<u>Vendor CAGE number</u>	<u>Vendor name and address</u>
06665	Analog Devices Precision Monolithics Division 1500 Space Park Drive P O Box 58020 Santa Clara, CA 95050-8020
1ES66	Maxim Integrated Products, Inc. 120 San Gabriel Drive Sunnyvale, CA 94086-5126
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062-9106 Point of contact: 181 Ballardvale Street Wilmington, MA 01887-1024
54186	Micro Power Systems 3151 Jay Street Santa Clara, CA 95054-0965

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.