Fundusze Europejskie
Wiedza Edukacja Rozwój

Unia Europejska
Europejski Fundusz Społeczny

Politechnika Śląska jako Centrum Nowoczesnego Kształcenia
opartego o badania i innowacje

POWR-03.05.00-00-Z098/17-00

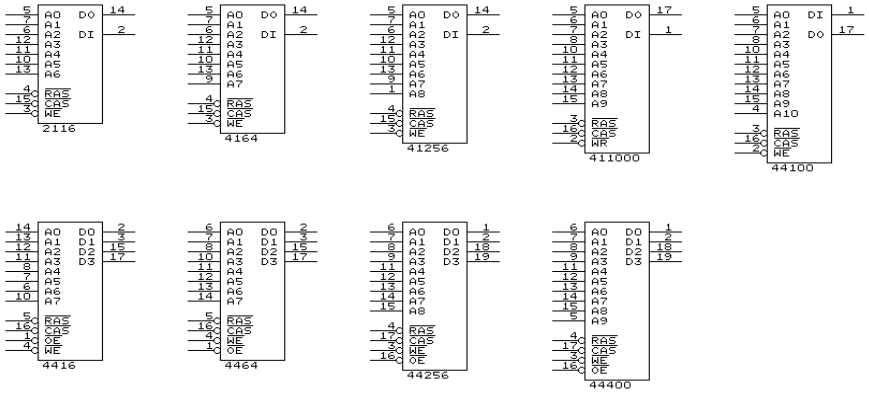
Microprocessor and Embedded Systems

Faculty of Automatic Control, Electronics and Computer Science / Informatics, Engineer Degree, sem. 4

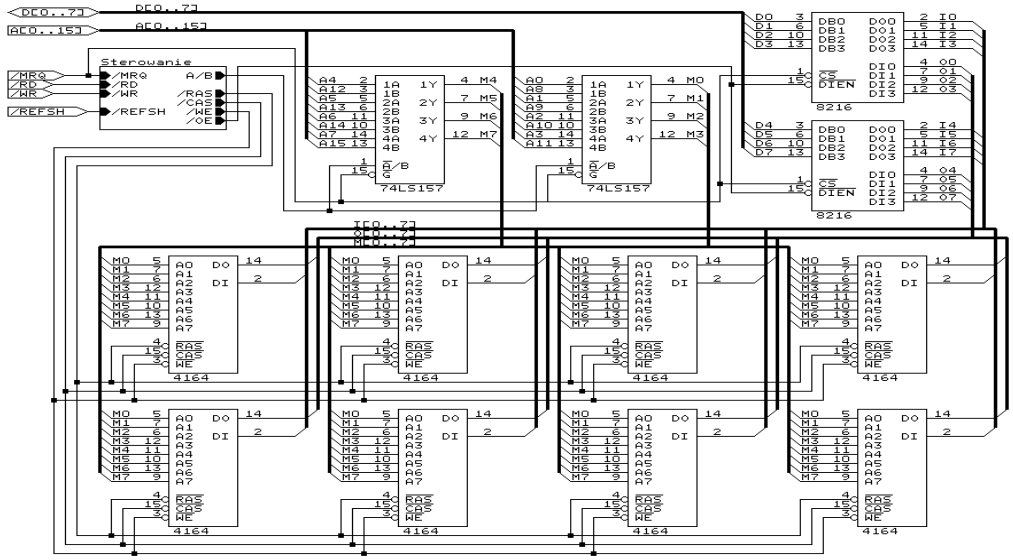
Materiały dydaktyczne współfinansowane przez Unię Europejską ze środków Europejskiego Funduszu Społecznego

Classes 5 – DRAM memories (part 1)

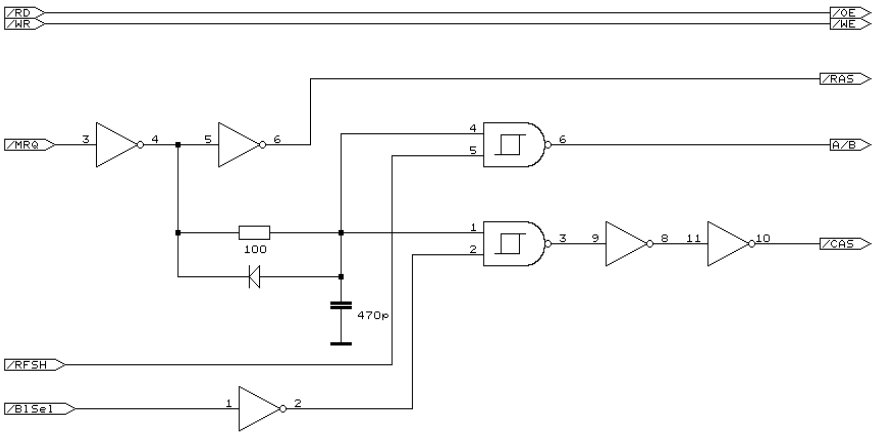
Selected DRAM memory pinout



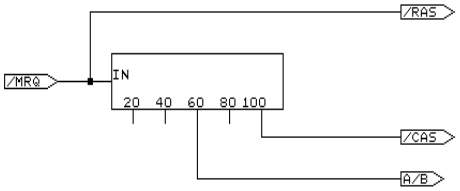
Example 1



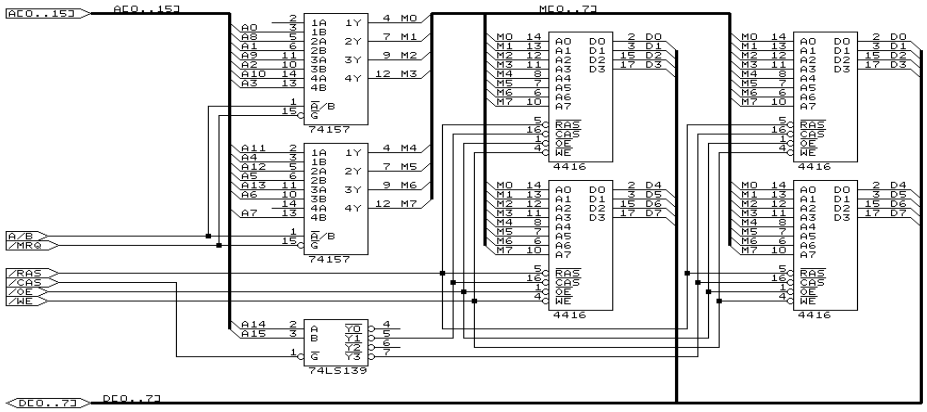
Control unit for ex. 1 – gates version



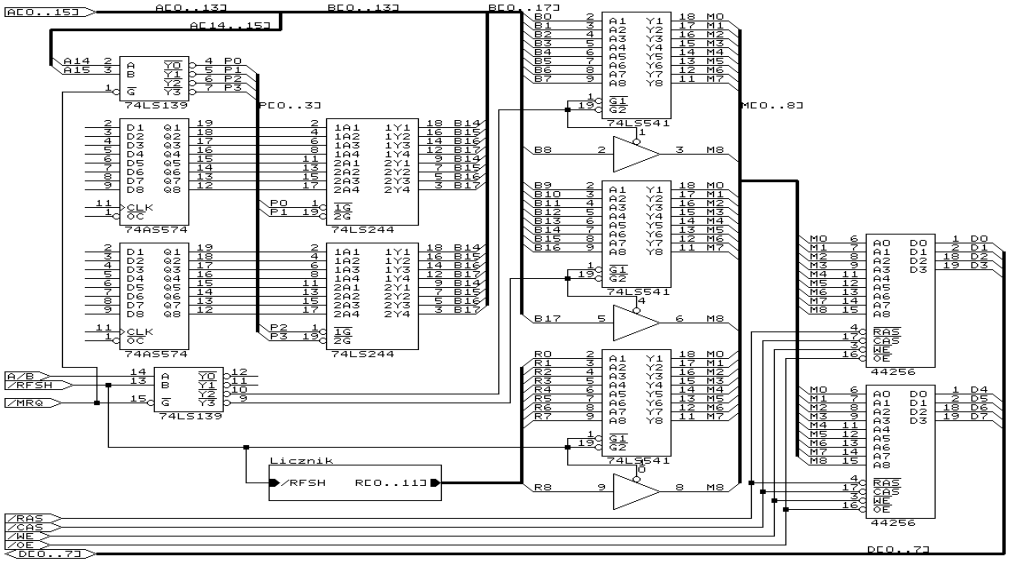
Control unit for ex. 1 – delay line version



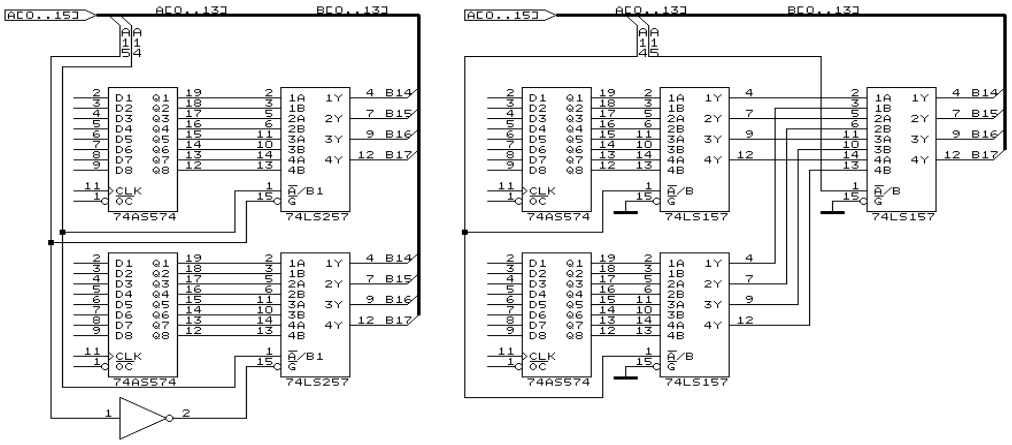
Example 2



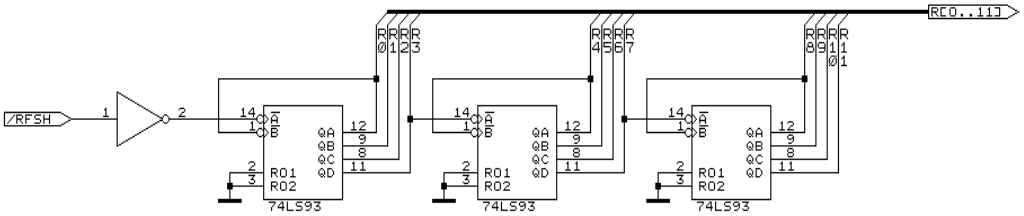
Example 3



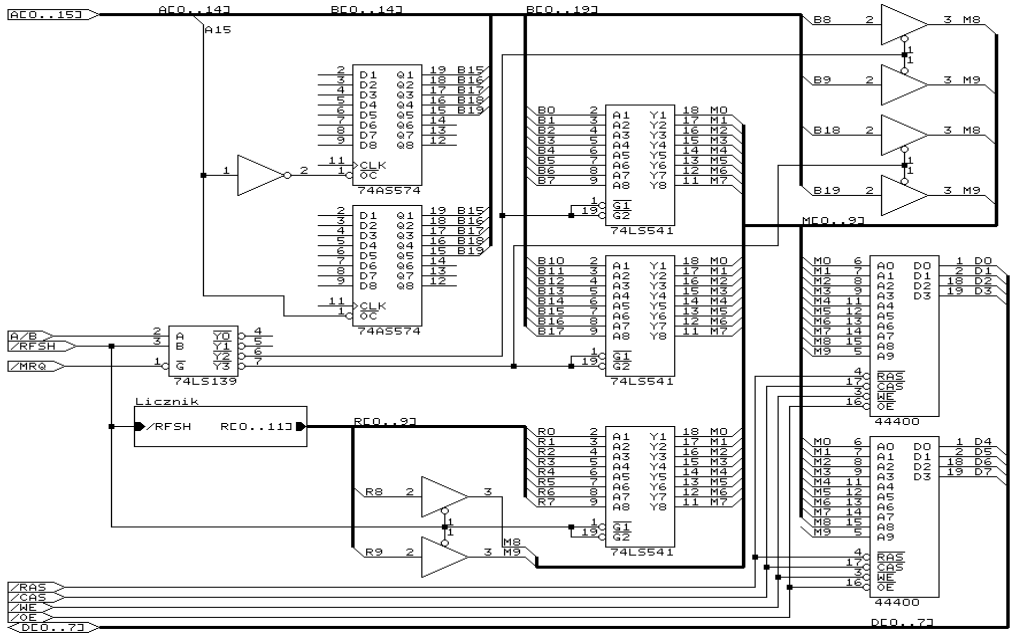
Alternative paging units for ex. 3



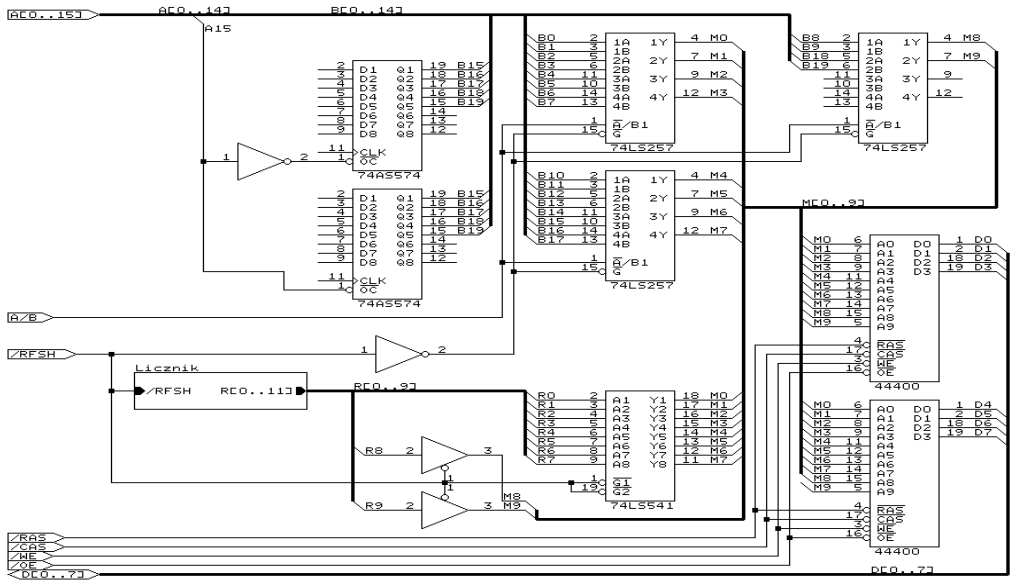
Refresh counter for ex. 3



Example 4

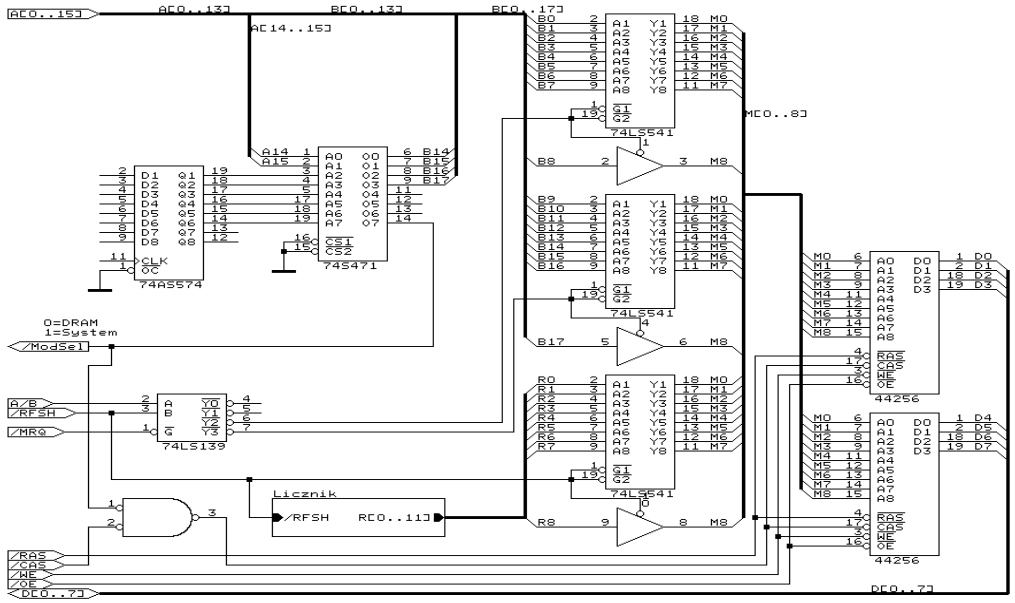


Example 5 - alternative solution



Example 5

Address	Mode 0	Mode 1	Mode 2	Mode 3
0000-3FFF$_h$	„system”	„system”	page 0	page 0
4000-7FFF$_h$	page 0	page 2	page 2	page 1
8000-BFFF$_h$	page 1	page 3	page 3	page 2
C000-FFFF$_h$	„system”	„system”	„system”	page 3



PROM memory content for e

Mode A_7-A_2	Address A_1-A_0	Page D_3-D_0	$\overline{\text{ModSel}}$ D_7	
000000	00	dowolny	1	
	01	0000	0	
	10	0001	0	
	11	dowolny	1	
000001	00	dowolny	1	
	01	0010	0	
	10	0011	0	
	11	dowolny	1	
000010	00	0000	0	
	01	0010	0	
	10	0011	0	
	11	dowolny	1	
000011	00	0000	0	
	01	0001	0	
	10	0010	0	
	11	0011	0	

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