



Fundusze Europejskie
Wiedza Edukacja Rozwój



**Rzeczpospolita
Polska**

Unia Europejska
Europejski Fundusz Społeczny



**Politechnika Śląska jako Centrum Nowoczesnego Kształcenia
opartego o badania i innowacje**

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Microprocessor and Embedded Systems

**Faculty of Automatic Control, Electronics and Computer Science,
Informatics, Bachelor Degree**

Lecture 15

Memory addressing extensions

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Memory addressing extensions

Program:

- Page Size Extension
- Physical Address Extension

Memory addressing extensions

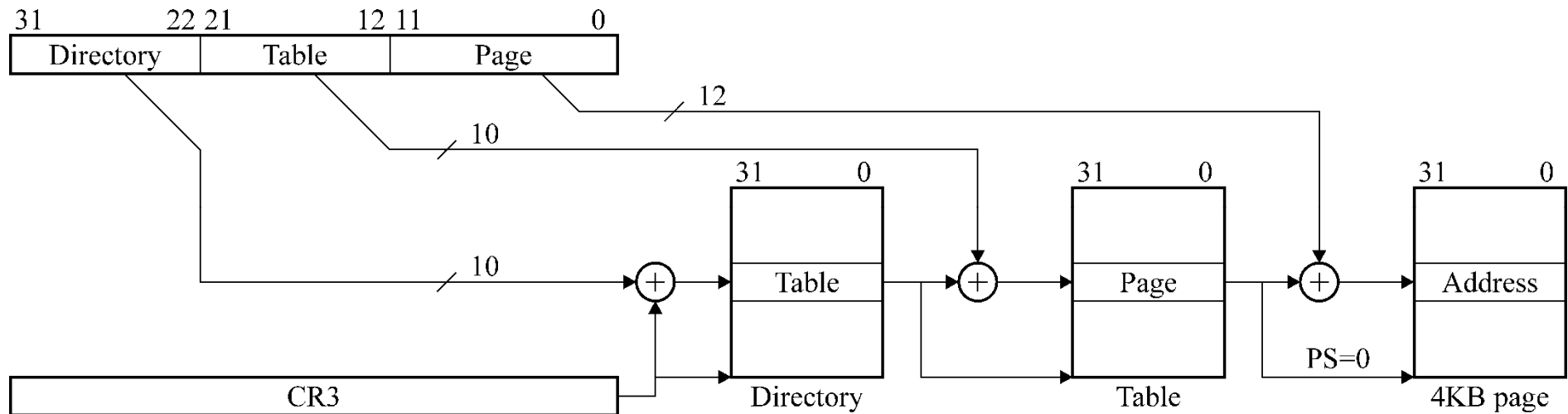
- PAE – Physical Address Extension
 - From Pentium Pro and Athlon
 - 3 levels page table hierarchy
 - 64-b table entries
 - Direct access to over 4GB
 - In x86-64 Long mode further extends to 4 levels
 - Visible in a μp that has separate address bus
 - A0..A35 \rightarrow 64 GB total memory
 - Less apparent for HT or QPI-equipped μp 's

Memory addressing extensions

- PSE – Page Size Extension
 - Reduces system performance decrease when using „small” (4KB) pages
 - E.g., 1MB memory
 - 256 pages
 - TLB entirely filled
 - With PSE, 1MB = 1 page
 - Only one TLB entry needed
 - *But internal fragmentation appears*

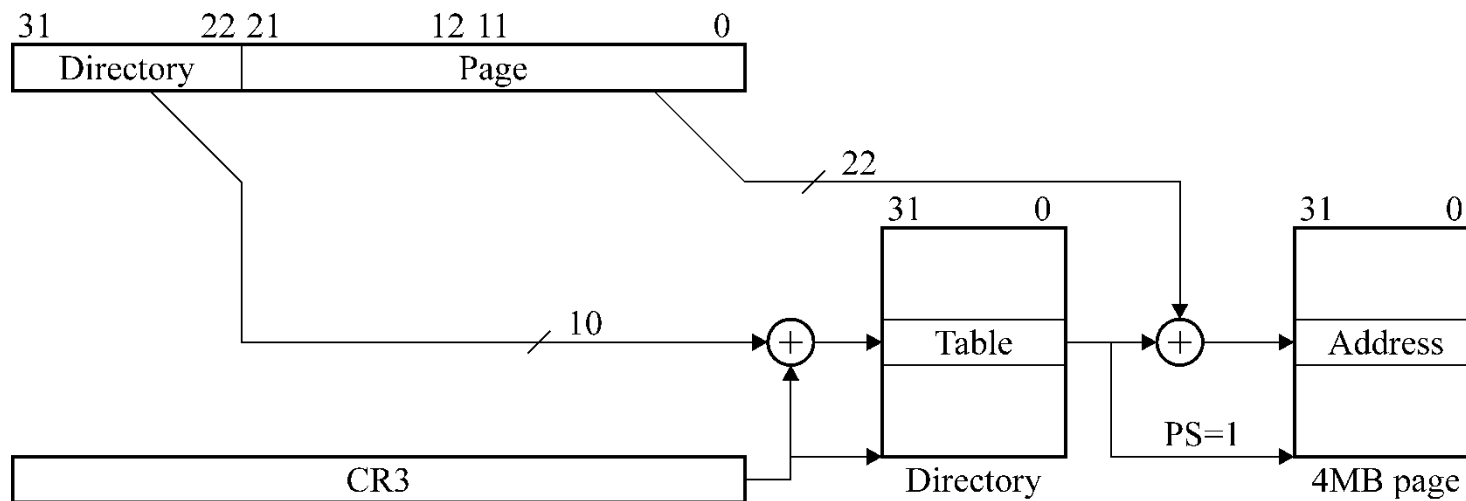
Memory addressing extensions

- PAE – Physical Address Extension
 - No PAE, 4KB page (as in 486)



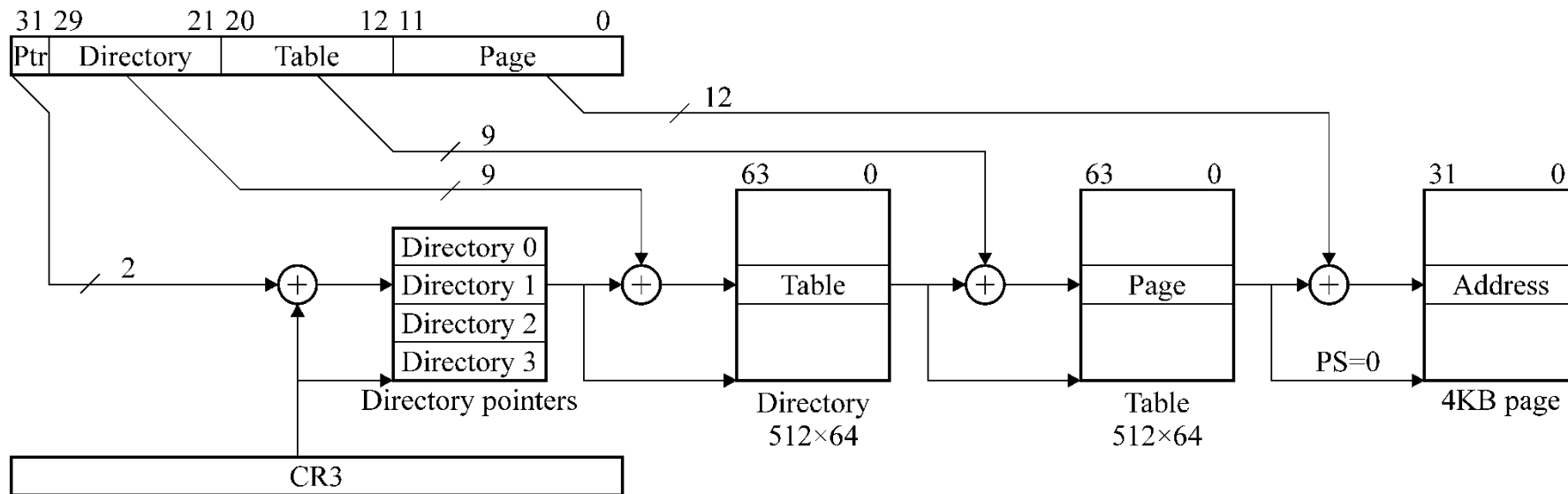
Memory addressing extensions

- PAE – Physical Address Extension
 - No PAE, 4MB page (PSE – Page Size Ext.)



Memory addressing extensions

- PAE – Physical Address Extension
 - PAE, 4KB page



Memory addressing extensions

- PAE – Physical Address Extension
 - PAE, 2MB page

