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Microprocessor and Embedded Systems

Faculty of Automatic Control, Electronics and Computer Science, Informatics, Bachelor Degree

Lecture 10

64-bit microprocessors
AMD Athlon 64

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Athlon 64

Program:

- Genesis of 64-b processors
- AMD Athlon
  - Main properties
  - Structure
  - Operating modes
- HyperTransport bus
  - System architecture
  - Signalling
  - Data packet communication

Athlon 64

- Genesis of 64-b processing
  - Goal:
    - µp for highly efficient workstations and servers
  - Two ways:
    - AMD: evolution
      - Extension of x86 architecture
    - Intel: revolution
      - Completely new (but interesting) architecture

Athlon 64

- Discussion on AMD approach
  - µp for highly efficient workstations and servers
    - In a simplified form – for „usual” PCs
  - Assumptions
    - x86 has limitations, but proper development can remove or omit them
    - Backward compatibility with hard- and software is a great advantage
    - Existing code should be executed with maximum possible performance (no 64-b programs)
    - A typical user may need 64-b PC to efficiently manage memory >4 GB

Athlon 64

- Discussion on Intel approach
  - µp for highly efficient workstations and servers
  - Assumptions
    - x86 has limitations
      - Backward compatibility complicates µp structure and operation
      - Backward compatibility makes modifications difficult
    - Highly efficient µp don't have to execute existing code with maximum performance
      - There will be optimised code for 64-b µp's
    - Typical user does not need 64-b processing

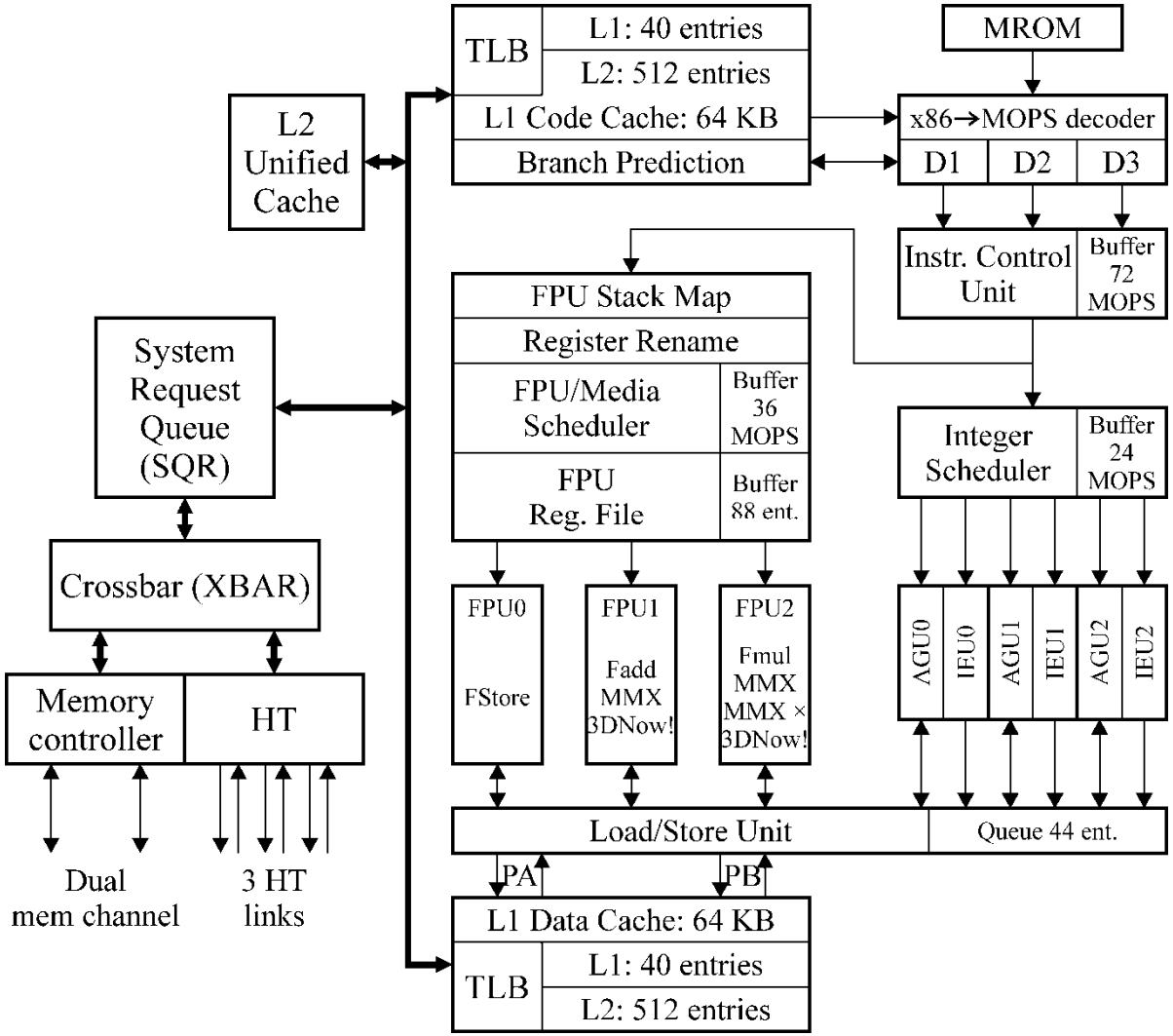
  → *IA-64 does not even resemble x86*

Athlon 64

- Athlon 64 – main properties
  - Structure similar to 32-b Athlon
  - Built-in DDRAM controller
  - HyperTransport bus
  - 64-b operating modes
  - x86 registers extended to 64 bits
    - Number of registers doubled

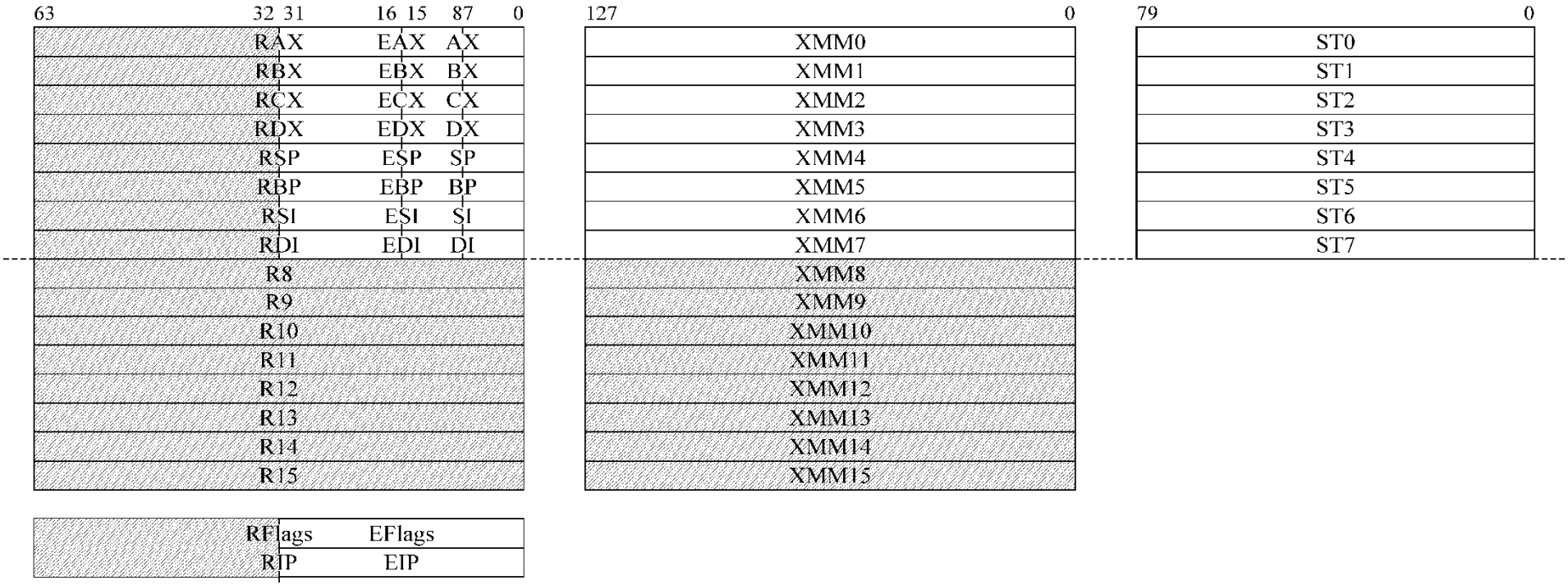
Athlon 64

- Athlon 64 – block diagram



Athlon 64

- Athlon 64 – registers



Athlon 64

- Athlon 64 – operating modes
  - Legacy – for 32-b OS
    - Typical x86, full-compatible with 32b, 16b apps
    - No 64-b extensions
  - LongMode – for 64-b OS
    - 64-b
      - for 64-b apps
      - 64-b processing
      - 64-b registers
    - Compatibility
      - 32/16-b apps, no recompile necessary
      - No 64-b extensions

Athlon 64

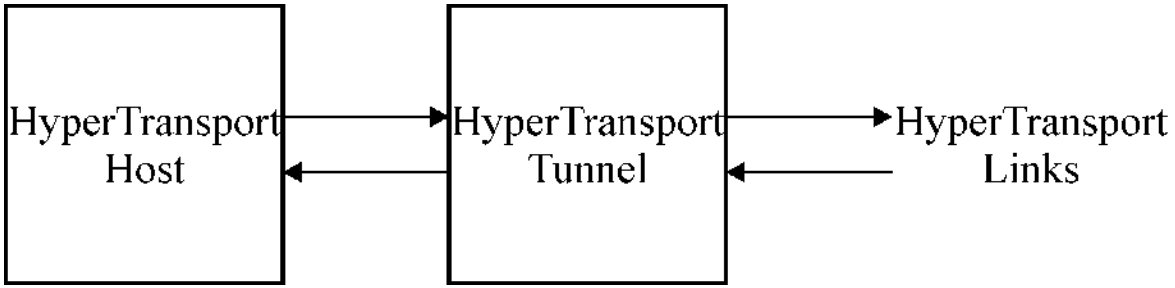
- Athlon 64 – main properties
  - Built-in DDRAM controller
    - Shorter delays (80 vs. 160 ns in NorthBridge)
      - Higher throughput for random access
    - Single (4 GB) or double (8 GB) channel
    - 2.48 GBps/channel
    - DDR support
    - Less flexibility of memory selection
      - Future upgrade to DDR2 support
      - Memory access via NorthBridge still possible

Athlon 64

- Athlon 64 – main properties
  - HyperTransport bus
    - Open standard (opposite to Intel FSB)
    - Serial, bi-dir, point-to-point links
    - LVDS (Low Voltage Differential Signalling) 1.2V
    - 400M to 2.8G transfers/s
    - Data link 2, 4, 8, 16, 32 bits, can be asymetrical
    - Up to 22.4 GBps
    - Packet: 4..64 B payload, 8..12 B header
    - Can cooperate with PCI, PCI-X, PCI-Express

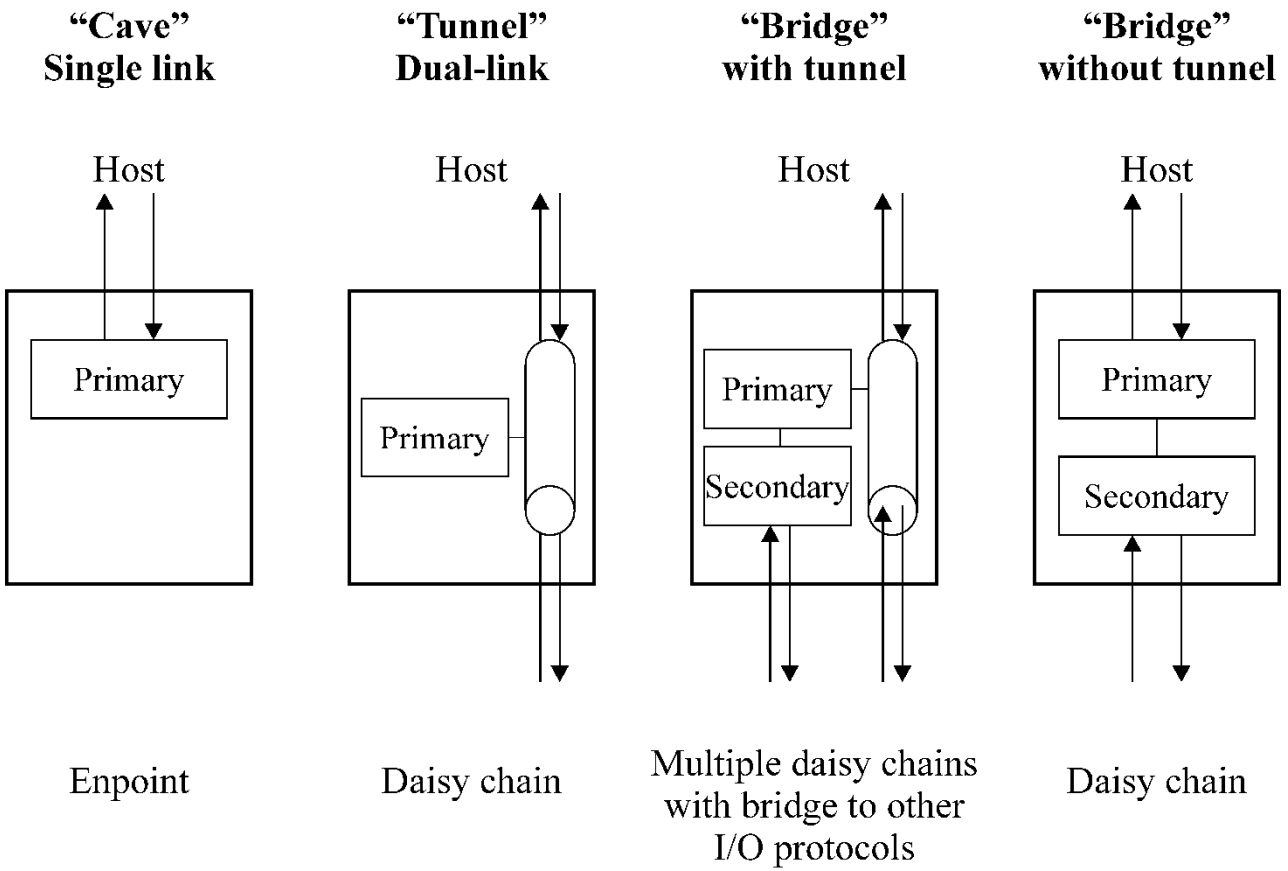
Athlon 64

- HyperTransport Bus
  - General architecture



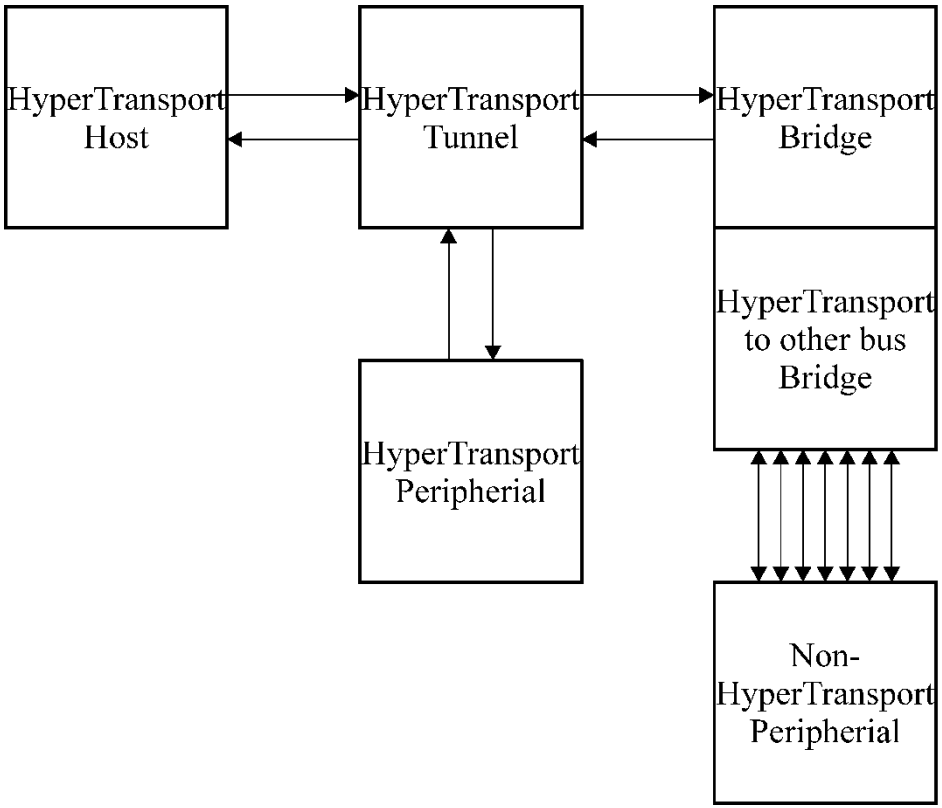
Athlon 64

- HyperTransport Bus
  - I/O device configurations



Athlon 64

- HyperTransport Bus
  - System example
    - Cooperation with PCI, PCI-X, PCI Express possible



Athlon 64

- HyperTransport Bus
  - Link
    - Data path: 2, 4, 8, 16 or 32 bits
    - Clock
    - Control line
    - Each signal = twin wire lines
  - Signals
    - CAD (command, address, data)
    - CLK – one per 8 CAD bits
      - 2×, 4×, 8× – only 1 CLK
    - CTL – control (1=control, 0=data)
    - Reset, PWROK

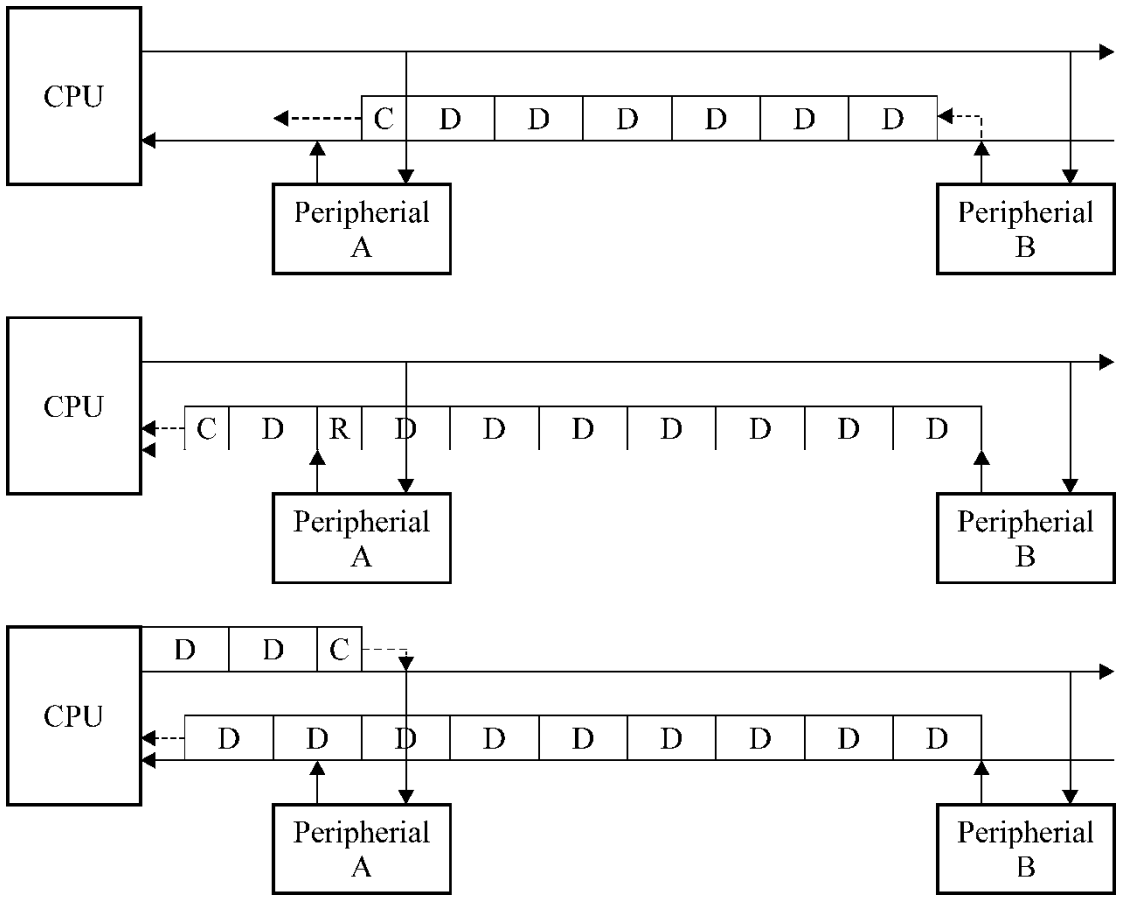
Athlon 64

- HyperTransport Bus
  - Packet format
    - Control – 4 or 8 B
    - Data – 4..64 B

    - Low latency (low overhead)
      - E.g., PCI-Express:
        - » 12-16 B transaction layer
        - » 8 B data link layer
        - » 8b/10b encoding (20%) physical layer

Athlon 64

- HyperTransport Bus
  - Priority Request Interleaving
    - Request packet insertet into ongoing data stream



Athlon 64

- HyperTransport Bus
  - Example PC structure