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Microprocessor and Embedded Systems

Faculty of Automatic Control, Electronics and Computer Science, Informatics, Bachelor Degree

Lecture 10

Advanced 32-bit microprocessors

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Advanced 32-b…

Program:

- AMD Athlon
  - Structure
  - Pipeline details
- Intel Pentium 4
  - Main properties
- SSE extensions
- Hyper-Threading

Advanced 32-b…

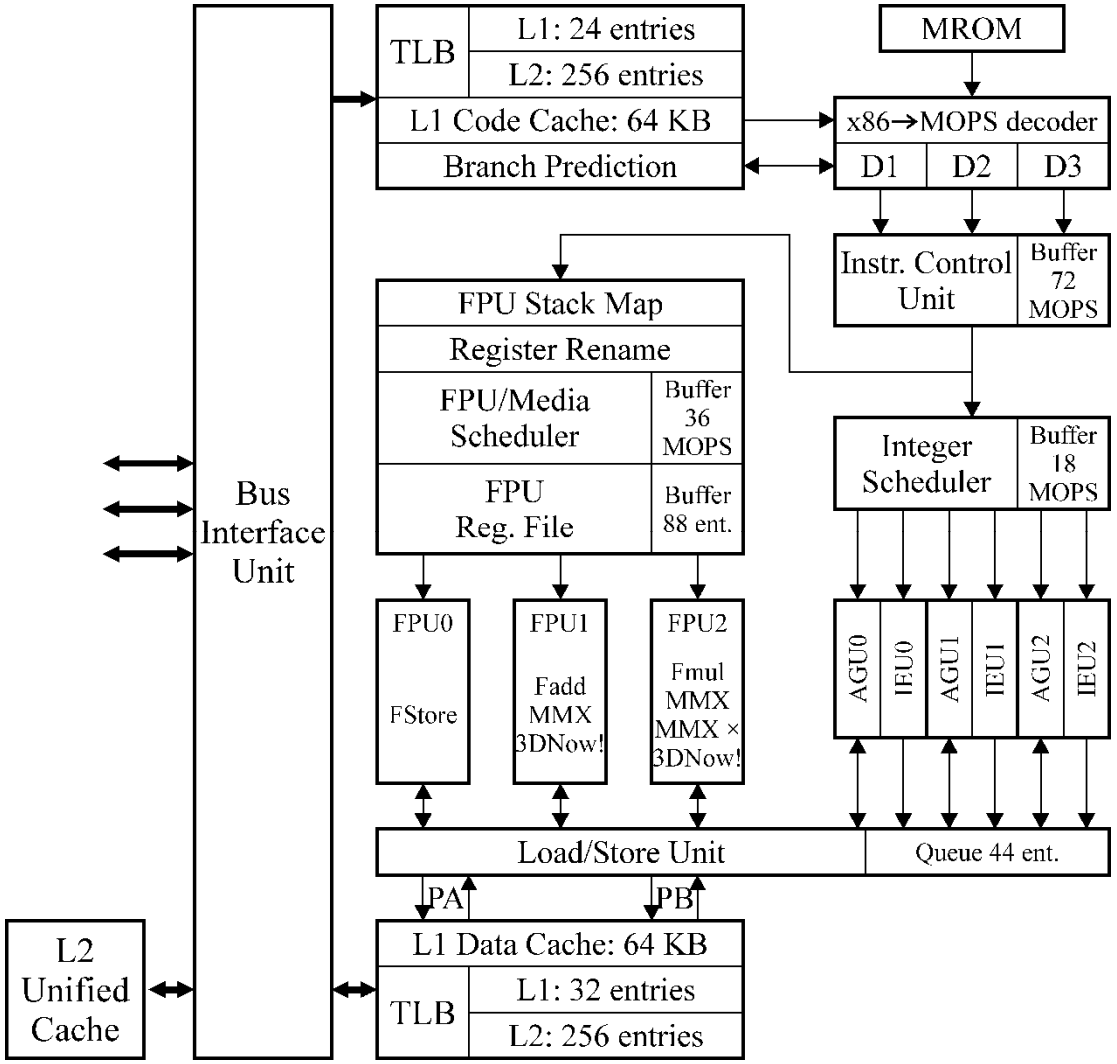
- AMD Athlon
  - 9 execution units
    - 3 integer
    - 3 address
    - 3 floating-point
  - Out-of-order
    - MMX, FPU and 3DNow! Interleaved
  - 3 universal decoders
    - x86 → MOPS
    - Command ≤ 15B → Direct Path
    - Command > 15B → Vector Path + MacroCode ROM

Advanced 32-b…

- AMD Athlon
  - Pipelines
    - Integer 10/FPU 15 stages (1-6 common)
  - BTB 2048 entries
  - EV-6 Bus
    - From DEC Alpha µp
    - Up to 200 MHz
    - 64-b data + 8-b ECC
  - Exclusive Cache
    - Data in L1 deleted from L2

Advanced 32-b…

- AMD Athlon – structure

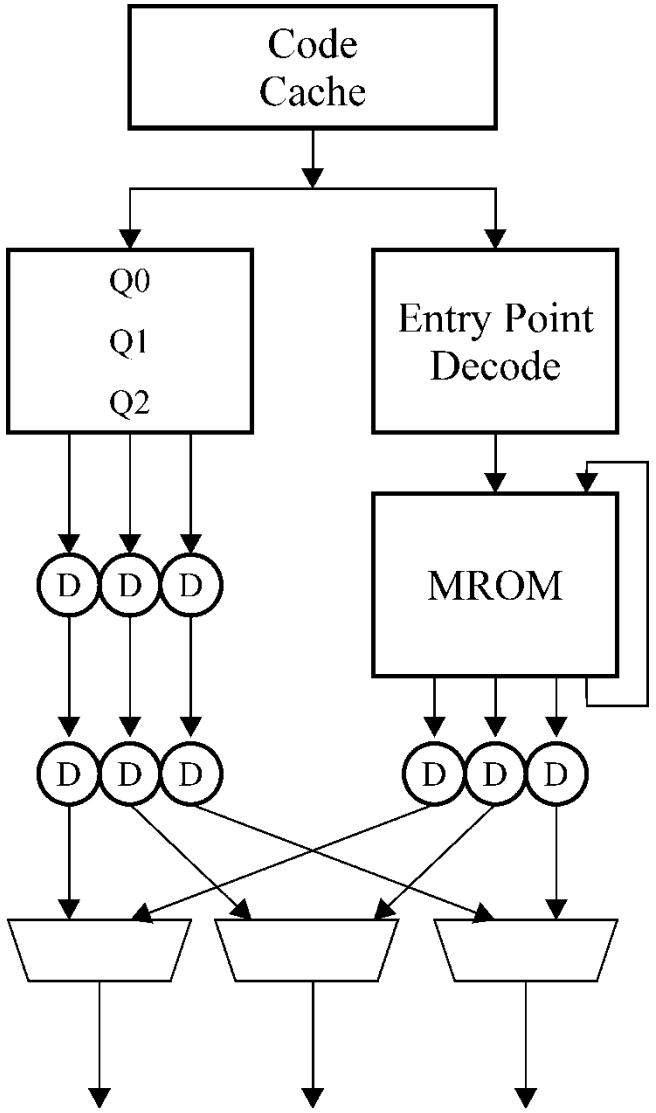


Advanced 32-b…

- AMD Athlon – pipeline
  - Decoder instr→MacroOP
    - Constant length, ≥Ops
    - 3 MOPs/clk
    - Direct Path
      - Instr → 1 MOP → 1..2 Ops
      - Max 3 instr/8 B
      - Fetched in 16B units → max. 6 instr. enters Direct Path
    - Vector Path
      - Instr ≥2 MOPs
      - MacroCode ROM used
      - Max 3 MOPs/clk

Advanced 32-b…

- AMD Athlon – decoding
  - Fetch
  - Scan
  - Align1/MECtl
    - Microcode Engine Control
  - Align2/MEROM
    - Microcode Engine ROM
  - EDEC/MEDEC
    - Microcode Eng./Early Decode
  - IDEC/Rename



Advanced 32-b…

- AMD Athlon – decoding

Stage	Direct Path	Vector Path
Fetch	Next fetch address calc	
Scan	Find instr beg/end; ≤6 → DP, ≤1 → VP	
Align1/MECtl	≤9 inst. Buffering; 3 inst. → Align2	MROM entry point generation
Align2/MEROM	Decoding	MROM indexing by entry point
EDEC/MEDEC	MOPs sequence generation	
IDEC/Rename	DP/VP MOPs selection → goto ICU	

Advanced 32-b…

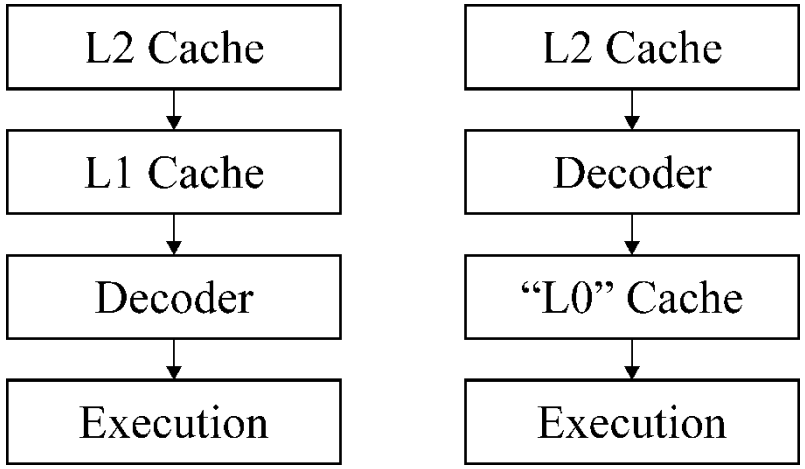
- AMD Athlon – ALU pipe
  - Sched
    - MOPs buffering; MOPs operands collection
  - Exec
    - Execution → ALU, AGU
  - AddrGen
    - Linear address calculation
  - DCAcc
    - Data Cache & TLB access
    - If MOP needs data → goto Exec
  - Response
    - Data Cache hit/miss report

Advanced 32-b…

- AMD Athlon – FPU pipe
  - StkRen
    - StackRename – FPU register renaming
  - Register Rename
  - SchedWrite
  - Sched
    - MOP execution planning; FPU regs read
  - Freg
    - FPU regs read
  - FExec 1..4
    - 3 logical FPU pipes (FAdd, FMul, FStore)

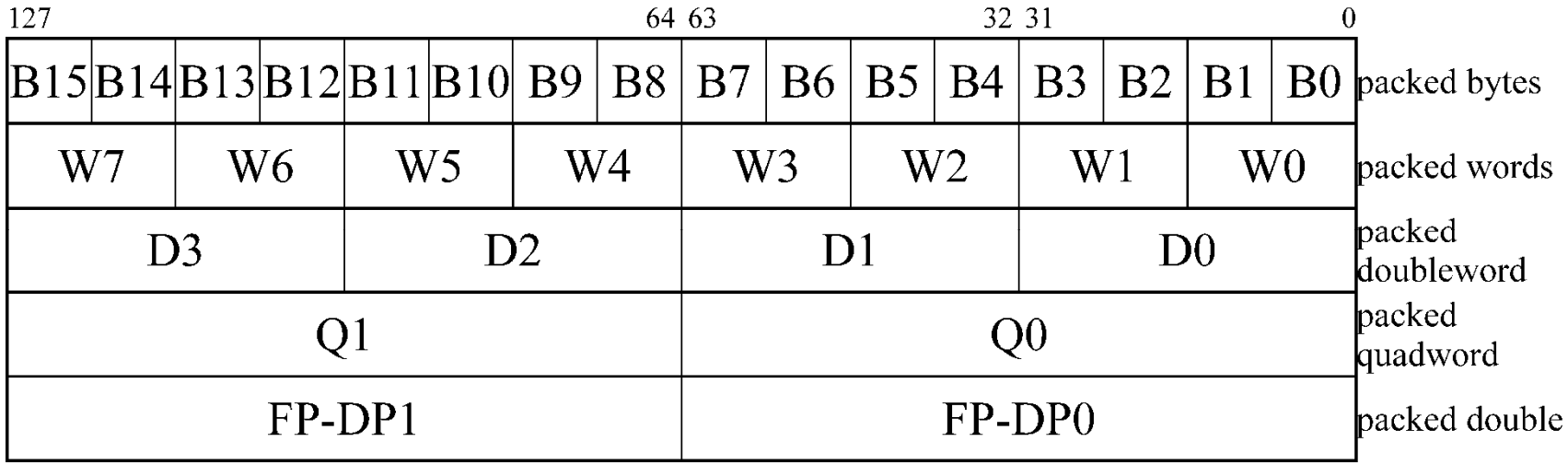
Advanced 32-b…

- Intel Pentium 4
  - Execution Trace Cache
    - Stores decoded µops, not commands
    - No need to decode instr. multiple times
    - Capacity: 12/16/32 kµops (from cpuid description)
      - Equivalent of abt. 32-64 KB L1 (according to *Anatomia PC*)



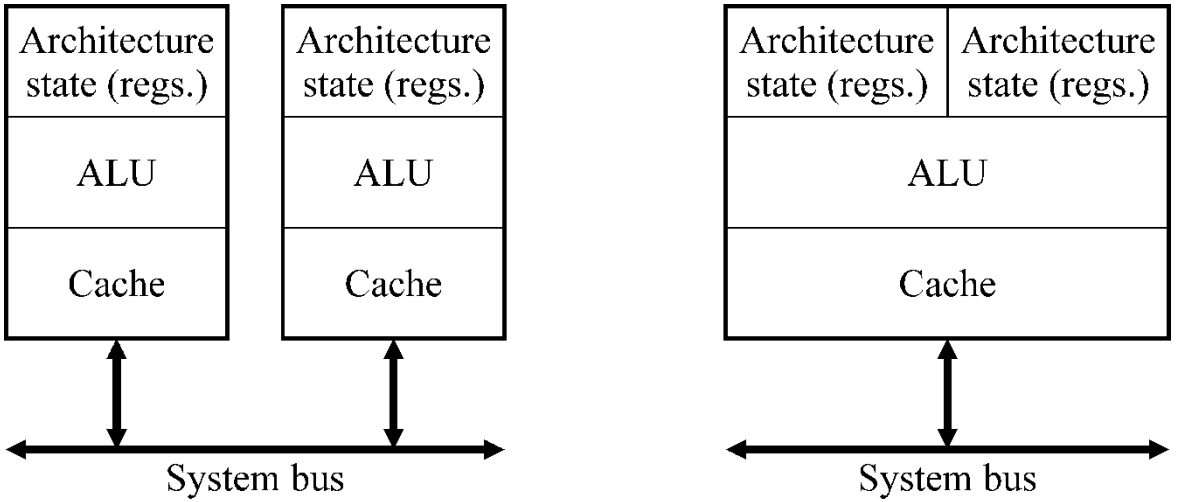
Advanced 32-b…

- SSE2 Extension
  - Uses SSE registers: $XMM_{0..127}$
  - New data types



Advanced 32-b…

- Hyper Threading
  - A kind of SMT (*Simultanous Multi-Threading*)
    - SMT: 2 physical µp's
    - HT: 1 physical µp, 2 logical µp's
    - An intermediate form between 1µp and 2µp



Advanced 32-b…

- Hyper Threading
  - Available in every Pentium 4
    - But not every can have it switched on
  - HT occupies abt. 5% semiconductor
    - Few tens % higher performance
  - Goal: higher utilisation of existing exec. units
  - Good if multiple threads
    - If a thread stops, exec. units assigned to another thread
  - In contrast to MMX/SSE, any app can make use
    - Hard- & software must be prepared for HT
  - If optimal app, no gain