Fundusze Europejskie
Wiedza Edukacja Rozwój

Rzeczpospolita Polska

Unia Europejska
Europejski Fundusz Społeczny

Politechnika Śląska jako Centrum Nowoczesnego Kształcenia
opartego o badania i innowacje

POWR.03.05.00-IP.08-00-PZ1/17

Projekt współfinansowany przez Unię Europejską ze środków Europejskiego Funduszu Społecznego

Microprocessor and Embedded Systems

Faculty of Automatic Control, Electronics and Computer Science, Informatics, Bachelor Degree

Lecture 10

Pentium Pro

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Pentium Pro

Program:

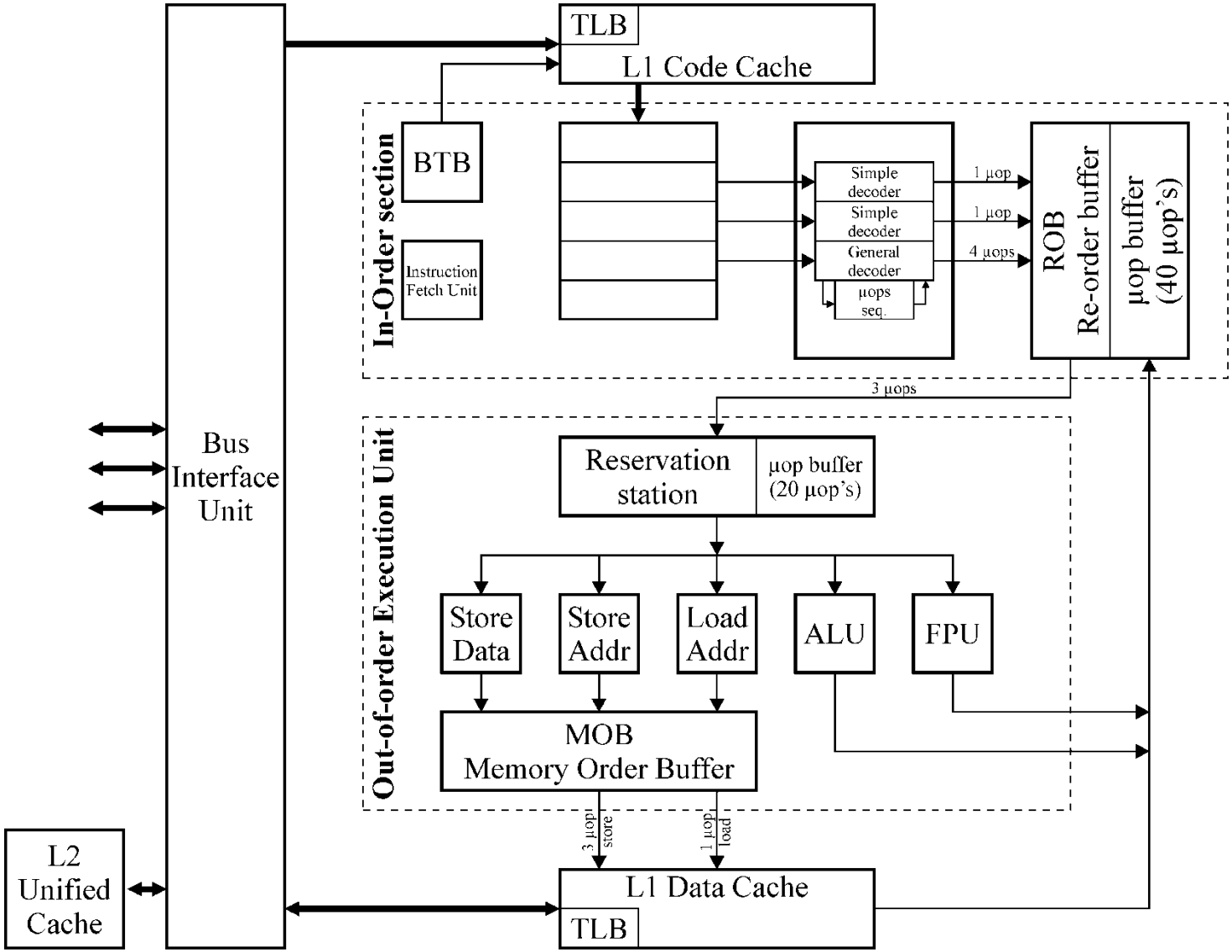
- Pentium Pro processor
  - Structure
  - Operating rules
- 3DNow! extensions
- SSE extensions
- cpuid command

Pentium Pro

- Pentium Pro procesor
  - Externally
    - *What the programmer can see*
    - Superscalar, CISC
    - Up to 3 cmd/clk
  - Internally
    - *What the programmer can't see*
    - RISC kernel
    - Instructions translated to RISC µops

Pentium Pro

- Pentium Pro – structure



Pentium Pro

- Pentium Pro – BTB
  - No jump → no delay (if good prediction)
  - Well-predicted jump → 1 clk delay, loss of what was decoded after jump command
  - Wrong prediction → min delay 9 clk, typically 10..15 clk, max 26 clk, depending on execution conditions
  - Static prediction → 5..6 clk delay
    - For jumps not described in BTB
    - Jump backward → jump (e.g., end of loop)
    - Jump forward → no jump (e.g., error)

Pentium Pro

- Pentium Pro
  - Instruction decoding – according to command order
  - 3 decoders:
    - 2 simple – for short/simple instr., e.g. mov reg, reg
    - 1 general + sequencer for long instructions
  - Up to 3 instr/clk (complex or long → <3)
    - ≤8B → simple decoder
    - ≤15B → general decoder
      - ≥9B → more clks
    - >4 µops → more clks
  - Max performance
    - 1-1-4 rule
    - Number of µops/instr given in the command list

Pentium Pro

- Pentium Pro
  - 1 µop = 118 bits (operator, src1, src2, dst)
  - Re-Order Buffer
    - Input – up to 6 µop/clk
    - „Instruction Pool” – command processing center
    - Out-of-order execution/speculative execution
    - Stores temporary results
    - Solves command dependencies (Reg. Alias Table)
    - Served µops → Reservation Station

Pentium Pro

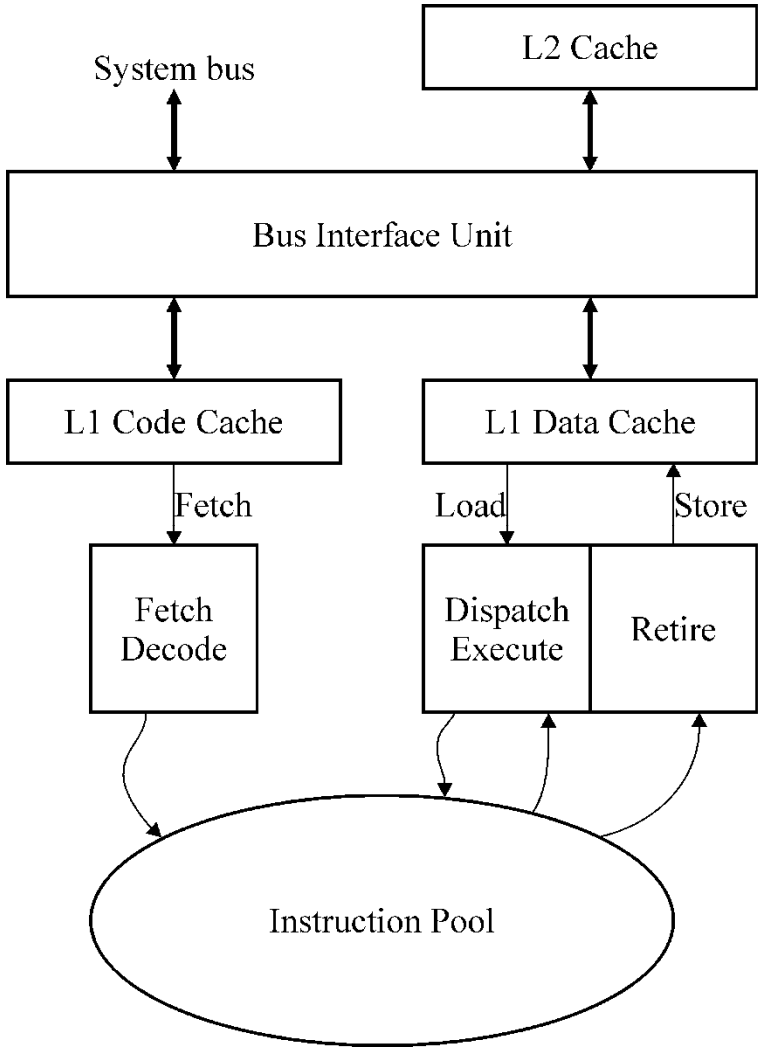
- Pentium Pro
  - Reservation Station
    - Up to 20 µops waiting for execution units
    - Ready → execution (Data Flow)
    - Execution time
      - Integer 1 clk
      - Mul 4 clk
      - Div 12-36 clk
      - FPU avg. 3..38 clk
      - Load/Store address – 1 clk

Pentium Pro

- Pentium Pro
  - Pipelines
    - Integer – 14 stages
    - FPU – 16 stages
    - No memory – 12 clk
    - Memory call +6 clk
    - Dynamic Execution
      - Program & data flow analysis to achieve optimal command execution sequence
  - Command finished – „Retirement”
    - µops removed from ROB
    - Results stored in reg/Mem

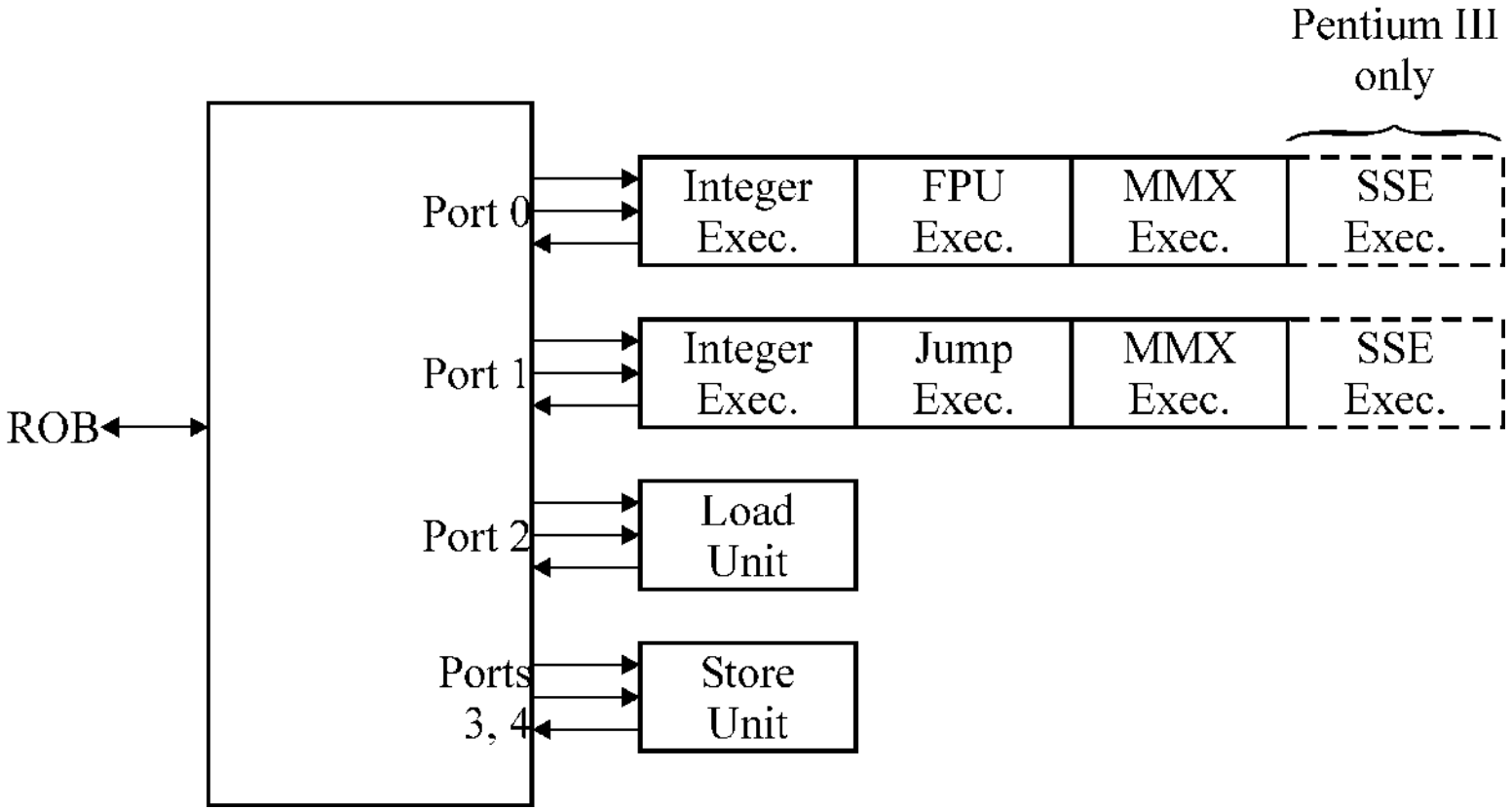
Pentium Pro

- Pentium II – simplified



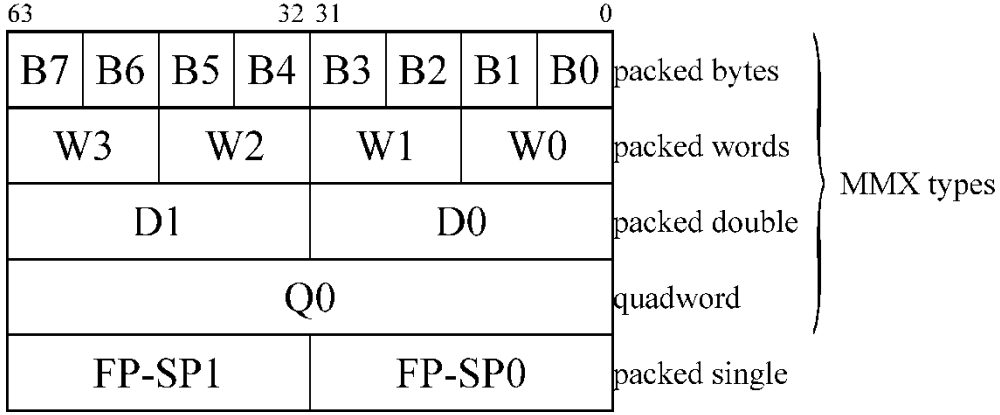
Pentium Pro

- Pentium II, III
  - Disadvantage
    - Ports 0, 1: many exec. units, only 2 ports



Pentium Pro

- 3DNow! Extension
  - Adds floating point to MMX
    - 2 single precision values in a register



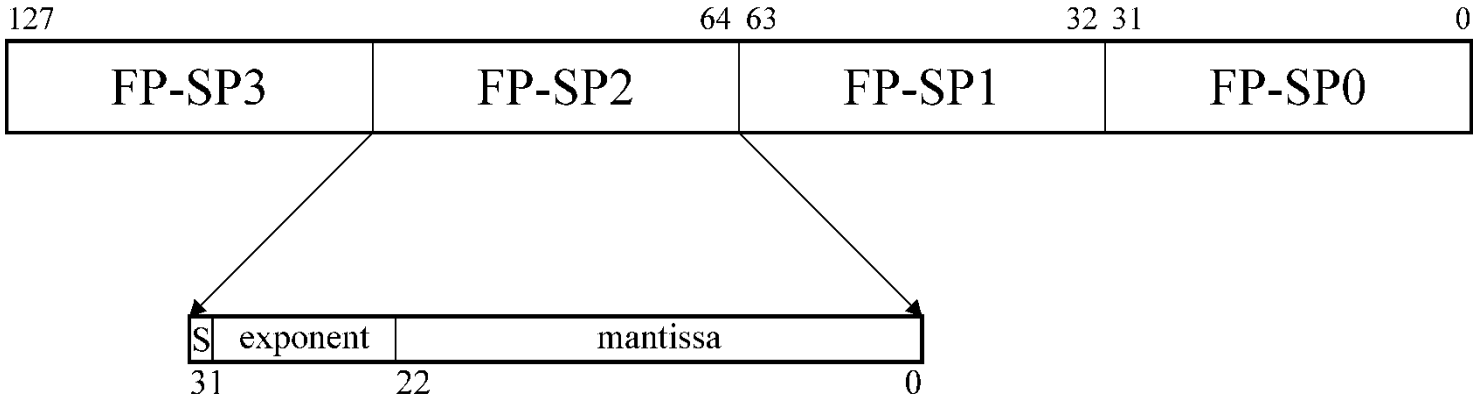
    - 21 commands
    - IEEE-754-compatible

Pentium Pro

- 3DNow! Extension
  - Pipelined execution
    - 2 pipes → up to 2 instr/clk
    - No pairing rules/limitations
    - If 2 commands in 2 pipes use the same exec. unit, 1 command may wait ≤1 clk
    - Some MMX and 3DNow! Operations executed in the same execution units

Pentium Pro

- SSE
  - *Streaming SIMD Extensions*



Microprocessor recognition

- Cpuid command

Microprocessor recognition

- Older recognition methods
  - Some typically unimportant differences in command execution
    - E.g. push/pop command
      - Write mem[SP], then SP++
      - SP++, then write mem[SP]
  - Programming tricks
  - Some µp's set the register values after reset
    - Can be read only immediately after reset
    - Not available to application unless saved upon system start

Microprocessor recognition

- `cpuid` command
  - Available in 8086 family starting from Pentium and late 486
  - Can be executed at any priviledge level
    - Available to all the applications
  - More and more information available
    - Now decoding it is a quite complex task

Microprocessor recognition

- `cpuid` command
  - If present, a special flag can be set
  - Usage:
    - EAX = function number
    - `Cpuid`
    - Output → EAX, EBX, ECX, EDX
      - Interpretation is function-dependent
    - Functions:
      - Basic: 0x00000000…..
      - Extended: 0x80000000……

Microprocessor recognition

- `cpuid` command
  - Basic functions
    - EAX=0: Highest Function Parameter and Manufacturer ID
      - EAX = highest basic function number
      - EBX, EDX, ECX = vendor string, e.g.
        - » `GenuineIntel` – Intel
        - » `AuthenticAMD` or `AMDisbetter!` – AMD
        - » `CyrixInstead` – Cyrix
        - » `CentaurHauls` – VIA
        - » `VMwareVMware` – VMware virtual machine
        - » `Microsoft Hv` – Hyper-v virtual machine

Microprocessor recognition

- `cpuid` command
  - Basic functions
    - EAX=1: Processor Info and Feature Bits
      - EAX = Processor Type, Family, Model, Stepping
        - » Later also Exteded Family & Model
      - EBX = Brand ID & some other advanced info
      - ECX, EDX – feature flags, e.g.
        - » FPU, MMX, SSE, SSE2, SSE3, SSSE3, SSE4.1, SSE4.2
        - » TSC, PSE (Page Size Ext.), PAE (Phys. Addr. Ext.), PSN (Processor Serial Number), HTT (Hyper-Threading Techn.) etc.

Microprocessor recognition

- `cpuid` command
  - Basic functions
    - EAX=2: Cache and TLB Descriptor information
      - Available since Pentium II
      - EAX, EBX, ECX, EDX = 8-b descriptors
        - » Decoded in a loop (AL = loop count)
        - » App must understand the descriptor values
          - New ID's not understandable for older apps
        - » Some values ambiguous
        - » Currently only for TLB description
          - Cache data available through another (better) mechanism

Microprocessor recognition

- `cpuid` command
  - Basic functions
    - EAX=3: Processor serial number
      - Available in Pentium III only
      - Can by disabled by BIOS (until reset)
      - Nowadays, only a historical meaning
        - » Privacy concerns
        - » Might be used as a hardware key?

Microprocessor recognition

- `cpuid` command
  - Basic functions
    - EAX=4: Deterministic cache parameters
      - (in) EAX = 4; ECX = index; repeated until $AL_{5..0} = 0$
      - (out) EAX, EBX, ECX, EDX = cache information
      - Cache size & organisation must be calculated
      - No descriptors must be known to understand the information

Microprocessor recognition

- `cpuid` command
  - Basic functions
    - EAX=5…A – some advanced architecture-dependent functions
    - EAX=B: Processor Topology
      - Number of cores and threads

Microprocessor recognition

- `cpuid` command
  - Extended functions
    - EAX=80000000: largest extended function
    - EAX=80000001: extended feature bits
    - EAX=80000002..80000004: Processor Brand String
    - …..

Microprocessor recognition

- More information:
  - Intel® Processor Identification and the CPUID Instruction. Application Note 485 (*withdrawn!*)
  - Intel® 64 and IA-32 Architectures Software Developer's Manual Volume 2A: Instruction Set Reference, A-L, pp. 3-190 to 3-224 (2016)
  - AMD CPUID Specification 2.34 (2010)

  - https://en.wikipedia.org/wiki/CPUID

  - http://ixbtlabs.com/articles3/cpu/via-nano-cpuid-fake-p1.html
  - https://www.agner.org/optimize/#cpuidfake

Microprocessor recognition

Example results – Asus EEE PC 1000HG (1)

```
Max. CPUID function: 000A

OEM string: GenuineIntel
FamModStp.: 006.1C.2
Brand     :  0 - No brand
Processor features:
PBE       TM        HTT       SS        SSE2      SSE       FXSR      MMX       ACPI
DS        CLFSH     PAT       CMOV      MCA       PGE       MTRR      SEP       APIC
CX8       MCE       PAE       MSR       TSC       PSE       DE        VME       FPU
Processor features:
MOVBE     PDCM      xTPR      SSSE3     TM2       EST       DS-CPL    Monitor
DTES64    SSE3
CLFSH line size: 8 B
Count of logical processors: 2
Serial No.: not supported or disabled
59h: Data TLB0, 4KB page, fully assoc., 16 ent.
BAh: Code TLB, 4KB page, 8-way assoc., 64 ent.
4Fh: Code TLB, 4KB page, 32 ent.
C0h: Data TLB1, 4KB page, 4-way assoc., 64 ent.
80h: Code TLB, 2MB/4MB page, 4-way assoc., 8/4 ent.
30h: L1 Code cache 32KB, 8-way assoc., 64-byte line
0Eh: L1 Data cache 24KB, 6-way assoc., 64B line
```

Microprocessor recognition

Example results – Asus EEE PC 1000HG (2)

```
Deterministic cache information:
Data L1, 2 thread(s), 1 Core(s), 64B line, 1 part, 6-ways assoc., 64 sets
Size: 24 KB
Code L1, 2 thread(s), 1 Core(s), 64B line, 1 part, 8-ways assoc., 64 sets
Size: 32 KB
Unif L2, 2 thread(s), 1 Core(s), 64B line, 1 part, 8-ways assoc., 1024 sets
Size: 512 KB

Processor name:          Intel(R) Atom(TM) CPU N270   @ 1.60GHz



Please wait, measuring processor frequency (about 5 seconds)...
Reported frequency [MHz]:  1600
Measured frequency [MHz]:  1601
```

Microprocessor recognition

Example results – Samsung RC710 (1)

```
Max. CPUID function: 000B

OEM string: GenuineIntel
FamModStp.: 006.25.5
Brand     :  0 - No brand
Processor features:
PBE       TM        HTT       SS        SSE2      SSE       FXSR      MMX       ACPI
DS        CLFSH     PSE-36    PAT       CMOV      MCA       PGE       MTRR      SEP
APIC      CX8       MCE       PAE       MSR       TSC       PSE       DE        VME
FPU
Processor features:
POPCNT    SSE4.2    SSE4.1    PCID      PDCM      xTPR      CX16      SSSE3     TM2
EST       VMX       DS-CPL    Monitor   DTES64    SSE3
CLFSH line size: 8 B
Count of logical processors: 16
5Ah: Data TLB0, 2MB/4MB page, 4-way assoc., 32 ent.
03h: Data TLB, 4KB page, 4-way assoc., 64 ent.
55h: Code TLB, 2MB/4MB page, fully assoc., 7 ent.
DDh: L3 cache 3MB, 12-way assoc., 64B line
B2h: Code TLB, 4KB page, 4-way assoc., 64 ent.
F0h: 64B prefetch
2Ch: L1 Data cache 32KB, 8-way assoc., 64B line
21h: L2 MLC 256KB, 8-way assoc., 64B line
CAh: Shared L2 TLB, 4KB page, 4-way assoc., 512 ent.
09h: L1 Code cache 32KB, 4-way assoc., 64B line
```

Microprocessor recognition

Example results – Samsung RC710 (2)

```
Deterministic cache information:
Data L1, 2 thread(s), 8 Core(s), 64B line, 1 part, 8-ways assoc., 64 sets
Size: 32 KB
Code L1, 2 thread(s), 8 Core(s), 64B line, 1 part, 4-ways assoc., 128 sets
Size: 32 KB
Unif L2, 2 thread(s), 8 Core(s), 64B line, 1 part, 8-ways assoc., 512 sets
Size: 256 KB
Unif L3, 16 thread(s), 8 Core(s), 64B line, 1 part, 12-ways assoc., 4096 sets
Size: 3 MB

2 processors at level 00  - Thread
4 processors at level 01  - Core
Max. CPUID function: 0008

Processor features:
IA-64     RDTSCP    XD bit
Processor name: Intel(R) Core(TM) i3 CPU       M 380  @ 2.53GHz



Please wait, measuring processor frequency (about 5 seconds)...
Reported frequency [MHz]:  2533
Measured frequency [MHz]:  2526
```

Microprocessor recognition

Example results – Lenovo T540 (1)

```
FamModStp.: 006.3C.3
Brand     :  0 - No brand
Processor features:
PBE       TM        HTT       SS        SSE2      SSE       FXSR      MMX       ACPI
DS        CLFSH     PSE-36    PAT       CMOV      MCA       PGE       MTRR      SEP
APIC      CX8       MCE       PAE       MSR       TSC       PSE       DE        VME
FPU
Processor features:
RDRAND    F16C      AVX       XSAVE     AES       TSD d.l.  POPCNT    MOVBE
SSE4.2    SSE4.1    PCID      PDCM      xTPR      CX16      FMA       (11)
SSSE3     TM2       EST       VMX       DS-CPL    Monitor   DTES64    PCLMULDQ  SSE3
CLFSH line size: 8 B
Count of logical processors: 16
Serial No.: not supported or disabled
63h: Unknown: 63h
03h: Data TLB, 4KB page, 4-way assoc., 64 ent.
76h: Code TLB, 2MB/4MB page, fully assoc., 8 ent.
FFh: Unknown: FFh
B5h: Code TLB, 4KB page, 8-way assoc., 64 ent.
F0h: 64B prefetch
C1h: Shared L2 TLB, 4KB/2MB page, 8-way assoc., 1024 ent.
```

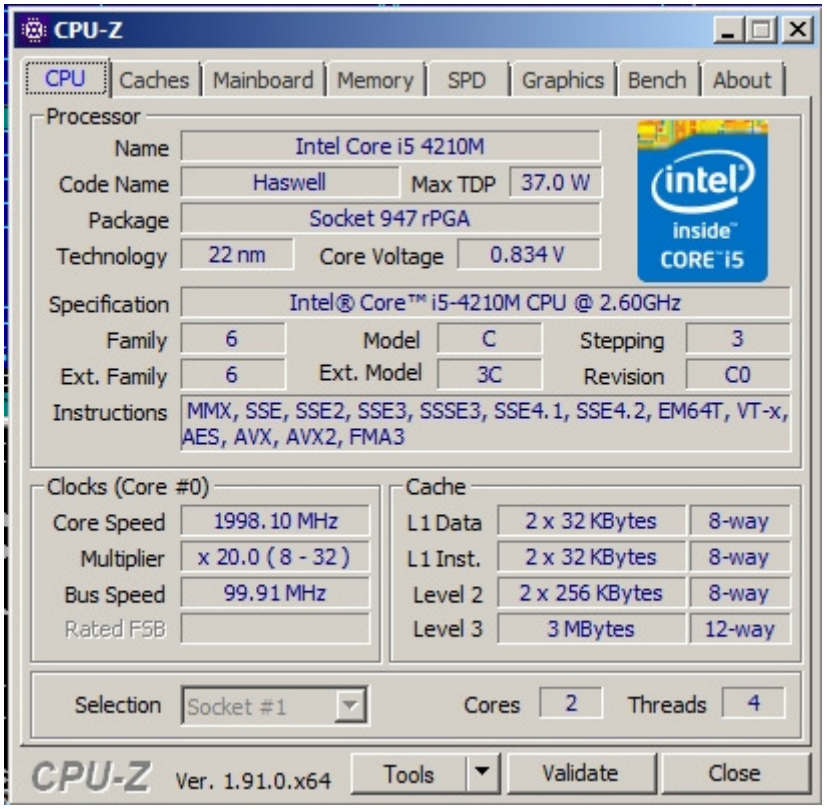
Microprocessor recognition

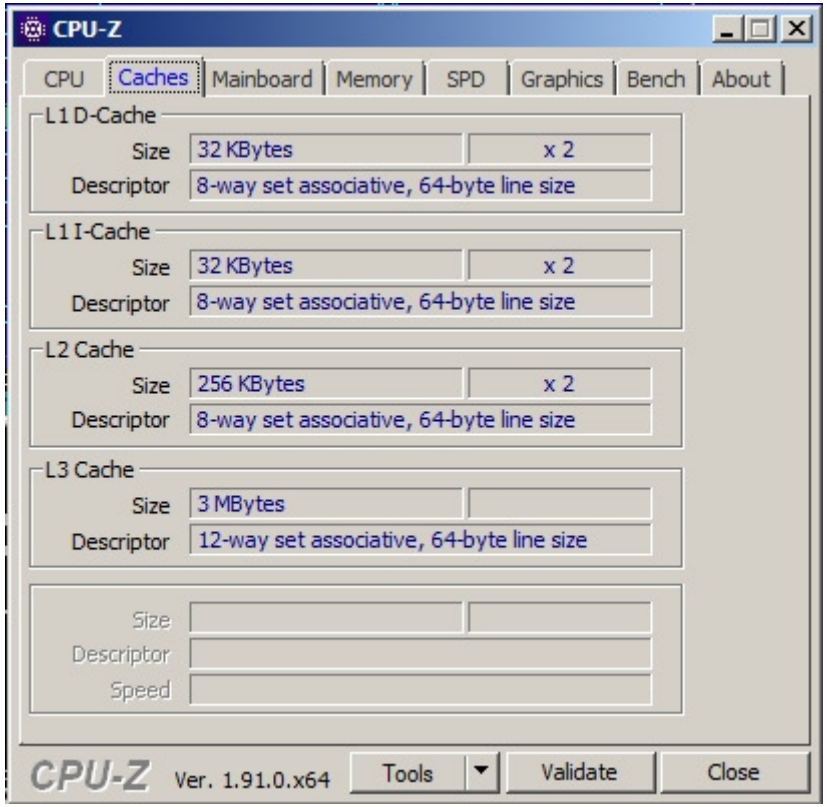
Example results – Lenovo T540 (2)

```
Deterministic cache information:
Data L1, 2 thread(s), 8 Core(s), 64B line, 1 part, 8-ways assoc., 64 sets
Size: 32 KB
Code L1, 2 thread(s), 8 Core(s), 64B line, 1 part, 8-ways assoc., 64 sets
Size: 32 KB
Unif L2, 2 thread(s), 8 Core(s), 64B line, 1 part, 8-ways assoc., 512 sets
Size: 256 KB
Unif L3, 16 thread(s), 8 Core(s), 64B line, 1 part, 12-ways assoc., 4096 sets
Size: 3 MB

2 processors at level 00  - Thread
4 processors at level 01  - Core
Max. CPUID function: 0008

Processor features:
IA-64     RDTSCP    SSE2      XD bit
Processor name: Intel(R) Core(TM) i5-4210M CPU @ 2.60GHz


Please wait, measuring processor frequency (about 5 seconds)...
Reported frequency [MHz]:  2600
Measured frequency [MHz]:  2593
```

Microprocessor recognition

Example results – Lenovo T540 (using cpu-z)





Microprocessor recognition

Example results – Samsung NC20 (subset)

```
Max. CPUID function: 000A
OEM string: CentaurHauls
FamModStp.: 006.0F.2
B0h: Code TLB, 2MB/4MB page, 4-way assoc., 8/4 ent.
B3h: Data TLB, 4KB page, 4-way assoc., 128 ent.
02h: Code TLB, 4MB page, fully assoc., 2 ent.
7Dh: L2 cache 2MB, 8-way assoc., 64B line
30h: L1 Code cache 32KB, 8-way assoc., 64-byte line
04h: Data TLB, 4MB page, 4-way assoc., 8 ent.
2Ch: L1 Data cache 32KB, 8-way assoc., 64B line
Deterministic cache information:
Max. CPUID function: 0008
Processor name:                VIA Nano processor U2250@1300+MHz
L1 Code TLB: 2/4 MB page, 0 entries, 0-way assoc.
L1 Data TLB: 2/4 MB page, 0 entries, 0-way assoc.
L1 Code TLB: 4KB page, 65408 entries, 8-way assoc.
L1 Data TLB: 4KB page, 65408 entries, 8-way assoc.
L1 Code cache: 64 KB, 16-way assoc., 64 B/line, 1 lines/tag
L1 Data cache: 64 KB, 16-way assoc., 64 B/line, 1 lines/tag
L2 Code/Unif TLB: 2/4 MB page, off
L2 Data TLB: 2/4 MB page, off
L2 Code/Unif TLB: 4KB page, off
L2 Data TLB: 4KB page, off
L2 Unif cache: 1024 KB, 16-way assoc., 64 B/line, 1 lines/tag
```

Microprocessor recognition

Example results – DOSBox 0.74

- Pentium emulation mode

```
Max. CPUID function: 0001

OEM string: GenuineIntel
FamModStp.: 005.01.3
Brand     :  0 - No brand
Processor features:
TSC       FPU



Please wait, measuring processor frequency (about 5 seconds)...
Reported frequency [MHz]:     0
Measured frequency [MHz]:     2
```