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Microprocessor and Embedded Systems

Faculty of Automatic Control, Electronics and Computer Science, Informatics, Bachelor Degree

Lecture 4

From 80286 to 80486

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286 to 486

Program:

- 80286 basic properties
- 80386 basic properties
- 80486 basic properties
- 80486 structure, signals

286 to 486

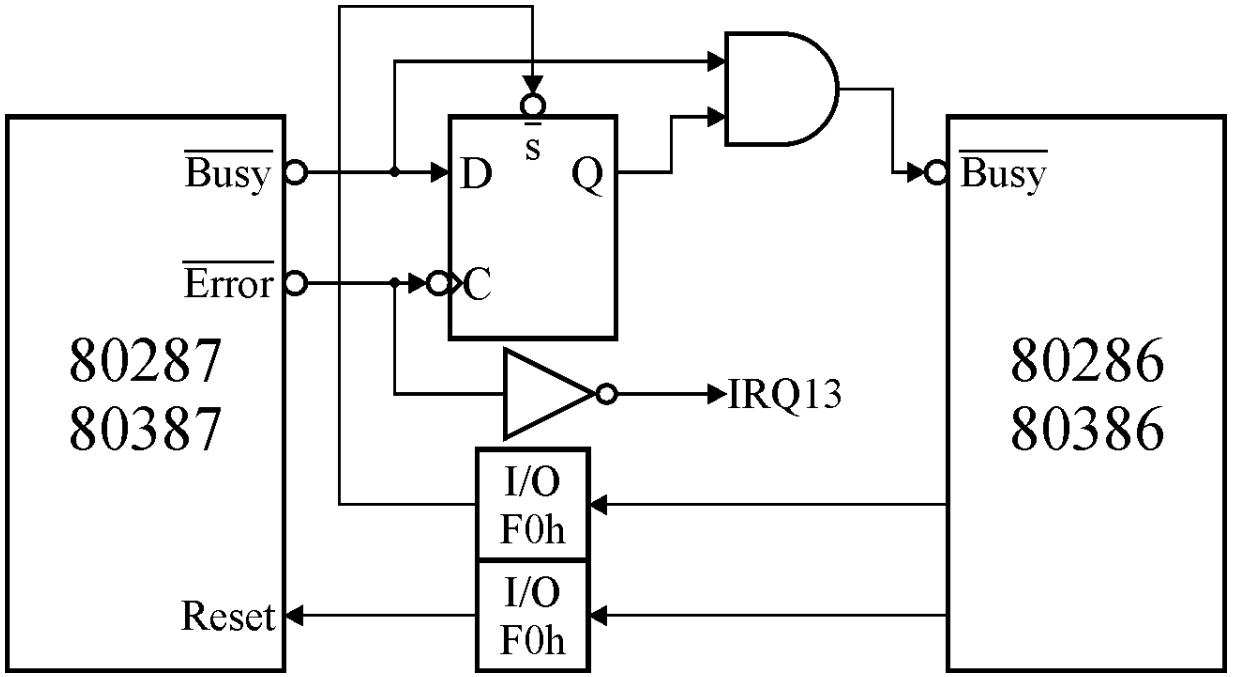
- 80286 basic properties
  - Two operating modes
    - Real mode
      - Executable code compatibility
      - Few additional commands
        - » Procedure call support
        - » Table support
    - Protected (virtual) mode
      - Additional commands
      - Operating system support functions
      - Some command restricted for OS
      - Source-code-only compatibility

286 to 486

- 80286 basic properties
  - Coprocessor cooperation changed
    - 287 can't address memory
      - Virtual addresses can be used
      - 286 must read/write data
        - » (2 access cycles: memory & coprocessor)
      - Coprocessor visible in 286' I/O addressing space
    - Software emulation possible
      - No coprocessor → exception

286 to 486

- 80286 basic properties
  - Coprocessor cooperation



286 to 486

- 80286 basic properties
  - Address & data buses separate
    - Higher throughput
    - Faster address decoding
    - Interleaved memory support
  - Disadvantages
    - Segment capacity ≤ 64 KB
    - 8086 software can't run under 80286 protected mode
    - Can't switch back to the real mode (reset required)
      - Problems in some µcomputer architectures (e.g., PC/AT)
    - Registers have predefined functions
      - e.g., accumulator, base, index…

286 to 486

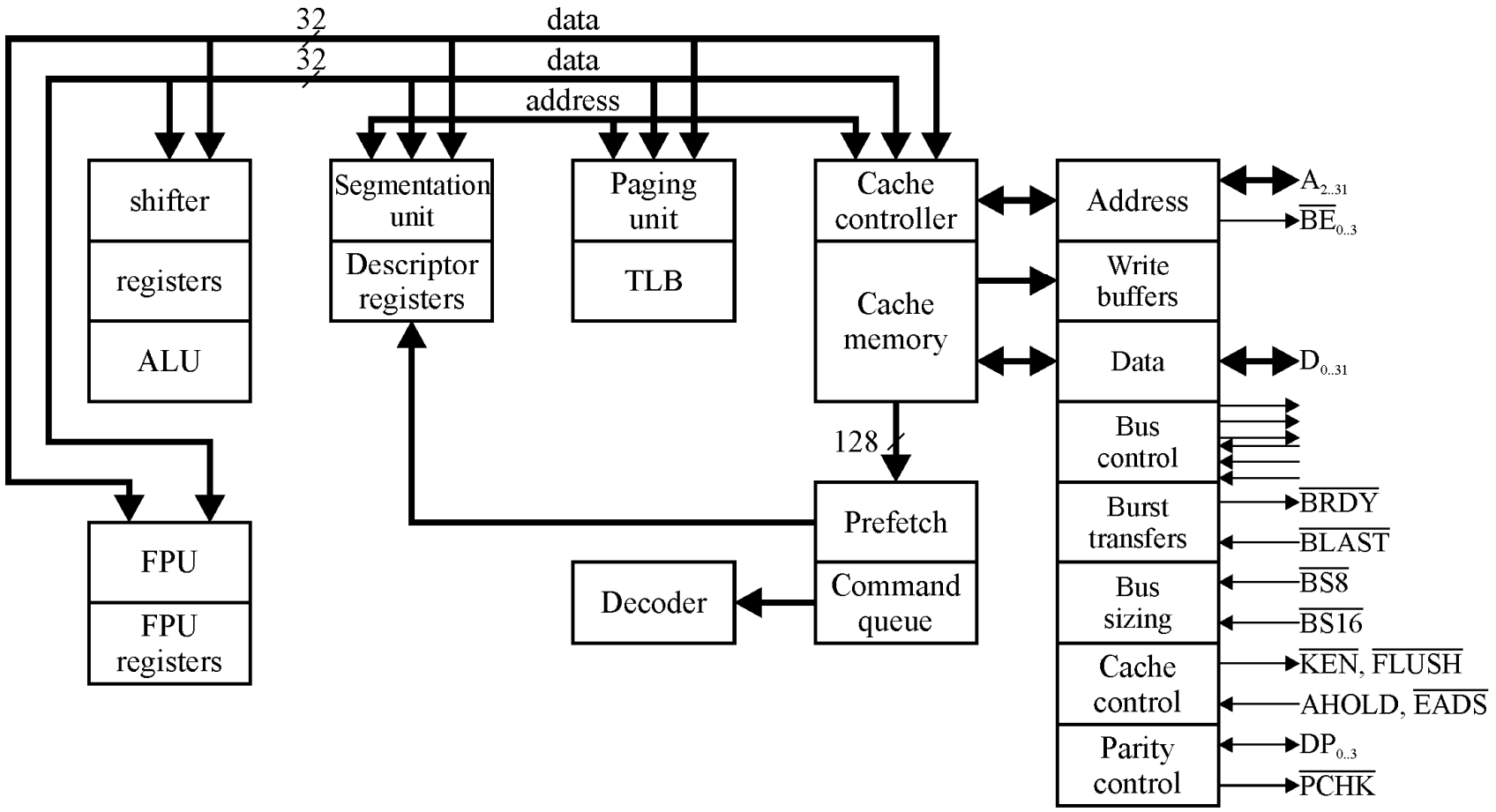
- 80386 basic properties
  - Three operating modes
    - Real mode
      - Like 8086 + few additional commands
    - Protected (virtual) mode
      - Like 80286, but 32-bit addressing
    - Virtual 8086
      - Can run real-mode programs in protected mode
      - Some direct hardware access is forbidden
      - Multitasking is possible
  - Software switch between all modes possible

286 to 486

- 80386 basic properties
  - Register usage limitations omitted
    - 16-b regs: only BX can address
    - 32-b regs: EAX, EBX, ECX, EDX can address
  - Coprocessor cooperation like in 80286
    - 80287 or 80387 can be used
  - Memory management
    - Segmentation
    - Paging
  - Most of 286 disadvantages resolved

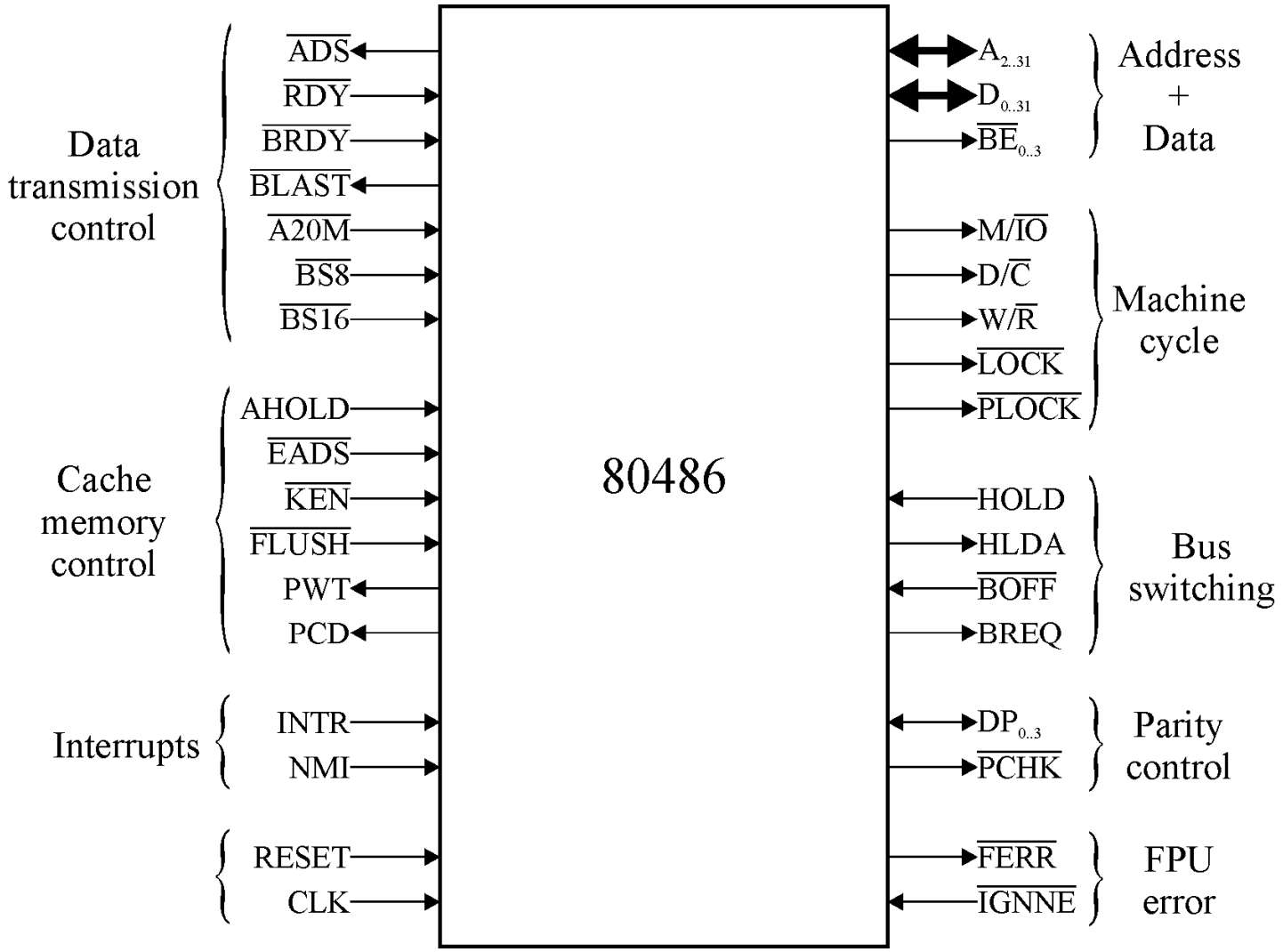
286 to 486

- 80486 structure



286 to 486

- 80486 signals



286 to 486

- 80486 signals
  - Address lines
    - $A_{0..1}$ → decoded into $\overline{BE_{0..3}}$
      - Which byte in double word is active during transfer
      - 1, 2, 3 or 4 bytes transferred
      - Not every combination possible
    - $A_{2..3}$ → output only
    - $A_{4..31}$ → bidirectional
  - Bus size
    - $\overline{BS8}$, $\overline{BS16}$ – data bus width adjustment to device capabilities
      - E.g., signal from address decoder
    - $\overline{A20M}$ – mask/unmask A20 line

286 to 486

- 80486 signals
  - Machine cycle
    - $\overline{\text{LOCK}}$ – bus lock
    - $\overline{\text{PLOCK}}$ (Pseudolock) – transfer longer than 1 bus cycle
      - Descriptor table read
      - Cache fill
      - FPU read/write
  - FPU error
    - $\overline{\text{FERR}}$ – FPU error
      - For MS-DOS compat.
    - $\overline{\text{IGNNE}}$ – ignore FP err.
      - $\overline{\text{FERR}}$ appears

M/$\overline{\text{IO}}$	D/$\overline{\text{C}}$	W/$\overline{\text{R}}$	Cycle
0	0	0	Interrupt acknowledge
0	0	1	Halt or special cycle
0	1	0	I/O Read
0	1	1	I/O Write
1	0	0	Fetch
1	0	1	
1	1	0	Memory Read
1	1	1	Memory Write

286 to 486

- 80486 signals
  - Bus switching
    - HOLD, HLDA – for DMA controller
    - BREQ – internal bus request generated
    - $\overline{\mathrm{BOFF}}$ (Backoff) – fast bus disconnect in the nearest clk
      - Faster than HOLD/HLDA
      - Transfer paused
  - Parity control
    - $\overline{\mathrm{PCHK}}$ – data parity error detected
      - System designer freedom how to cope with this
    - $\mathrm{DP}_{0..3}$ – data parity bit for each byte

286 to 486

- 80486 signals
  - Data transmission control
    - $\overline{\mathrm{ADS}}$ – address present on address lines
    - $\overline{\mathrm{RDY}}$ – device ready
    - $\overline{\mathrm{BRDY}}$ – device ready for burst transfer
    - $\overline{\mathrm{BLAST}}$ – latest byte of data exchange
  - Cache control
    - $\overline{\mathrm{EADS}}$ – address given by external device
    - AHOLD – another bus master invalidates cache
    - $\overline{\mathrm{KEN}}$ – current cycle is cacheable
    - $\overline{\mathrm{FLUSH}}$ – force memory update from cache
    - PWT, PCD – memory page cache policy