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Microprocessor and Embedded Systems

Faculty of Automatic Control, Electronics and Computer Science, Informatics, Bachelor Degree

Lecture 3

IBM PC microcomputer

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IBM PC

Program:

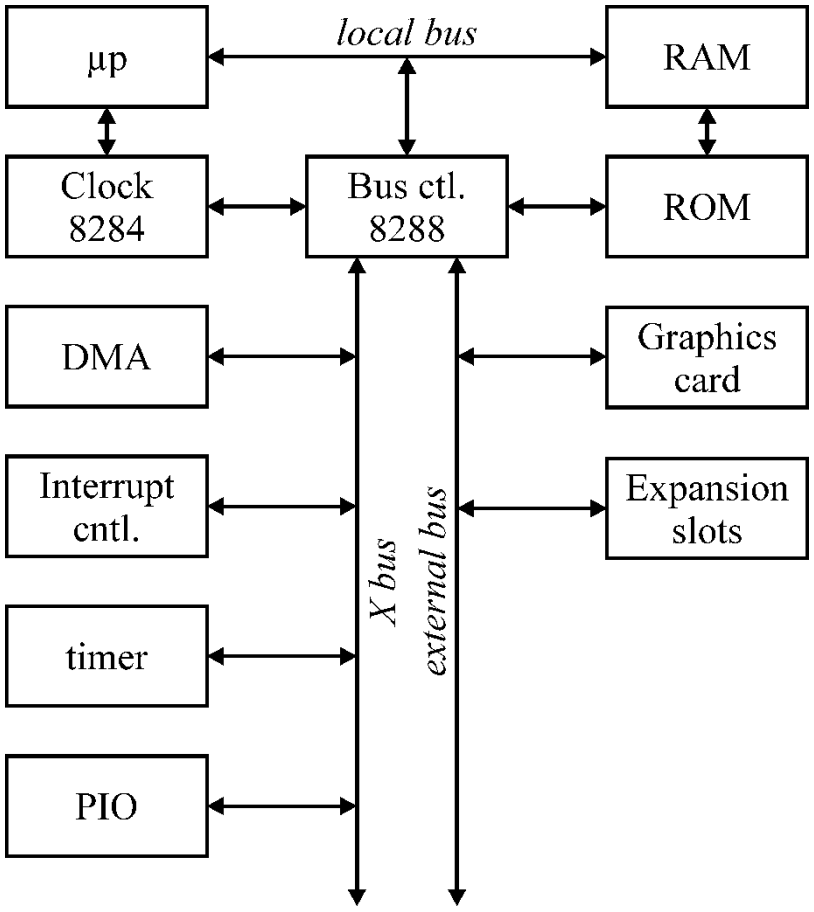
- General properties
- Detailed block diagram
- ISA-8 bus
- Extension to PC/AT
- ISA-16 extension

IBM PC

- Basic properties
  - µp: 8086/8088, (8087), NEC V20, V30
  - Clk = 14,318180 MHz :3 → 4,77 MHz for µp
  - Buses (according to „*Anatomia PC*”):
    - Local bus (20-b address + 16-b data)
    - System bus – buffered local bus + control signals
    - X – for mainboard resources (BIOS, I/O)
    - Memory – to DRAM
    - External – to expansion slots

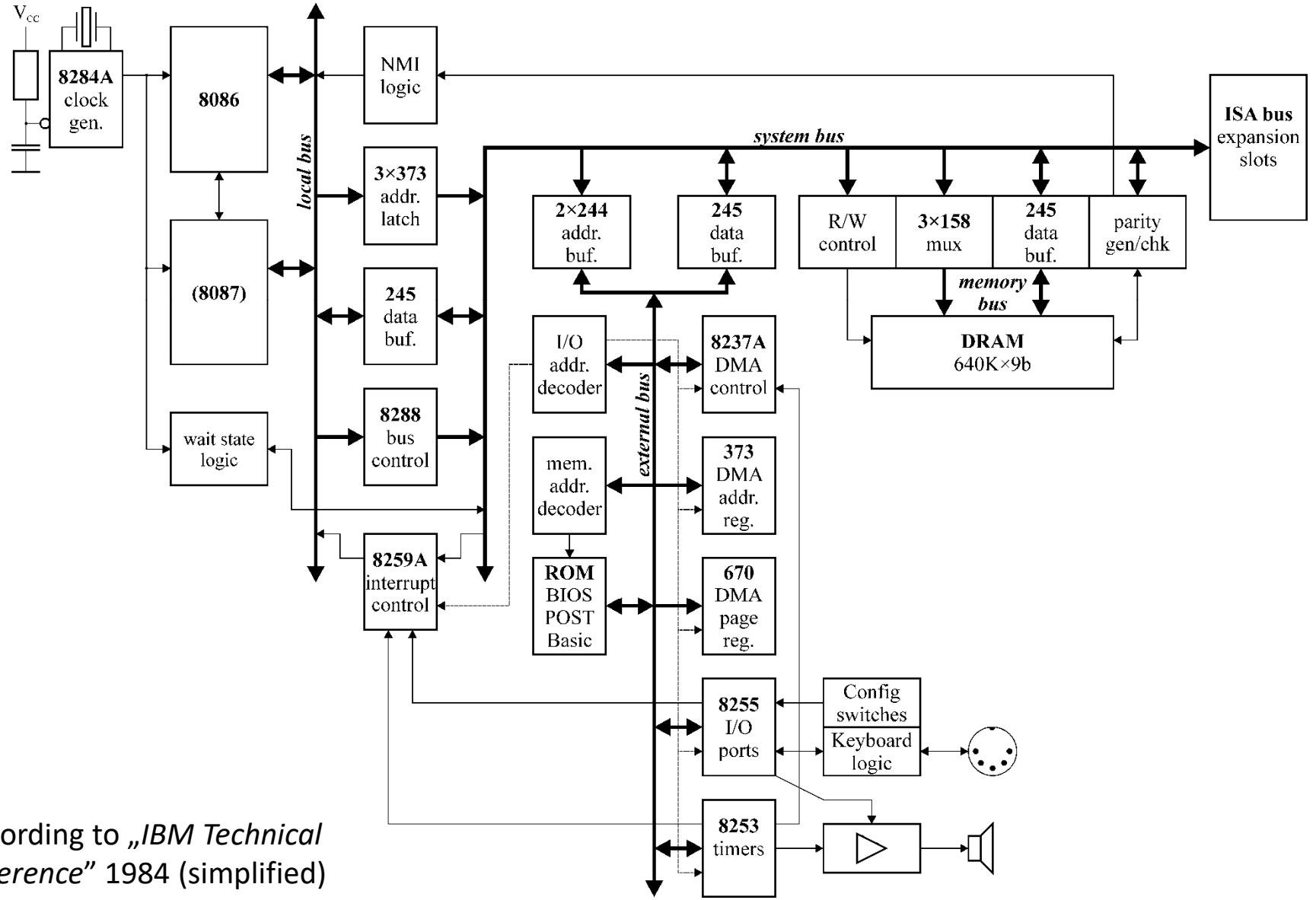
IBM PC

- Block diagram



According to „*Anatomia PC*”

IBM PC



According to „*IBM Technical Reference*" 1984 (simplified)

IBM PC

- Motherboard details
  - Interrupts

Interrupt		Device
0	08	System clock (8253)
1	09	Keyboard
2	0A	®
3	0B	COM2
4	0C	COM1
5	0D	HDD
6	0E	FDD
7	0F	LPT1

  - DMA

DMA	Device
0	DRAM refresh
1	SDLC
2	FDD
3	HDD

IBM PC

- Motherboard details
  - Memory addresses

Address		Memory
00000	9FFFF	RAM
00000	*03FFF*	*Interrupt vector table*
B0000	BFFFF	Video memory
C0000	C7FFF	®
C8000	C9FFF	HDD BIOS
F6000	FDFFF	Basic
FE000	FFFFF	BIOS
FFFF0		*reset*

IBM PC

- Motherboard details
  - IO addresses
    - (Simplified decoding!)

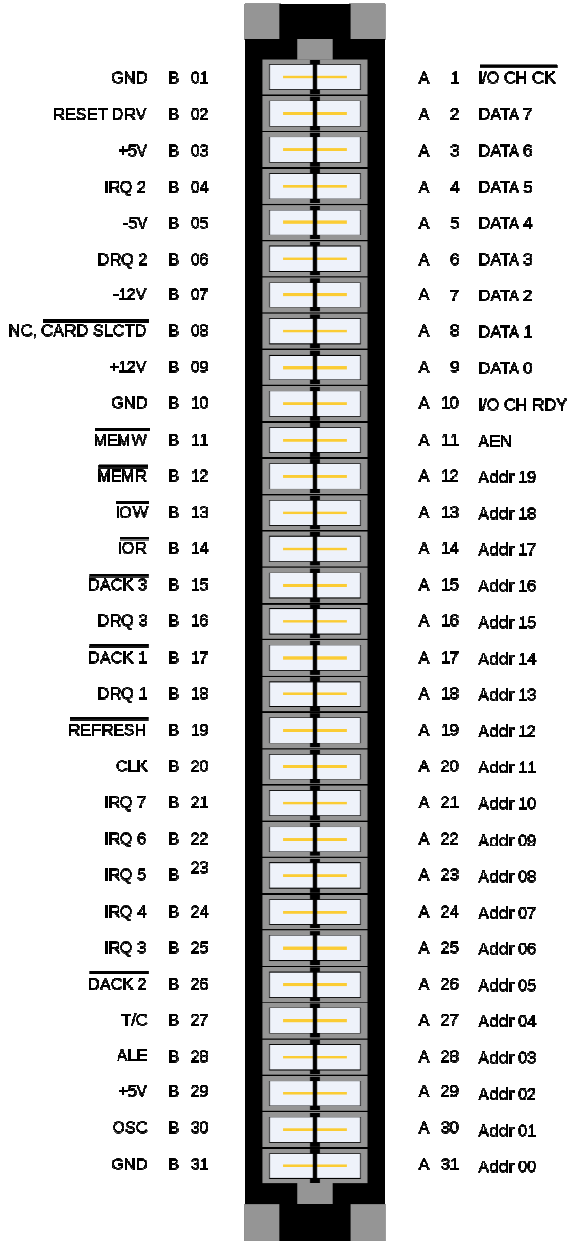
Address		Device
00	0F	8237A
20	21	8259A
40	43	8253
60	63	8255
80	83	DMA page registers
A0		NMI mask

IBM PC

- Expansion slots
  - Modular computer structure
  - Computer functions easily extended
  - Computer functions optimised for application
  - Wide (unlimited?) devices range
  - Ease of own devices & interfaces design
    - Accessible directly from µp's addressing space
  - ISA bus

IBM PC

- ISA bus
  - Signals
    - $A_{0..19}$
    - $D_{0..7}$
    - $IRQ_{2..7}$
    - $DRQ_{1..3}$
    - $\overline{DACK}_{1..3}$
    - $\overline{DACK}_{0}$
    - $\overline{IORd}$
    - $\overline{IOWr}$
    - $\overline{MemRd}$
    - $\overline{MemWr}$
    - Reset
    - OSC (14,3… MHz)
    - ALE
    - I/OChRdy
    - $\overline{IOChk}$
    - AEN
    - T/C
    - ±5V
    - ±12V
    - ground

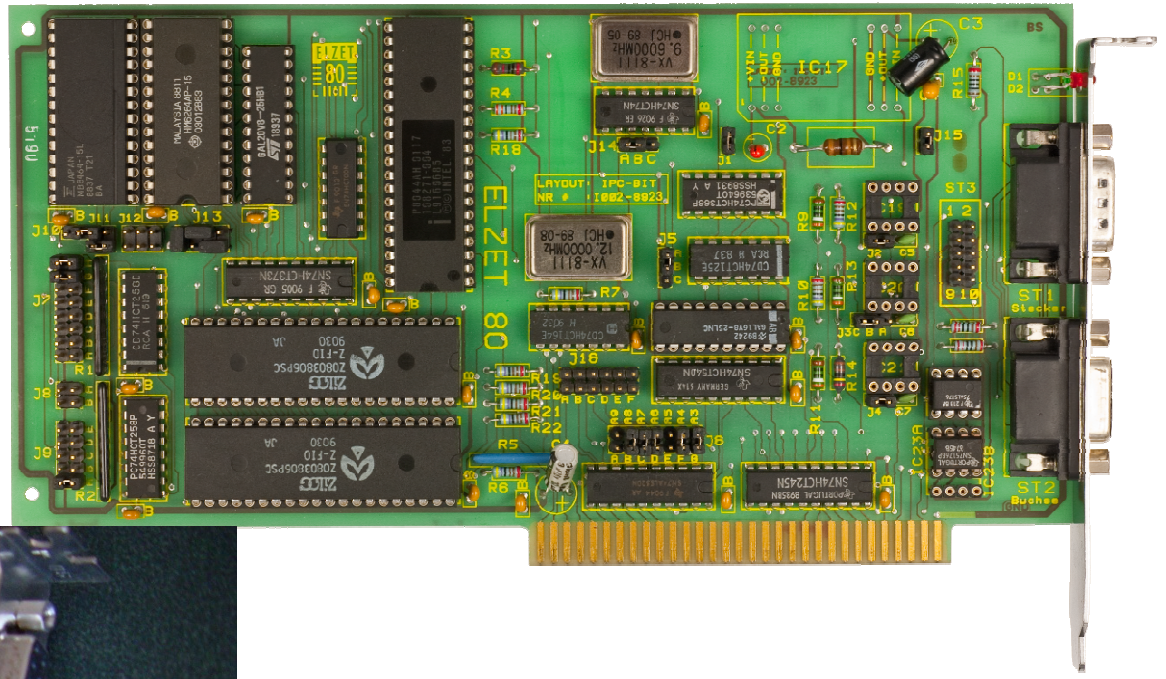


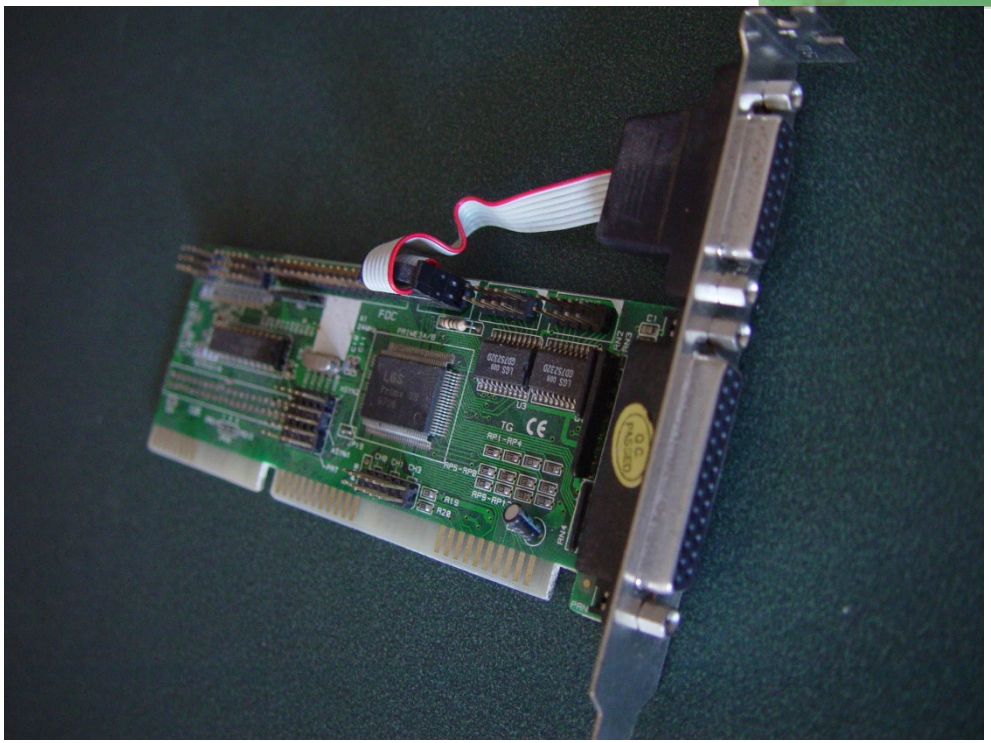
IBM PC

- ISA bus

IBM PC

- ISA bus





IBM PC

- IBM PC/AT
  - 80286, 386, 486 µp's
  - Buses
    - Local bus (24 b address + 16 b data)
    - System bus (buffered)
    - External (BIOS, motherboard I/O)
    - Memory (to DRAM)
    - L (latched address $A_{17..23}$)
  - Extended interrupt system (15 int's)
  - Extdended DMA system (7 channels)
  - DIP switches → CMOS setup

IBM PC

- Motherboard details
  - Interrupts
    - Master/slave 8259A controller configuration

Interrupt		Device
0	08	System clock (8253)
1	09	Keyboard
2	0A	®→slave 8259A
3	0B	COM2
4	0C	COM1
5	0D	LPT2
6	0E	FDD
7	0F	LPT1

Interrupt		Device
8	70	Real time clock
9	71	Remapped IRQ2
A	72	®
B	73	®
C	74	®
D	75	Coprocessor
E	76	HDD
F	77	® (later HDD2)

IBM PC

- Motherboard details
  - DMA
    - master/slave DMA controler configuration
    - cascade mode

DMA	Bits	Device
4	16	slave
5	16	
6	16	
7	16	

DMA	Bits	Device
0	8	®
1	8	SDLC
2	8	FDD
3	8	®

    - DRAM refresh every 15µs
      - Only 24 ISA cycles fit in burst transfer
      - Devicess need their own buffering

IBM PC

- Motherboard details
  - DMA
    - A_0 of DMA connected to A_1 of system bus
      - Only even addresses generated
      - Block extended to 128 KB
    - DMA Page registers connected without a shift
      - Address range is still 24-b
    - DMA address can’t inc/dec across page boundaries
      - 64K/128K depending on channel

IBM PC

- Motherboard details
  - IO addresses (AT)

Address		Device
00	1F	8237A #1
20	3F	8259A, Master
40	5F	Timer
60	6F	8042 (keyboard)
70	7F	Real-time clock, NMI
80	9F	DMA page registers
A0	BF	8259A, Slave
C0	DF	8237A #2
F0		Clear math coprocessor busy
F1		Reset math coprocessor
F8	FF	Math coprocessor

IBM PC

- ISA bus extension
  - Signals
    - $LA_{17..19}$ (appears earlier)
    - $SD_{8..15}$
    - $\overline{SBHE}$
    - $IRQ_{8..15}$
    - $DRQ_{4..7}$
    - $\overline{DACK}_{4..7}$
    - $\overline{SMemRd}$ (access all memory)
    - $\overline{SMemWr}$
    - $\overline{0WS}$
    - $\overline{REF}$
    - $\overline{MemCS16}$, $\overline{IOCS16}$