Fundusze Europejskie
Wiedza Edukacja Rozwój

Rzeczpospolita Polska

Unia Europejska
Europejski Fundusz Społeczny

Politechnika Śląska jako Centrum Nowoczesnego Kształcenia
opartego o badania i innowacje

POWR.03.05.00-IP.08-00-PZ1/17

Projekt współfinansowany przez Unię Europejską ze środków Europejskiego Funduszu Społecznego

Microprocessor and Embedded Systems

Faculty of Automatic Control, Electronics and Computer Science, Informatics, Bachelor Degree

Lecture 1

8086 microprocessor

Bartłomiej Zieliński, PhD, DSc

8086

Program:

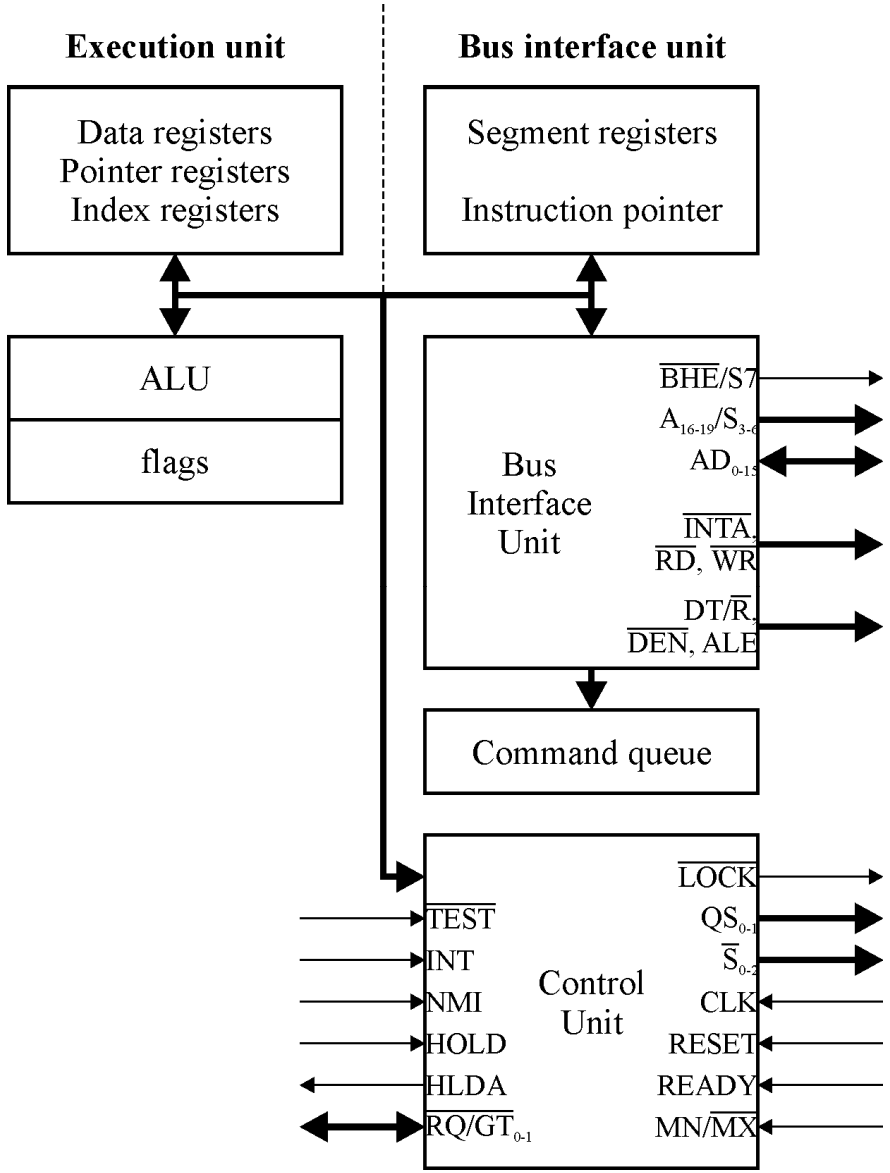
- General properties
- Internal structure
- Registers
- Addressing
- Addressing modes
- Signals, machine cycles
- Central unit
- Command formats

8086

- Basic properties
  - 20 address bits, 8/16 data bits
  - Multiplexed address/data bus
  - Addressing space: 1 MB memory, 64 KB I/O
  - 14 16-b registers
  - 2-phase command cycle (fetch/execute)
  - Advanced interrupt system
    - INT, NMI, int. vectors, internal int's, software int's
  - 2 ways of system cooperation
    - Minimum/maximum mode

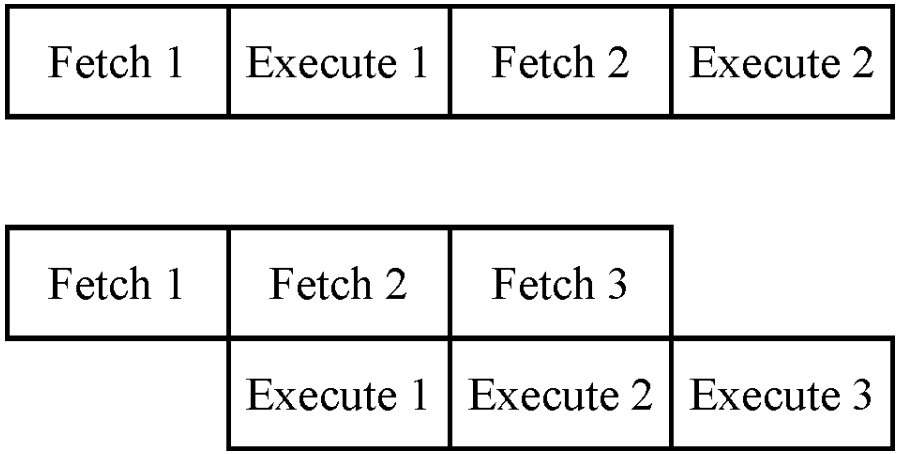
8086

- Internal structure
  - Execution unit
  - Bus interface unit
  - Command queue
    - 4/6B long
    - Filled if
      - ≥2B free
      - no R/W req. EU



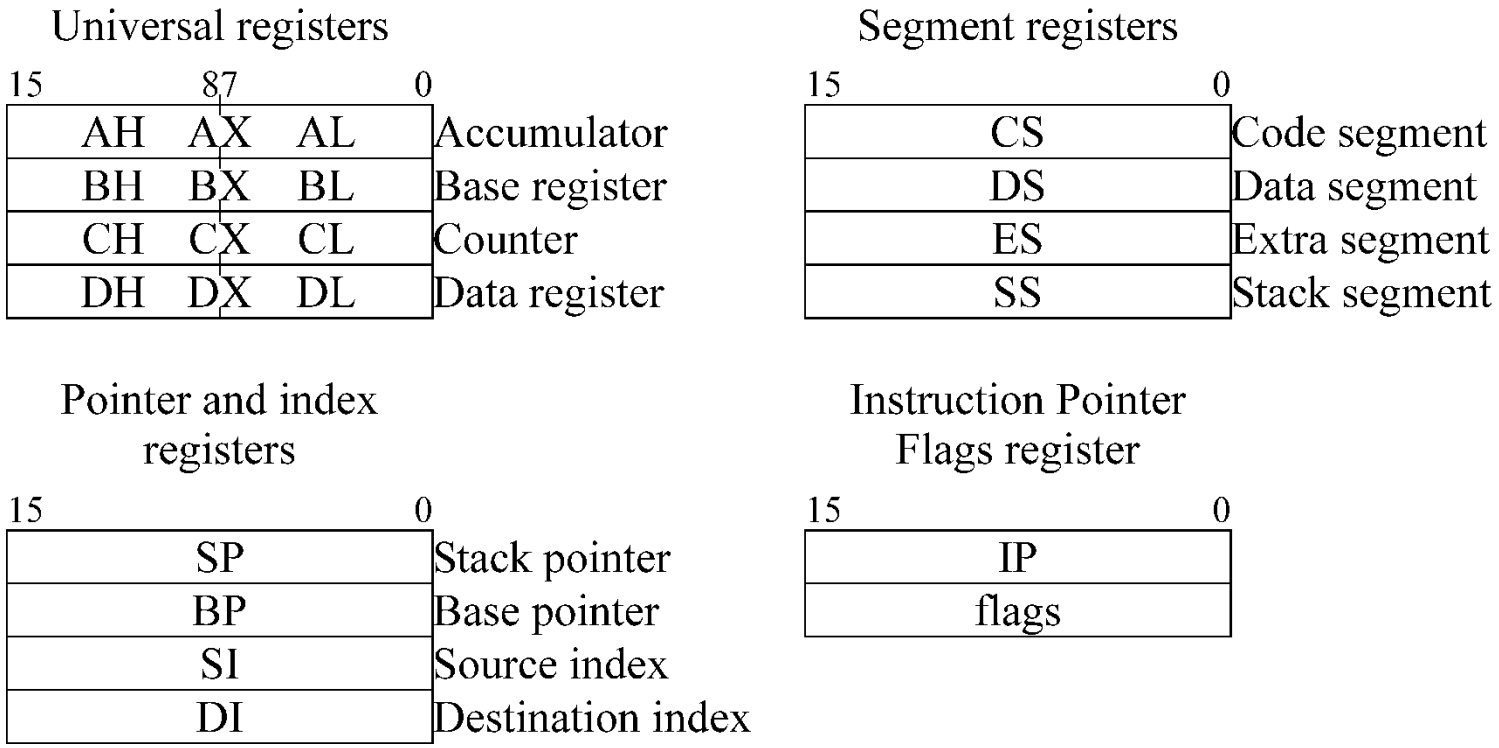
8086

- Command cycle
  - 2 explicit separate phases



8086

- Registers



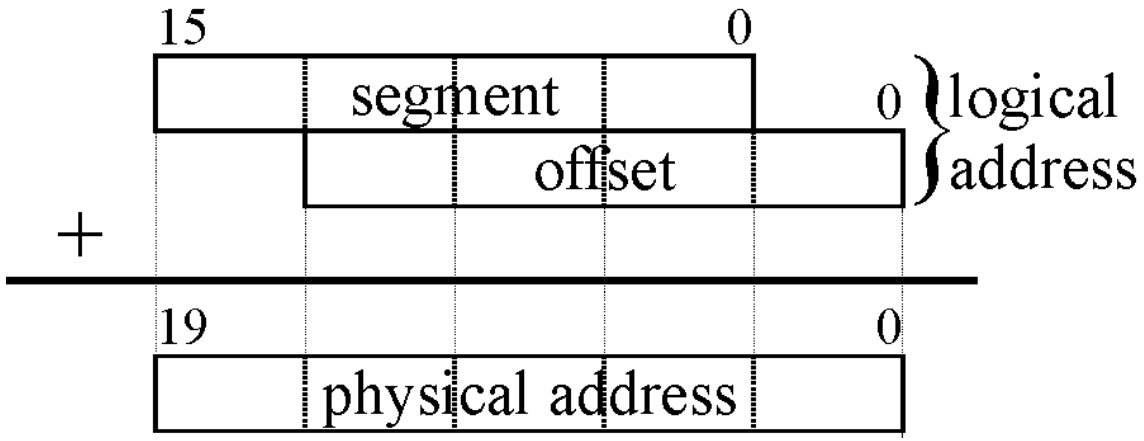
8086

- Registers – flags
  - 6 state bits: C, P, A, Z, S, O
  - 3 control bits: T, I, D

Symbol	Name	Function
C	Carry	1 = carry/borrow at the highest bit of the result
P	Parity	1 = even numer of 1's in lower result byte
A	Half carry	1 = carry/borrow at the 4^{th} bit of AL
Z	Zero	1 = result=0
S	Sign	= highest bit of the result
T	Trap	1 = Single step mode
I	Interrupt	1 = interrupts are unmasked
D	Direction	Block operations address: 1-decremented, 0-incremented
O	Overflow	1 = signed result has more bits than destination argument

8086

- Memory addressing
  - 1 MB capacity
  - Logical segments of 64KB each
  - Logical address:
    - Segment (16 bits)
    - Offset (16 bits)
  - Physical address:
    - 20 bits



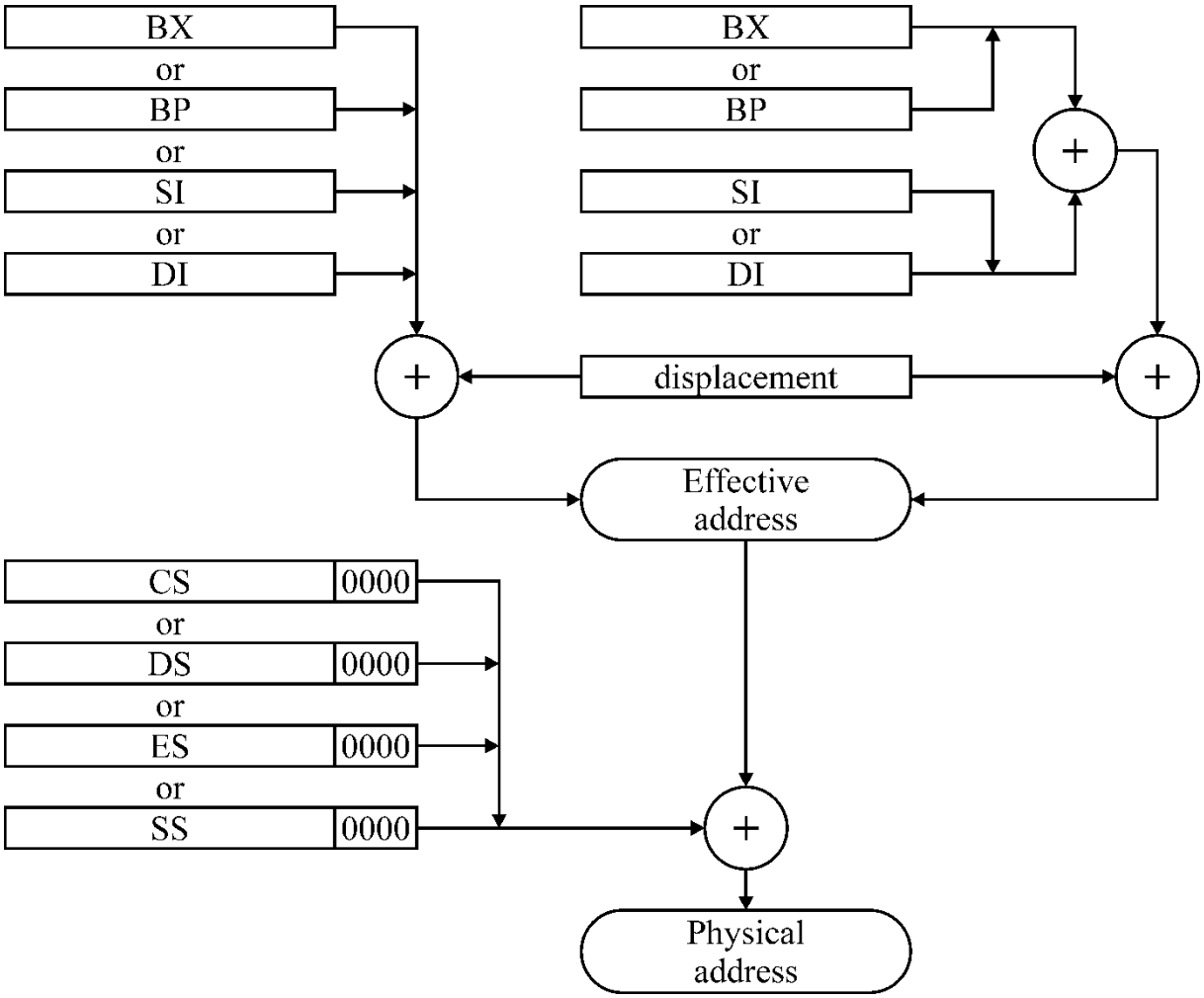
8086

- Memory addressing

Memory operation	Segment adress		Offset
	Default	Alternative	
Fetch	CS		IP
Stack	SS		SP
Block read	DS	CS, ES, SS	SI
Block write	ES		DI
BP as base reg.	SS	CS, DS, ES	Displacement, SI, DI, BX, BP
BX as base reg.	DS	CS, ES, SS	Displacement, SI, DI, BX, BP

8086

- Memory addressing



8086

- Addressing modes (1)
  - Immediate
    - `mov cx, 4929h; add ax, 2387h;  mov al, 5`
  - Register
    - `mov cx, bx; add ax, dx`
  - Direct
    - `mov ax, [1592h]; mov al, [0300h]`
  - Register indirect
    - `mov ax, [bx]; add ax, [bx]`

8086

- Addressing modes (2)
  - Based
    - `mov dx, [bx+4]; add cl, [bx+8]`
    - `mov ax, [bp+2]`
  - Indexed
    - `mov ax, [si+16]; add al, [di+16]`
  - Based-index
    - `add cx, [bx+si]; mov ax, [bp+di]`
  - Based indexed with displacement
    - `add cx, [bx+si+8]; mov ax, [bp+di+4]`

8086

- General command format

  - D(irection): from (0)/to (1) register
  - W(ord): 8 (0)/16 (1) bits
  - Mod(e):

Mode	
00	No displacement fields, disp=0
01	8-b displacement present (sign extended to 16-b)
10	16-b displacement present
11	R/M treated as Reg field

8086

- General command format (2)
  - Reg(ister):

Word operand (W=1)		Byte operand (W=0)		Segment	
000	AX	000	AL	00	ES
001	CX	001	CL	01	CS
010	DX	010	DL	10	SS
011	BX	011	BL	11	DS
100	SP	100	AH		
101	BP	101	CH		
110	SI	110	DH		
111	DI	111	BH		

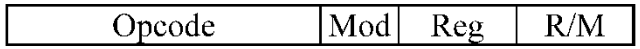
8086

- General command format (3)
  - Reg(ister)/M(emory):

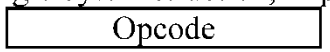
R/M	Effective address
000	(BX)+(SI)+disp
001	(BX)+(DI)+disp
010	(BP)+(SI)+disp
011	(BP)+(DI)+disp
100	(SI)+disp
101	(DI)+disp
110	(BP)+disp
111	(BX)+disp

8086

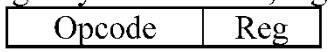
- Command formats



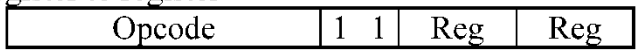
Single byte instruction, implied operand



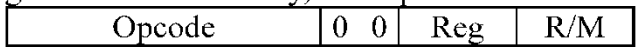
Single byte instruction, register mode



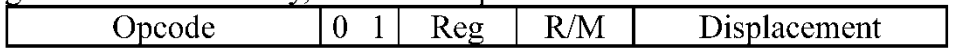
Register to register



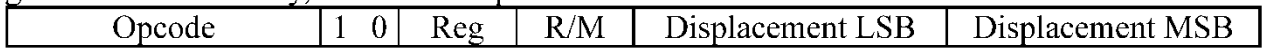
Register to/from memory, no displacement



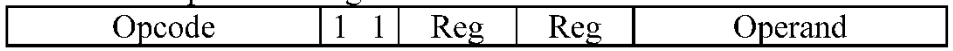
Register to/from memory, with 8-b displacement



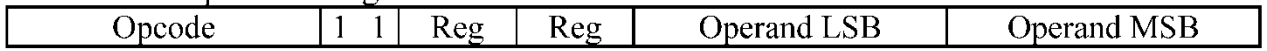
Register to/from memory, with 16-b displacement



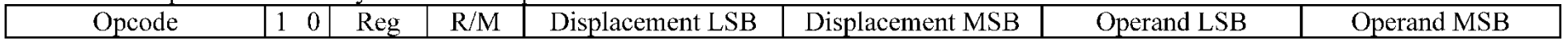
Immediate 8-b operand to register



Immediate 16-b operand to register



Immediate 16-b operand to memory with 16-b displacement



8086

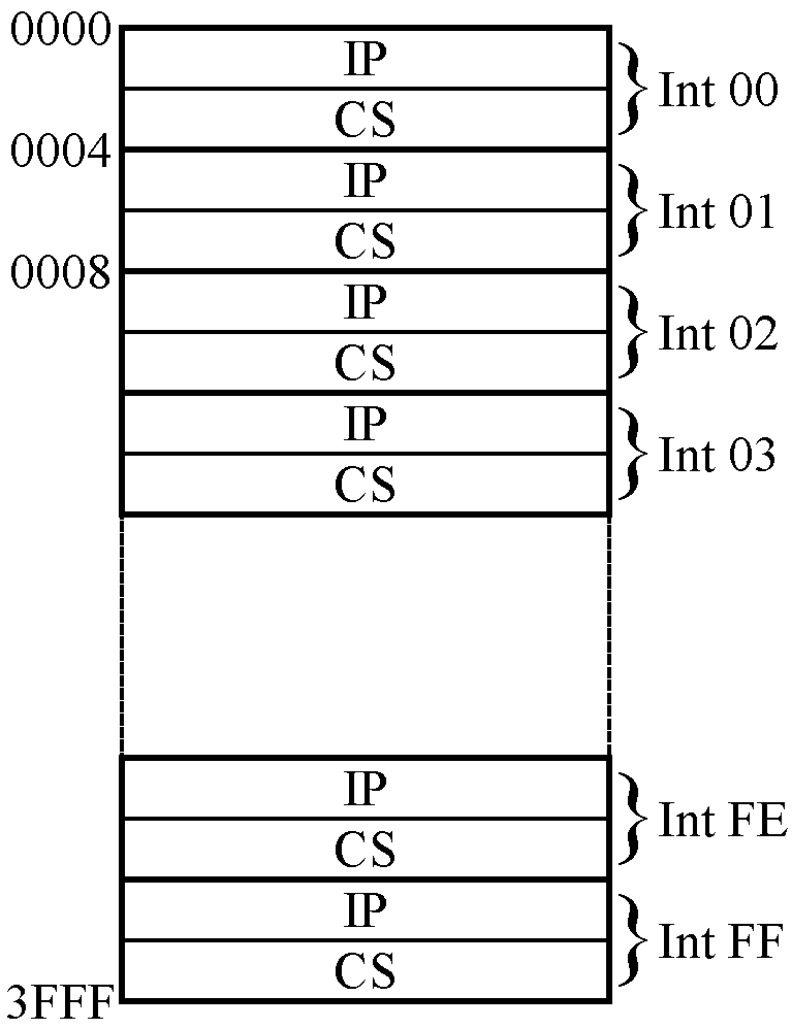
- Interrupts
  - 4 types
    - INT – maskable interrupt hardware input
    - NMI – nonmaskable interrupt hardware input
    - Software interrupts – program-called (INT command)
    - Internal interrupts – automatically generated:
      - Division by 0
      - Single step (if T=1, executed after each command)
      - NMI
      - Breakpoint
      - Overflow (executed if O=1 during INTO command)

8086

- Interrupts (2)
  - INTR signal active until int. ack.
  - 2 int. ack. cycles (for 8259A):
    - Master-slave 8259A arbitration
    - 8259A provides interrupt ID
  - Interrupt accepted:
    - flags→stack
    - T=I=0
    - CS:IP→stack
    - CS:IP=int_vec_table[int_id]

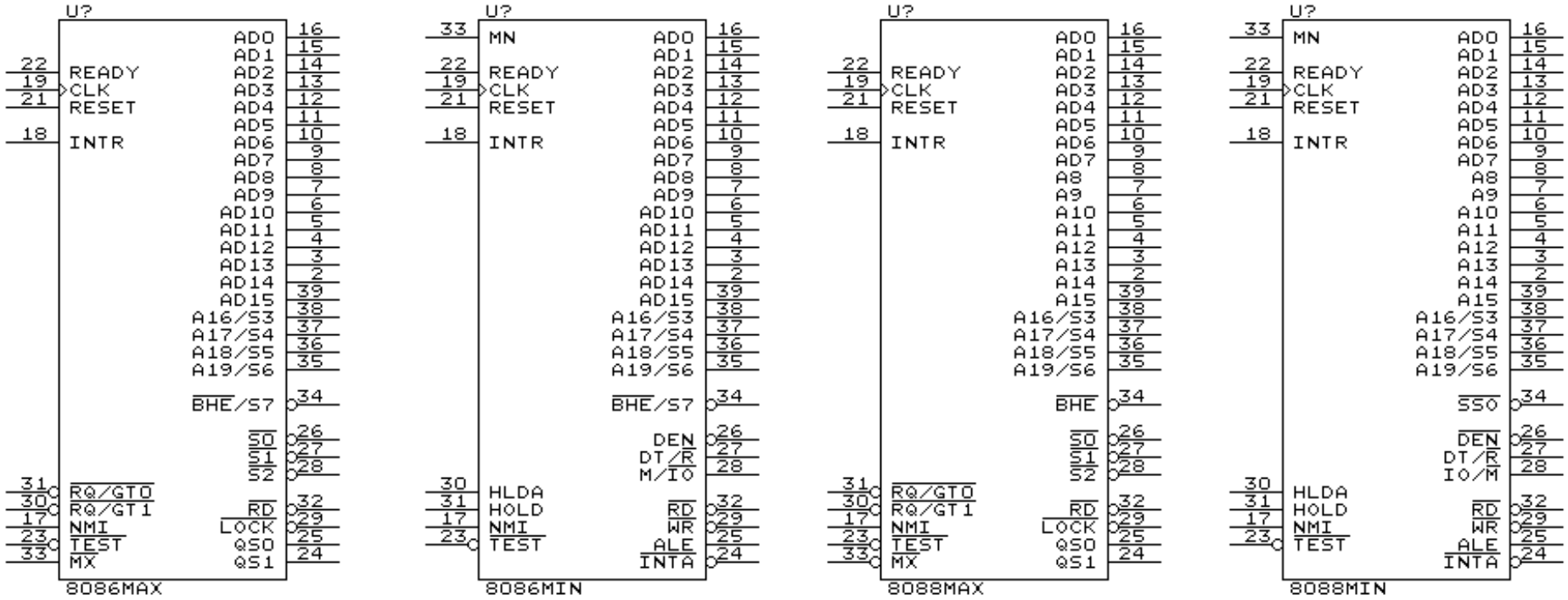
8086

- Interrupts (3) – vector table
  - Starts at 0000:0000
  - 256 cells × 4 bytes
  - Int 0÷4 – internal
  - Int 5÷31 – reserved
  - Int 32÷255 – available



8086

- Pins
  - 8086 or 8088
  - maximum or minimum mode



8086

- Pins

Common

$AD_{0..15}$

$A_{16..19}/S_{3..6}$

BHE/S_7

RD

READY

INTR

TEST

NMI

RESET

CLK

minimum

M/IO

WR

INTA

ALE

DT/R

DEN

HOLD

HLDA

maximum

$S_{0..2}$

$RQ/GT_{0..1}$

LOCK

$QS_{0..1}$

$S_{2..0}$	Machine cycle
000	Interrupt acknowledge
001	I/O read
010	I/O write
011	Halt
100	Fetch
101	Mem read
110	Mem write
111	No cycle

8086

- Pins (2)

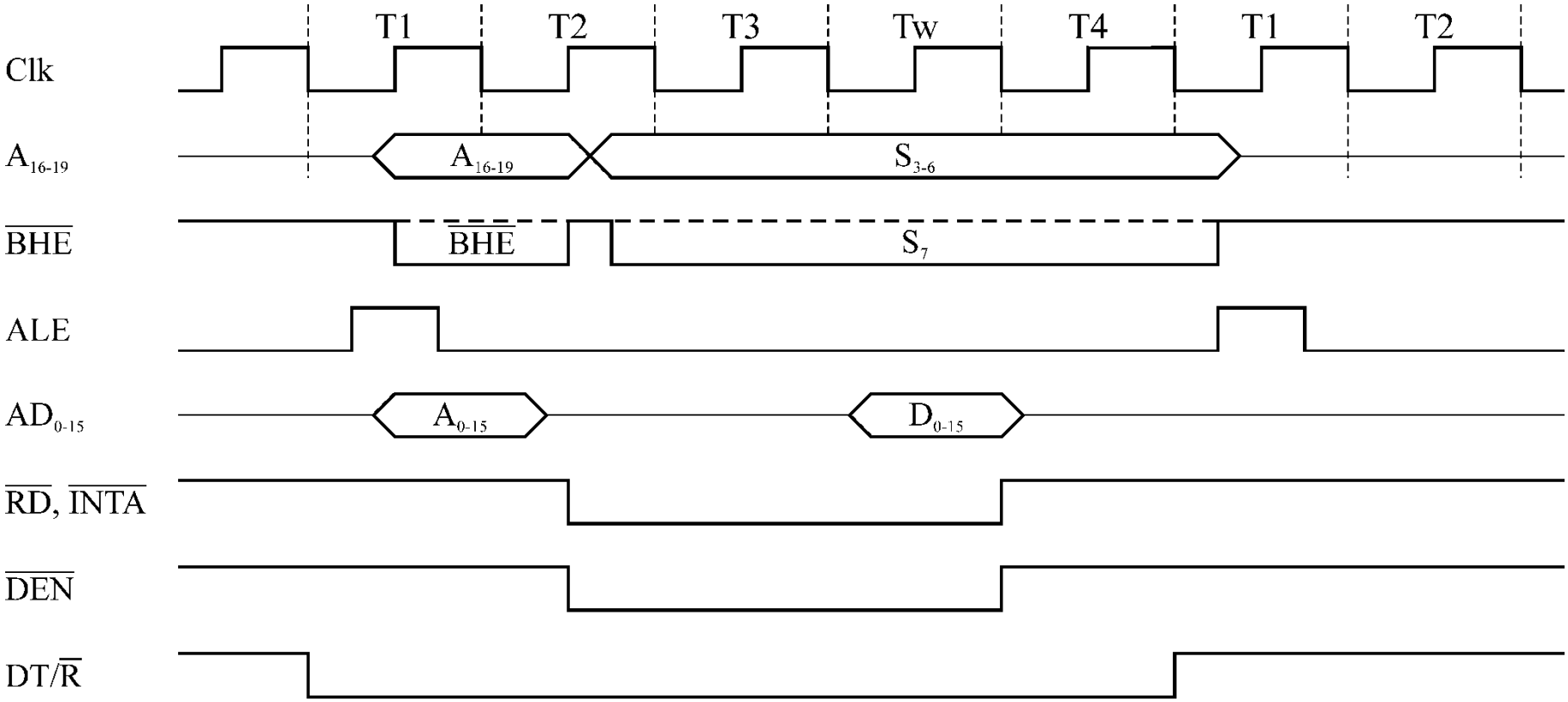
$S_{6..3}$	Machine cycle
0---	Bus manager by 8086
-1--	Interrupts enabled
--00	ES segment
--01	SS segment
--10	CS segment
--11	DS segment

BHE	A0	Read/write
0	0	Entire word
0	1	MSB (odd address)
1	0	LSB (even address)
1	1	No operation

$QS_{1..0}$	Machine cycle
00	No operation
01	1st byte fetched from queue
10	Queue empty
11	Next byte fetched from queue

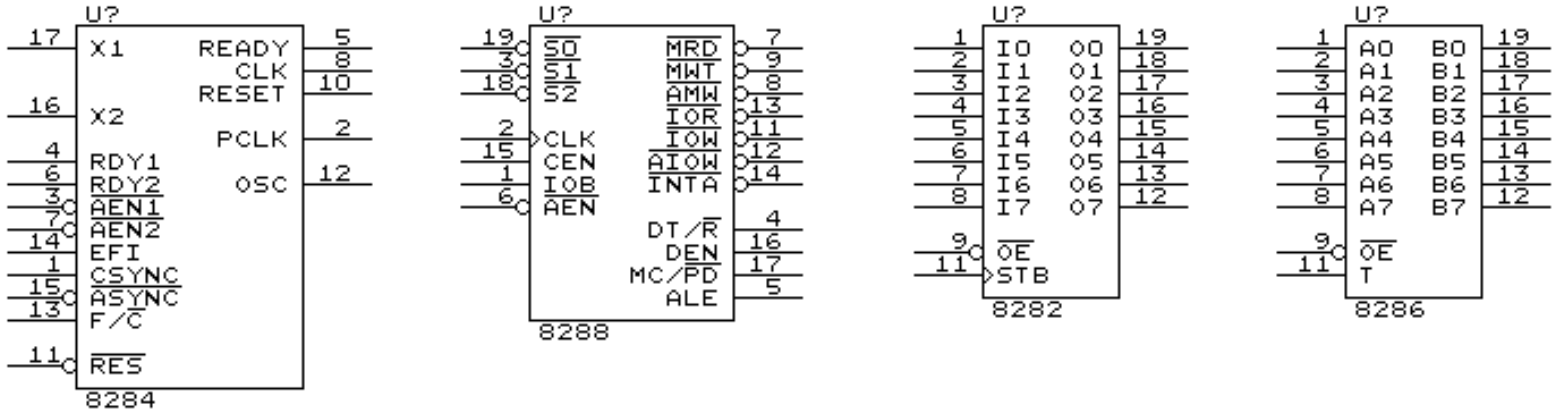
8086

- Bus operation



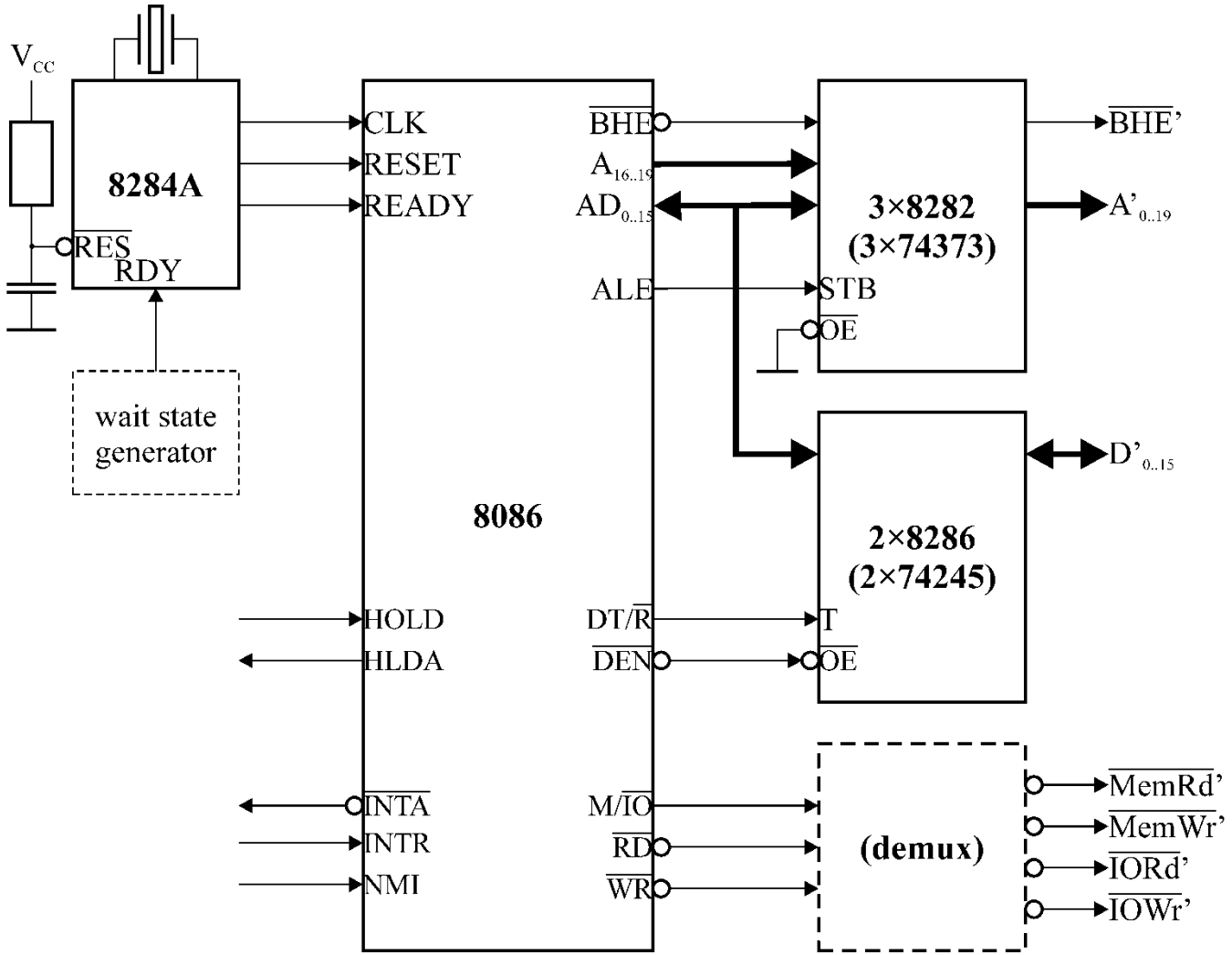
8086

- Central unit – supporting IC's
  - 8284 – clock/reset/wait generator
  - 8282 – 8-b latch register with 3-state outputs
    - Similar to 74373, 74573
  - 8286 – 8-b bi-directional 3-state buffer
    - Similar to 74245
  - 8288 – bus controller for maximum mode



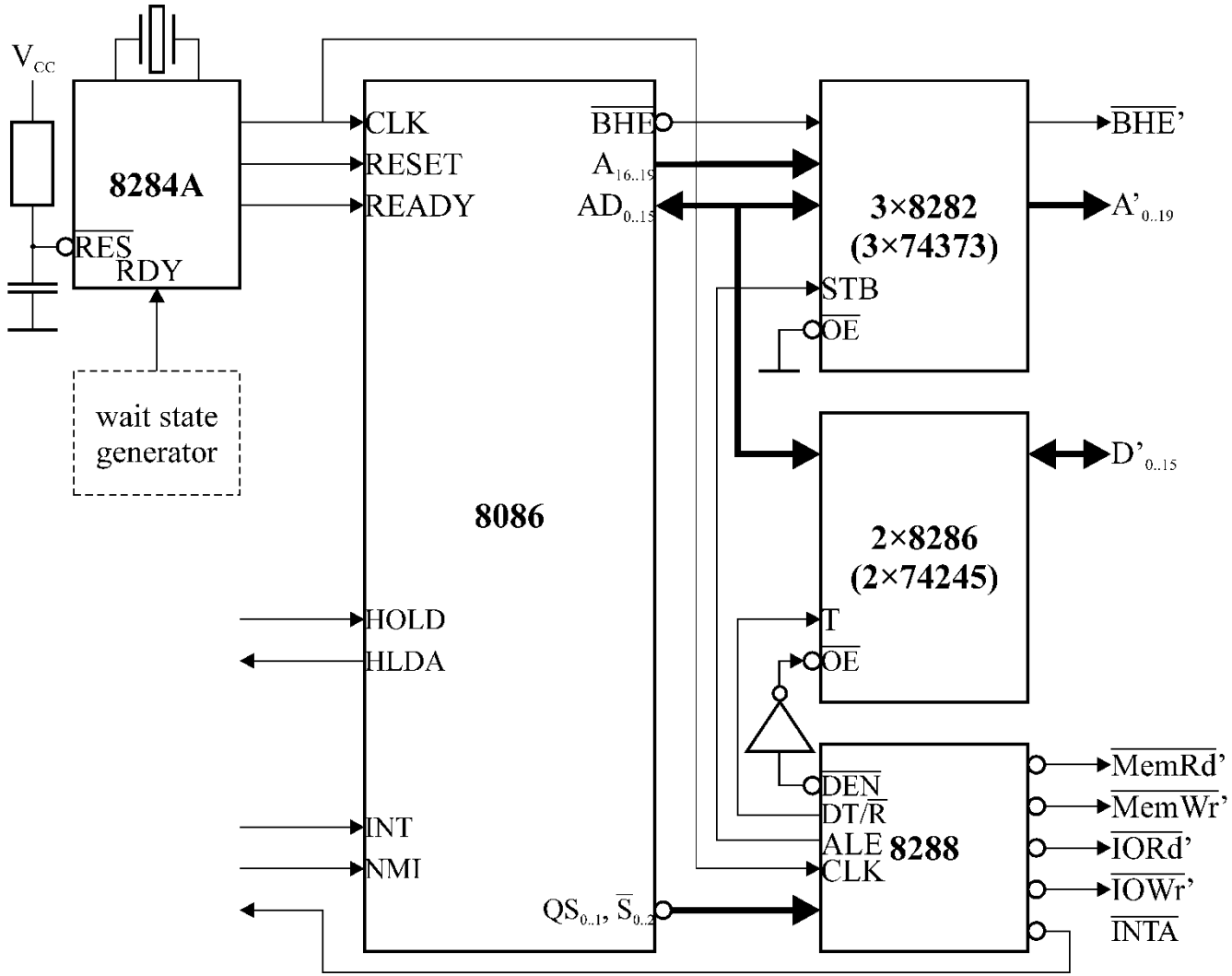
8086

- Central unit – minimum mode



8086

- Central unit – maximum mode



8288:

- Multibus-compatible signals
- Additional „advance” write signals for slower devices, no wait state necessary

8086

- Memory attachment
  - 1MB = 2×(512k×8)
  - 16-b access possible