Fundusze Europejskie
Wiedza Edukacja Rozwój

Rzeczpospolita Polska

Unia Europejska
Europejski Fundusz Społeczny

Politechnika Śląska jako Centrum Nowoczesnego Kształcenia
opartego o badania i innowacje

POWR.03.05.00-IP.08-00-PZ1/17

Projekt współfinansowany przez Unię Europejską ze środków Europejskiego Funduszu Społecznego

Microprocessor and Embedded Systems

Faculty of Automatic Control, Electronics and Computer Science, Informatics, Bachelor Degree

Lecture 7

Interrupt controllers

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Interrupt controllers

Program:

- Interrupt controller functions
- Interrupt controllers:
  - Simple: 8214
  - Complex, flexible, programmable: 8259(A)

Interrupt controllers

- Interrupt controller functions
  - Interrupt source recognition
  - Priority control
  - Interrupt mask control
  - Informing the µp what to do

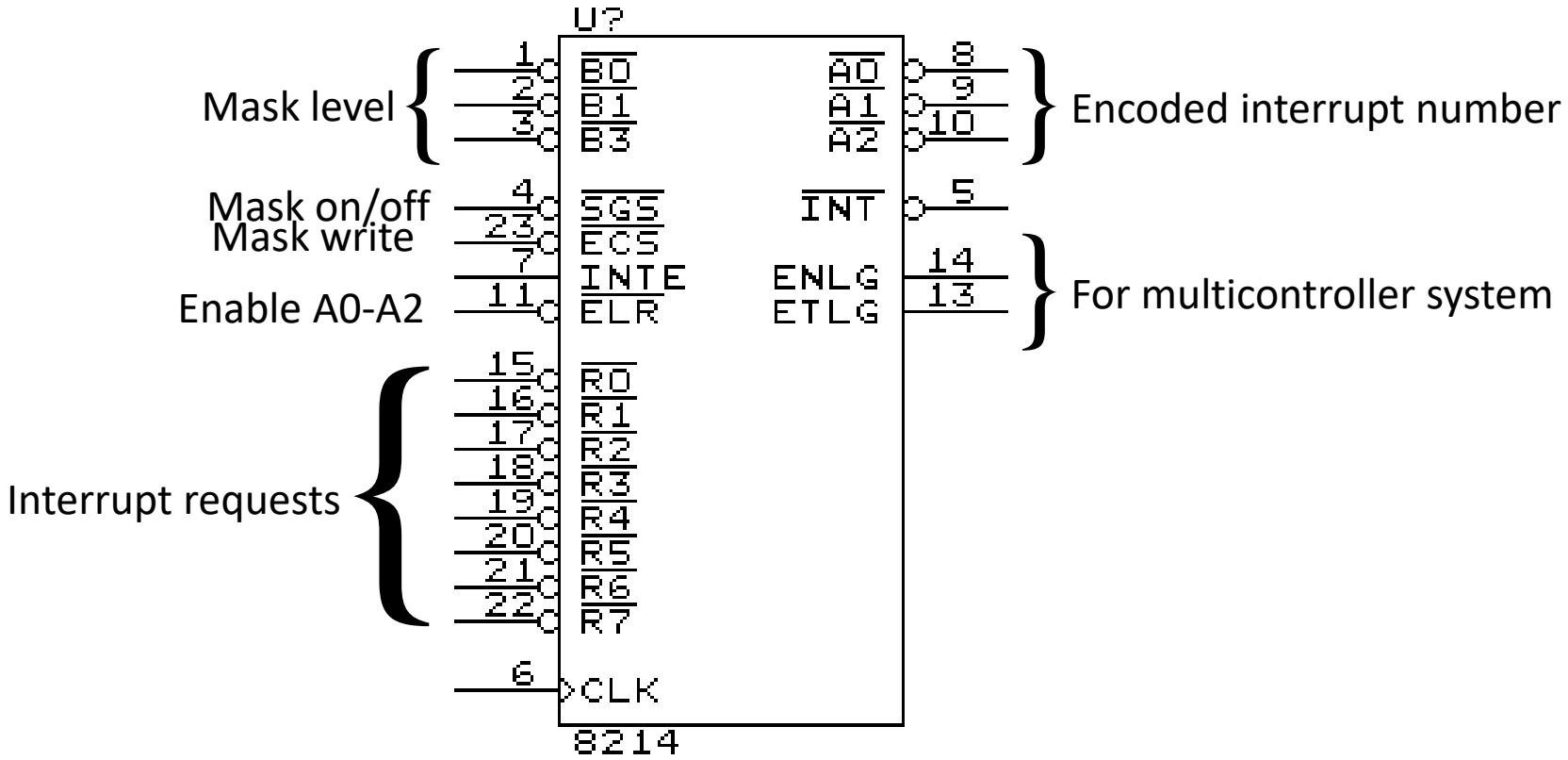
- Possible implementations
  - Separate IC (e.g., Intel)
  - „Distributed interrupt controller” (e.g., Zilog)
    - Lower cost (?), better scalability

Interrupt controllers

- Intel 8214
  - Simple interrupt controller
    - *or maybe a complex priority encoder?*
  - (almost) programmable
  - Constant (hierarchical) priority system
  - No individual masking
    - Configurable mask level

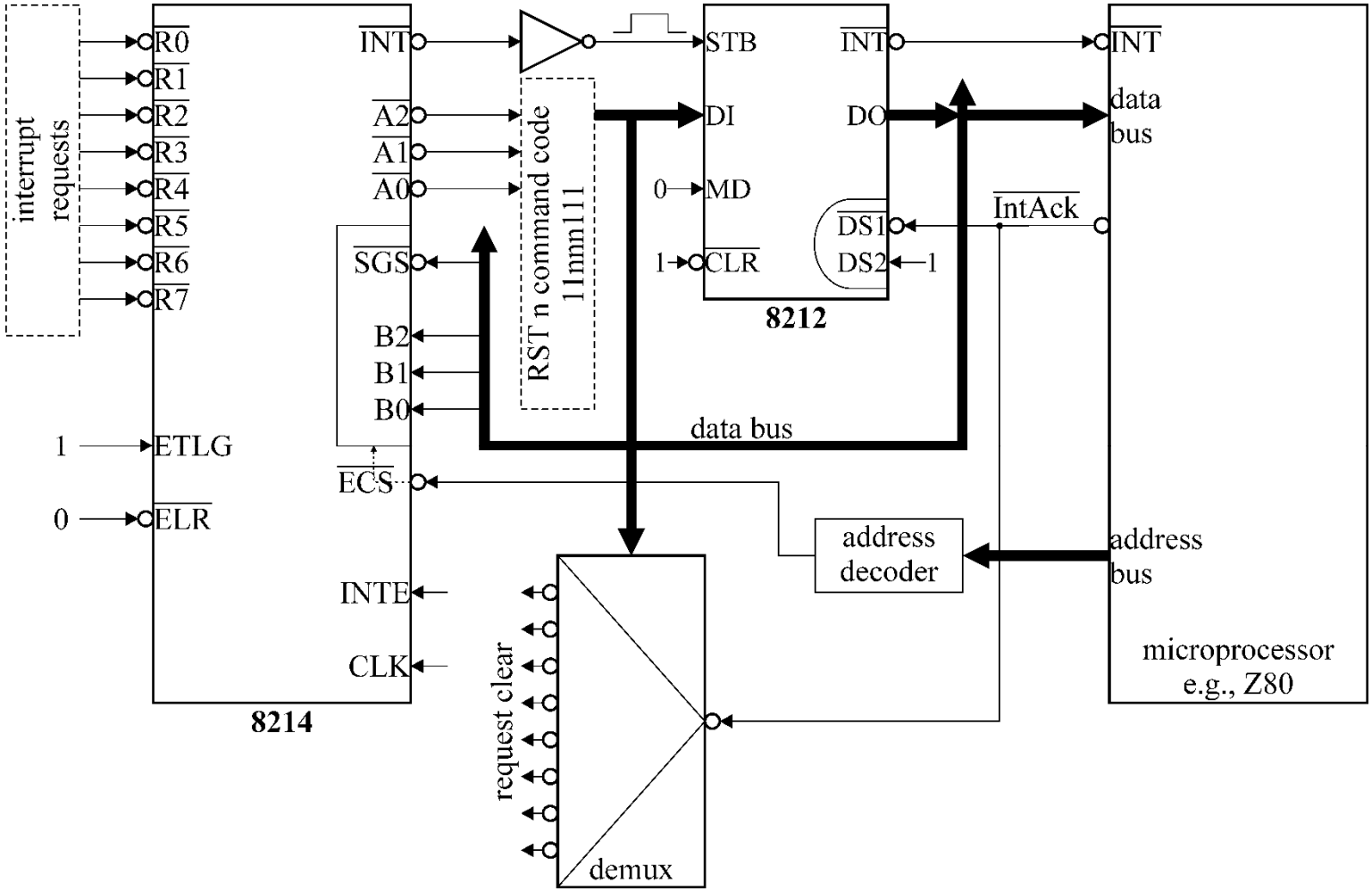
Interrupt controllers

- Intel 8214 circuit pins



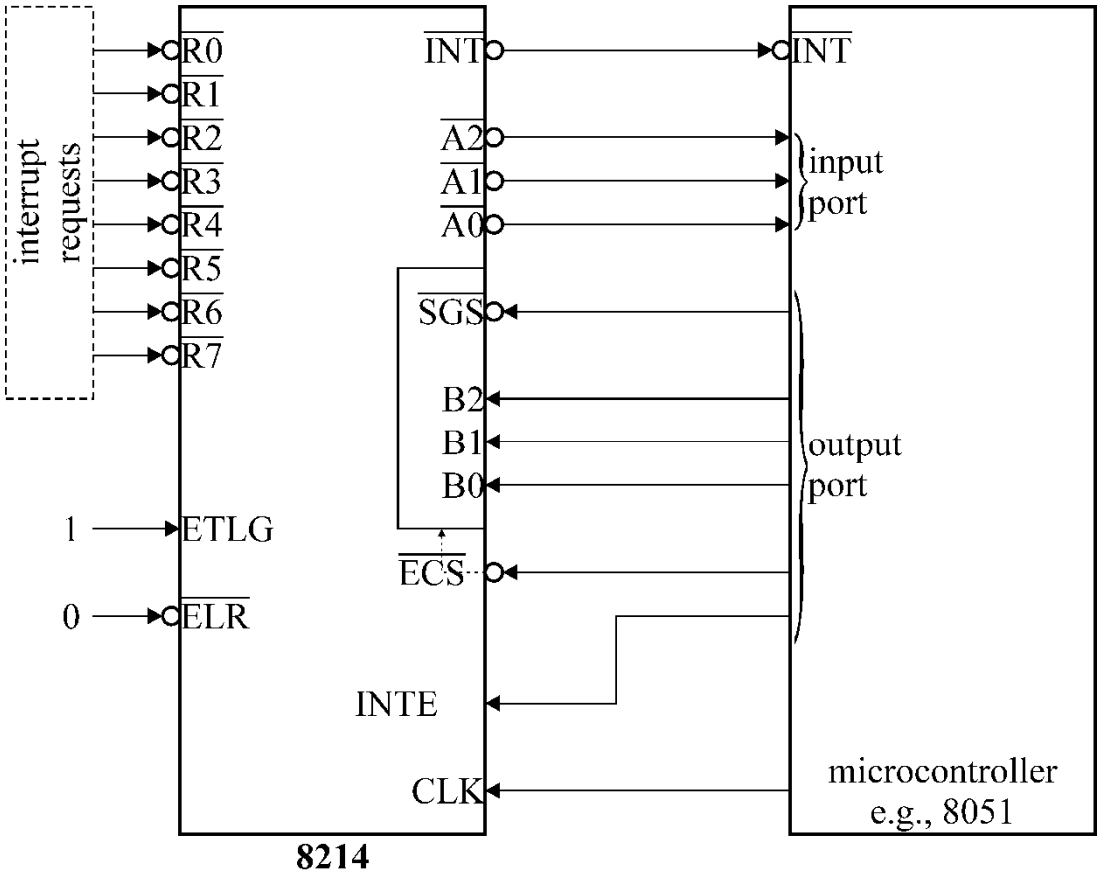
Interrupt controllers

- Intel 8214 application
  - For Z80 & similar microprocessors



Interrupt controllers

- Intel 8214 application
  - For 8051 & similar microcontrollers

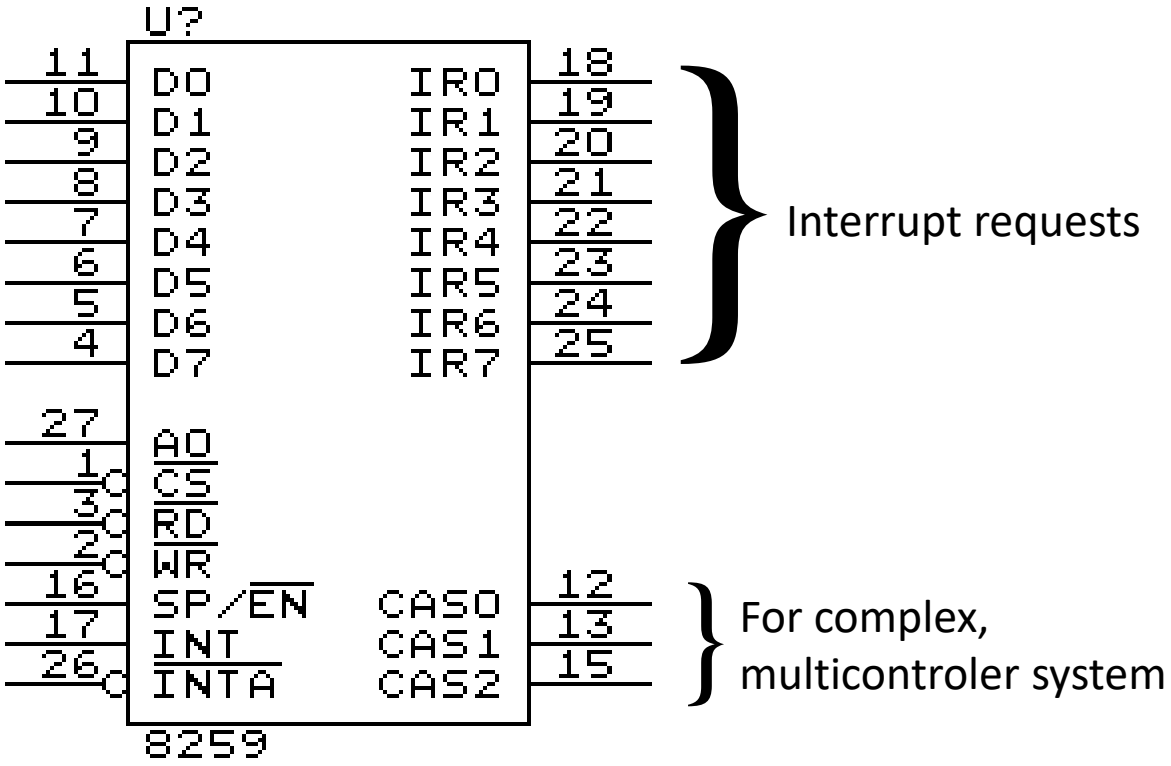


Interrupt controllers

- Intel 8214 disadvantages
  - Request signal active until interrupt service
    - *Otherwise µp may miss the request*
  - Request signal must be software cleared
    - *Otherwise µp will think it's the next request*
  - No information about interrupt service procedure placement
    - Only interrupt ID is given
    - On the other hand, it's like it's done nowadays
- *… but it's a simple controller anyway…*

Interrupt controllers

- Intel 8259 circuit pins

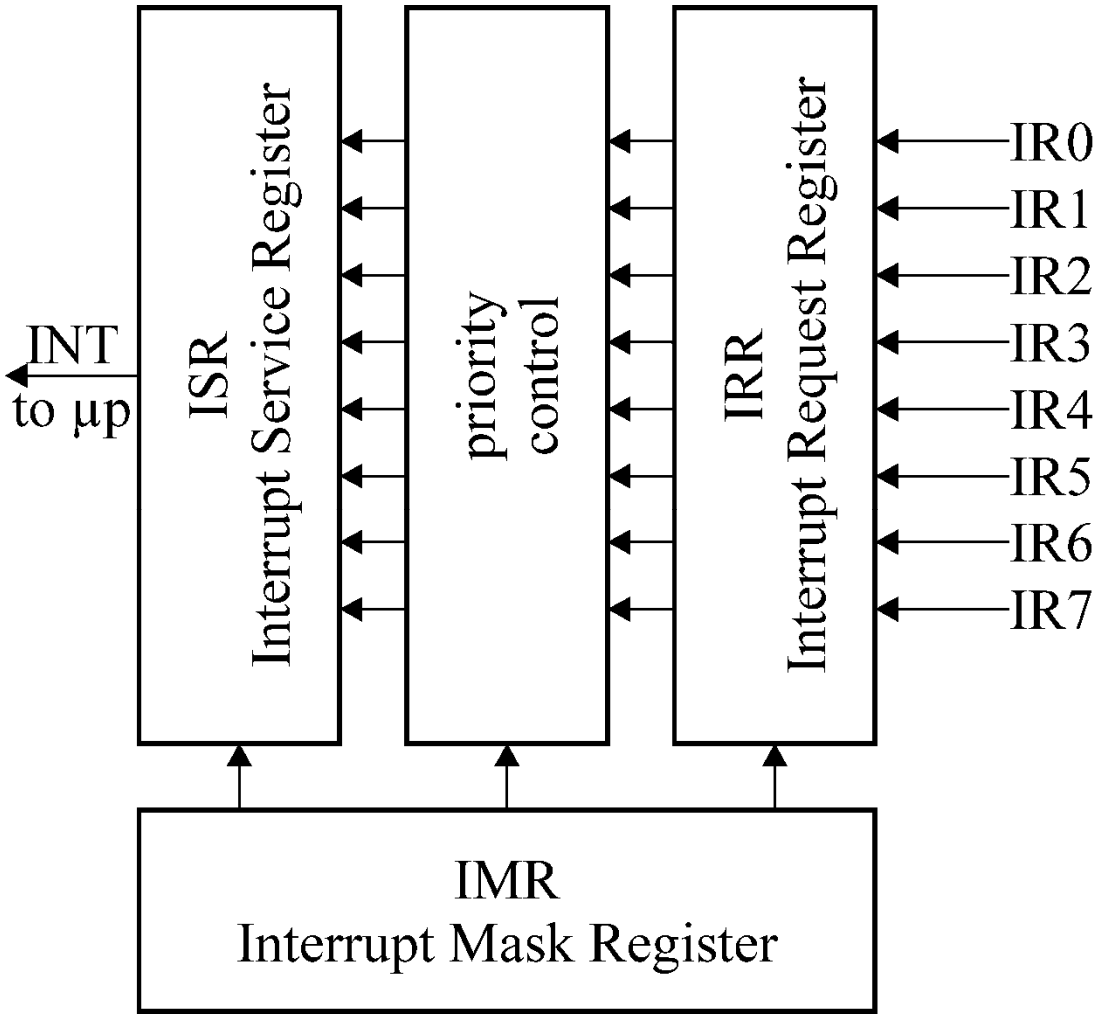


Interrupt controllers

- Intel 8259A properties
  - Up to 8 fully hardware-recognised interrupts
    - Individual masking
  - Few priority assignment methods
    - Hierarchical (static)
    - Rotating priority (dynamic)
    - Special masking
    - Polling mode
  - Few End-of-Interrupt possibilities
  - Complex system in cascade (Master/Slave) configuration

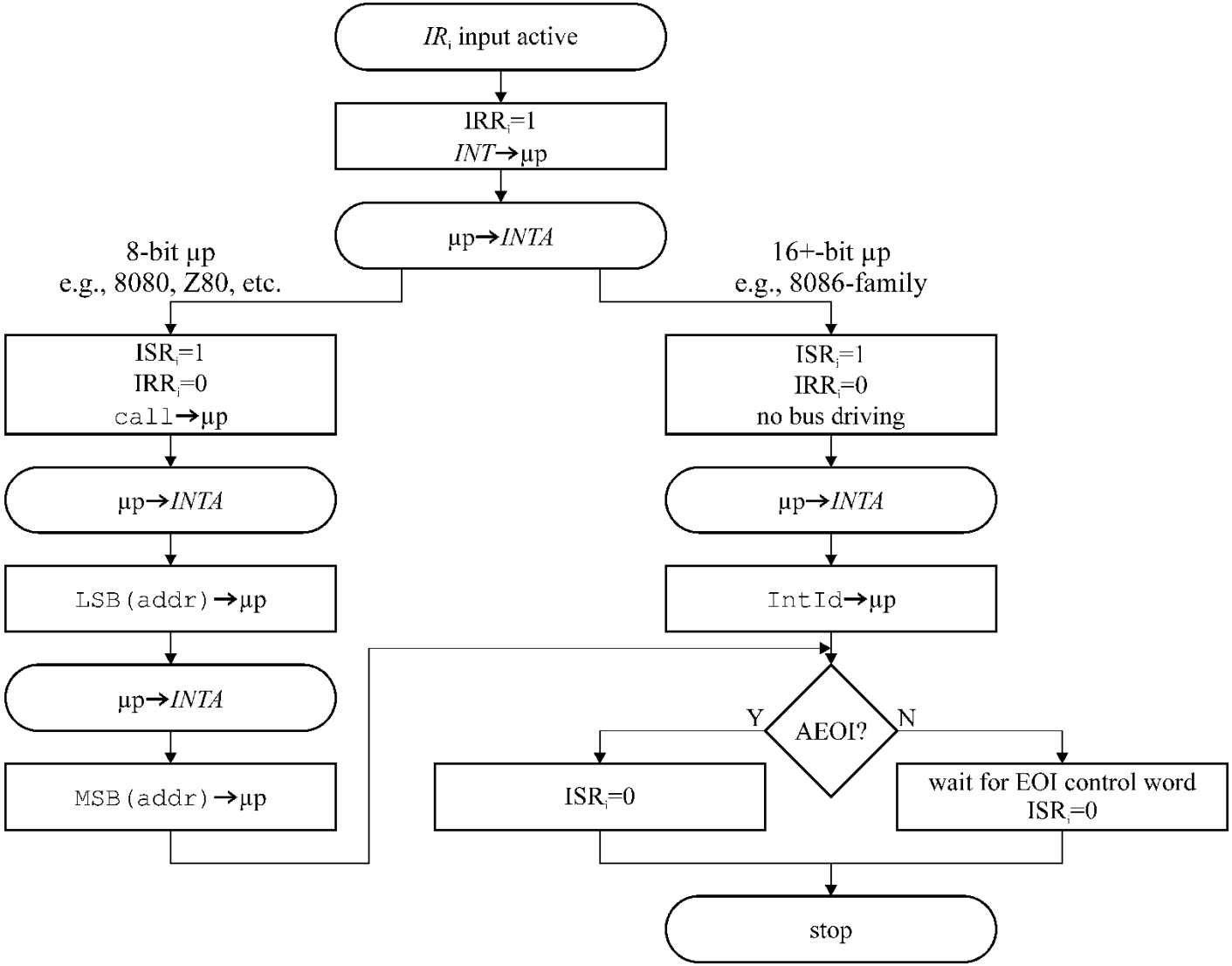
Interrupt controllers

- Intel 8259A structure



Interrupt controllers

- Intel 8259A interrupt processing

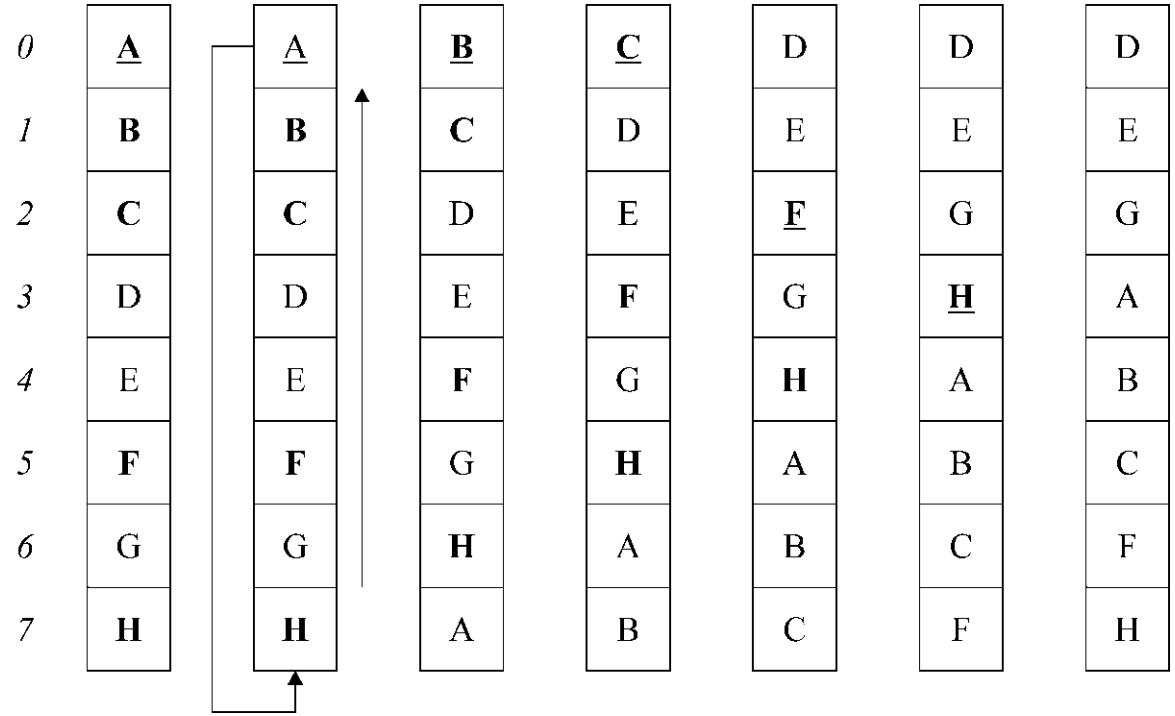


Interrupt controllers

- Intel 8259A priority modes (1)
  - Fully Nested Mode
    - Static assignment: IR0 highest … IR7 lowest priority
    - Level *N* being served → levels **≥***N* auto masked
  - Special Fully Nested Mode
    - Similar to Fully Nested Mode
    - Level *N* being served → levels **>***N* auto masked
      - Level *N* not masked
    - Useful for Master in a cascade system
    - Allows to accept interrupt from currently served Slave

Interrupt controllers

- Intel 8259A priority modes (2)
  - Rotating Priority Mode
    - Dynamic assignment
      - Interrupt just served is „rewarded” with the lowest priority
      - Remaining interrupts go one level higher in the hierarchy



Interrupt controllers

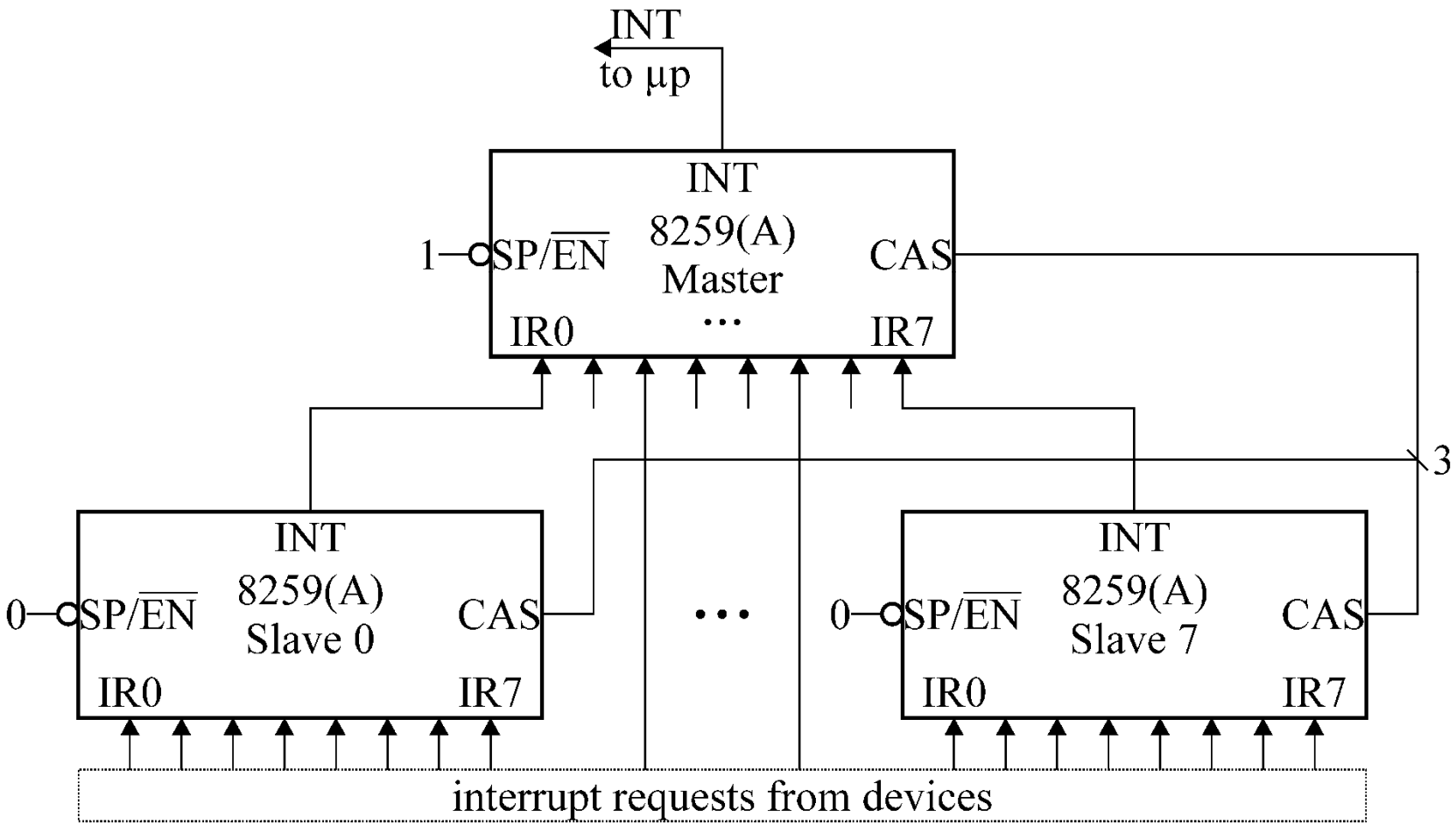
- Intel 8259A priority modes (3)
  - Special Masking Mode
    - Can accept interrupts of a lower priority than currently being served
  - Polled Mode
    - INT line not used
    - Interrupts status software returned by a command

Interrupt controllers

- Intel 8259A complex system
  - Up to 1 Master and 8 Slave circuits
  - Up to 64 fully hardware-recognised interrupts
  - Master: a bitmap tells where slaves are connected
  - Slaves: must know the Master IR input
  - CAS bus: during IntAck, selects a Slave to complete the cycle
  - IntID sent from:
    - Selected Slave, if request went through slave
    - Master, if request went directly to the master
  - IBM PC/AT: 1 Master, 1 Slave, 15 interrupts

Interrupt controllers

- Intel 8259A cascade system

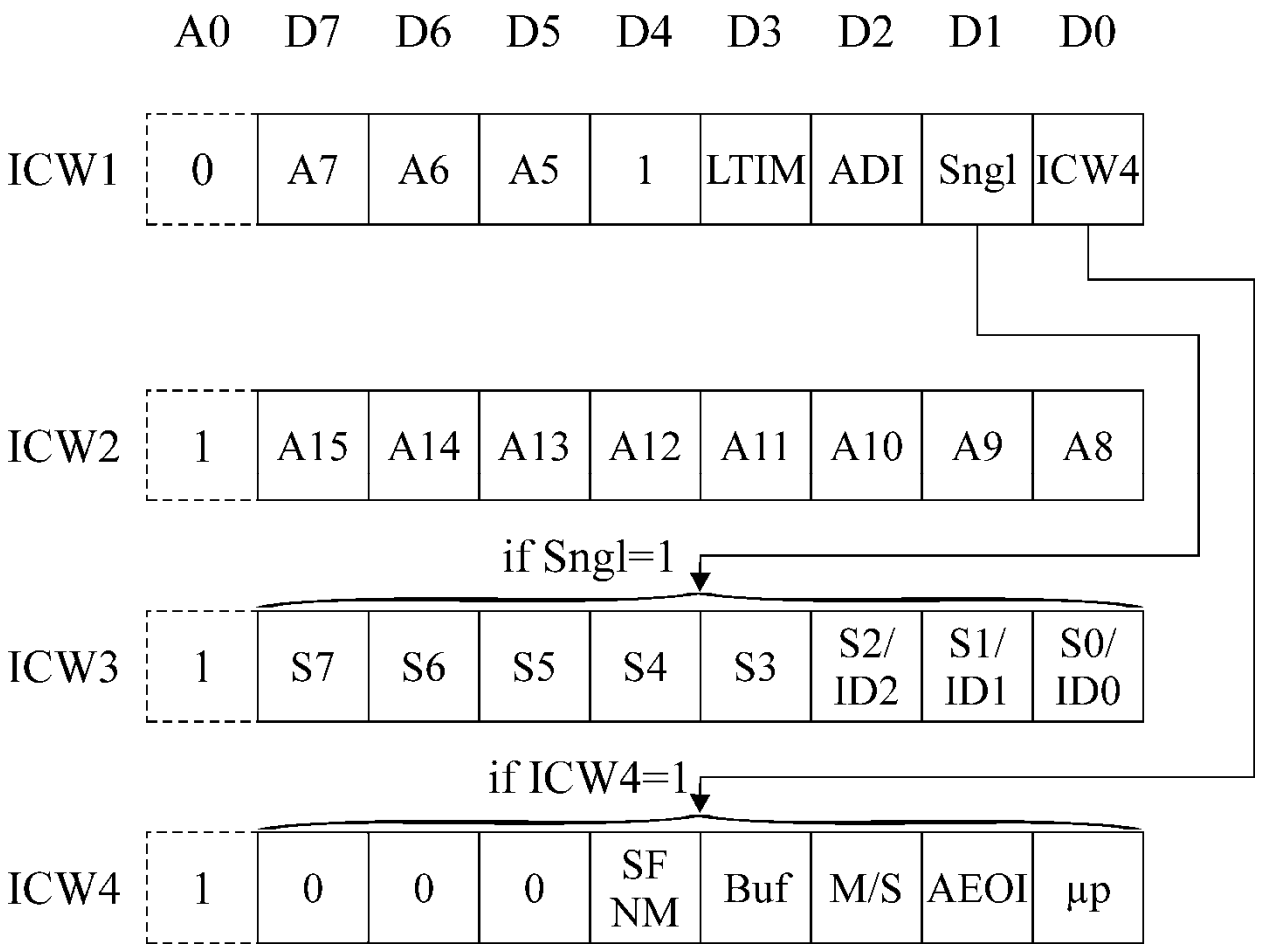


Interrupt controllers

- Intel 8259A programming
  - Initialisation command words
    - ICW1 – general options
    - ICW2 – higher part of address/interrupt ID
    - ICW3 – for cascade systems
    - ICW4 – additional options (8259A)
  - Operation command words
    - OCW1 – mask control
    - OCW2 – EOI, priority rotation
    - OCW3 – register read, special mask mode

Interrupt controllers

- Intel 8259A programming
  - Initialisation sequence



Interrupt controllers

- Intel 8259A programming
  - ICW1, ICW2

	D7	D6	D5	D4	D3	D2	D1	D0
ICW1	A7	A6	A5	1	LTIM	ADI	Sngl	ICW4
ICW2	A15	A14	A13	A12	A11	A10	A9	A8

  - ICW4 – ICW4 present
  - Sngl – single/multi controller interrupt system (ICW3!)
  - ADI – 4 or 8 bytes between iterrupt service procedures
  - LTIM – IR inputs edge or level sensitive
  - A15-A5 – higher adress bits of interrupt service procedures (for 8-b µp)
  - A15-A11 – common IntID part (for 16-b µp)
    - A10-A8 = INT input number

Interrupt controllers

- Intel 8259A programming
  - ICW3, ICW4

	D7	D6	D5	D4	D3	D2	D1	D0
ICW3	S7	S6	S5	S4	S3	S2/ ID2	S1/ ID1	S0/ ID0
ICW4	0	0	0	SF NM	Buf	M/S	AEOI	µp

- S7-S0 (Master) – slave connection bitmap
- ID3-ID0 (Slaves) – master INT number

- AEOI – Automatic End Of Interrupt
- M/S – Master/Slave (in Buffered mode)
- Buf – Buffered mode
- SFNM – Special Fully Nested Mode
- µp – µp type: 8-bit (8080/8085) / 16-bit (8086)

Interrupt controllers

- Intel 8259A programming
  - OCW1:
    - M7-M0 – mask bits
  - OCW2:
    - R, SL, EOI – EOI commands, priority rotation
    - L2-L0 – interrupt number for EOI/rotation
  - OCW3:
    - RR, RIS – read IRR or ISR on the nearest $\overline{\mathrm{RD}}$
    - P – poll command
    - SMM, ESMM – set or reset Special Mask Mode

	A0	D7	D6	D5	D4	D3	D2	D1	D0
OCW1	1	M7	M6	M5	M4	M3	M2	M1	M0
OCW2	0	R	SL	EOI	0	0	L2	L1	L0
OCW3	0	0	E SMM	SMM	0	1	P	RR	RIS

Interrupt controllers

- Intel 8259A programming
  - EOI types
    - Non-specific EOI: reset the highest ISR active bit
    - Specific EOI: reset the ISR bit specified by L2-L0
      - When not in Fully Nested Mode
    - AEOI: non-specific EOI automatically performed
  - Priority rotation:
    - Non-specific EOI + priority rotation
    - Specific EOI + priority rotation
    - Set/clear rotation on AEOI
    - Specific rotation only

Interrupt controllers

- Intel 8259A programming
  - Poll mode
    - Send OCW3 with P=1
    - On the nearest $\overline{\mathrm{RD}}$, status is given as follows:

I	—	—	—	—	L2	L1	L0

      - L2-L0 – highest priority level requesting interrupt
      - I – if any interrupt is active
  - Buffered mode
    - $\mathrm{SP}/\overline{\mathrm{EN}}$ used to control external buffer
    - Master/Slave selection software-set only

Interrupt controllers

- Intel 8259A programming
  - Word/register addressing summary

A0	D4	D3	$\overline{RD}$	$\overline{WR}$	action
0			0	1	Read IRR or ISR
1			0	1	Read IMR
0	0	0	1	0	Write OCW2
0	0	1	1	0	Write OCW3
0	1	*	1	0	Write ICW1
1	*	*	1	0	Write ICW2, ICW3, ICW4 or OCW1