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Microprocessor and Embedded Systems

Faculty of Automatic Control, Electronics and Computer Science, Informatics, Bachelor Degree

Lecture 6

Serial input/output circuits
Programmable timers/counters

Bartłomiej Zieliński, PhD, DSc

Serial IO/Timers

Program:

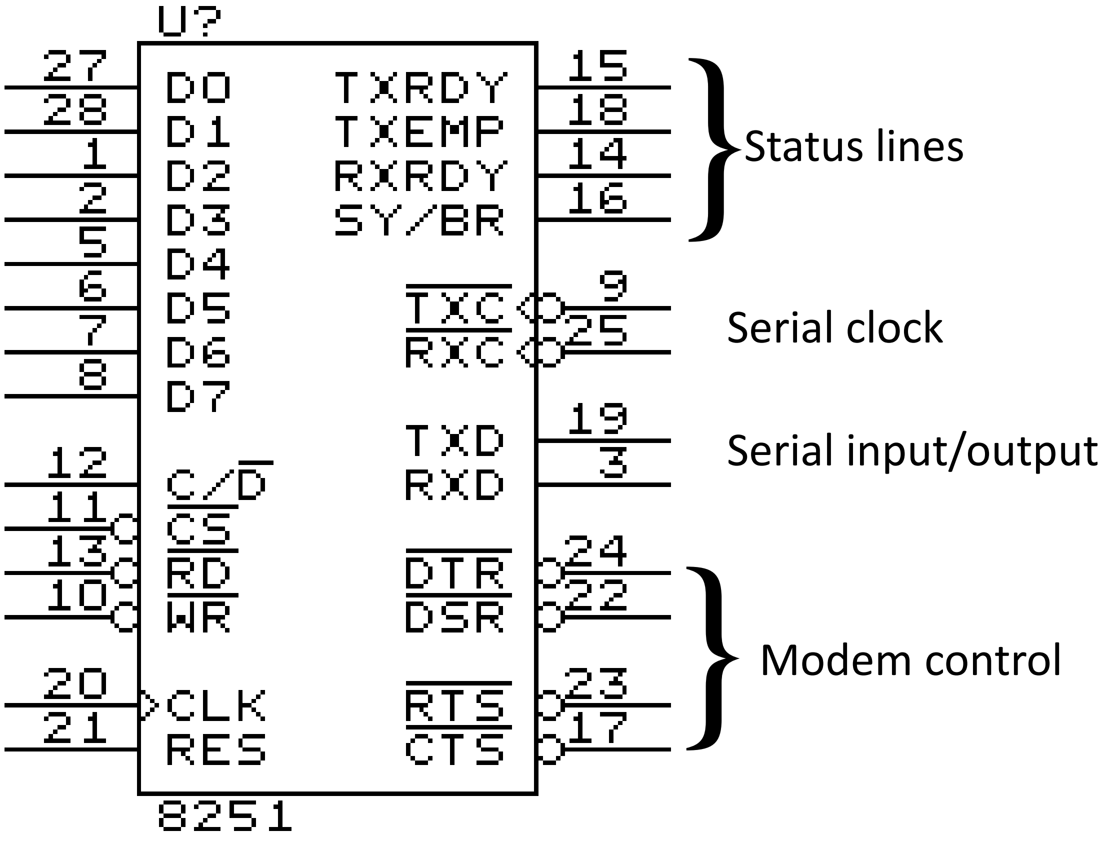
- Serial IO circuits
  - Intel 8251
  - Zilog Z80 SIO (brief)
- Timers/counters
  - Intel 8253
  - Zilog Z80 CTC

Serial IO

- Intel 8251 circuit
  - Programmable serial IO circuit
  - USART (**U**niversal **S**ynchronous/**A**synchronous **R**eceiver/**T**ransmitter)
  - Asynchronous
    - RS-232 compatible character format
    - Modem control
    - No built-in timer for transmission rate setting
  - Synchronous
    - Programmable synchronisation word(s)

Serial IO

- Intel 8251 circuit pins



Serial IO

- Serial IO + clock
  - Separate I/O signals
  - Separate clock
    - Different Tx/Rx transmission rates
  - Signals:
    - TxD (*Transmitter Data)* →
    - RxD (*Receiver Data)* ←
    - TxC (*Transmitter Clock)* ←
    - RxC (*Receiver Clock)* ←

Serial IO

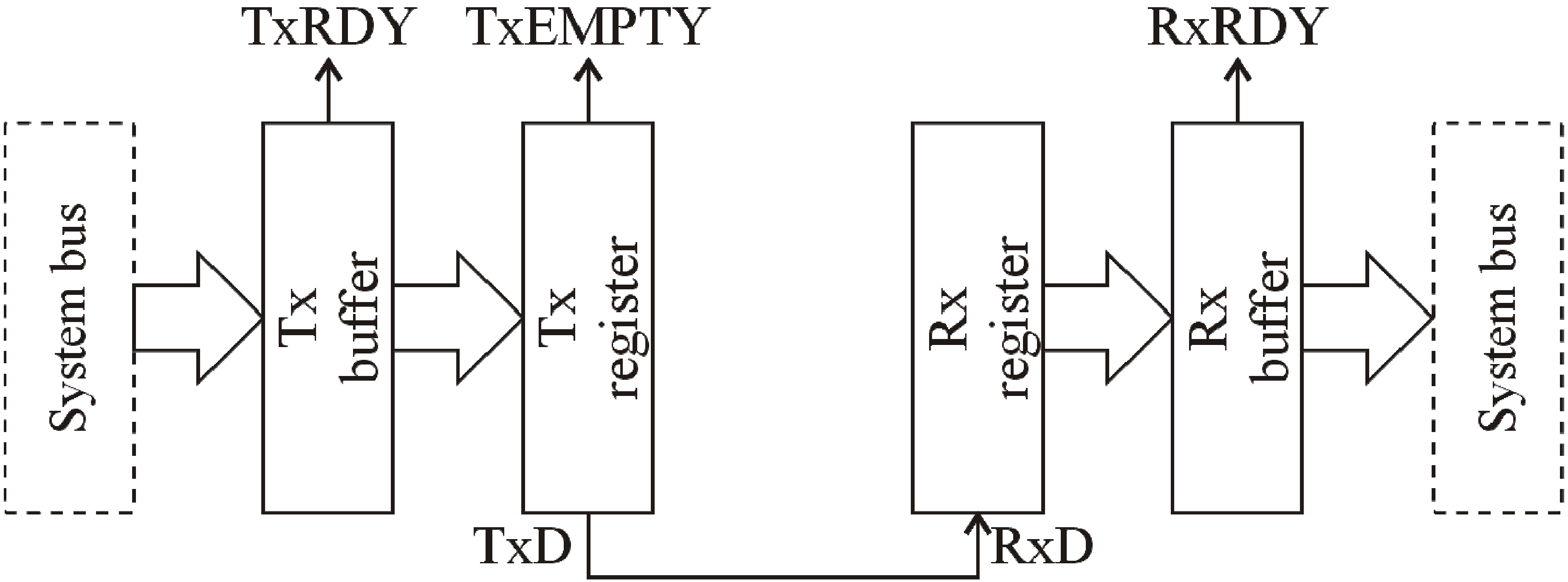
- Modem control
  - Comes from RS-232 standard
    - DTE (*Data Terminal Equipment*)
      - eg., computer, controller, etc.
    - DCE (*Data Communications Equipment*)
      - eg., modem, network card, etc.
  - Signals
    - DTR (*Data Terminal Ready*) →
    - DSR (*Data Set Ready*) ←
    - RTS (*Ready To Send*) →
    - CTS (*Clear To Send*) ←

Serial IO

- Status
  - Hardware signals
    - RxRDY (*Receiver Ready)* →
    - TxRDY (*Transmitter Ready)* →
    - TxEMPTY (*Transmitter Empty)* →
    - SynDet/BrkDet ↔
      - Synchronous transmission: *Synchronisation Detected*
        - » Input or output
      - Asynchronous transmission: *Break Detected*
  - Software status register read

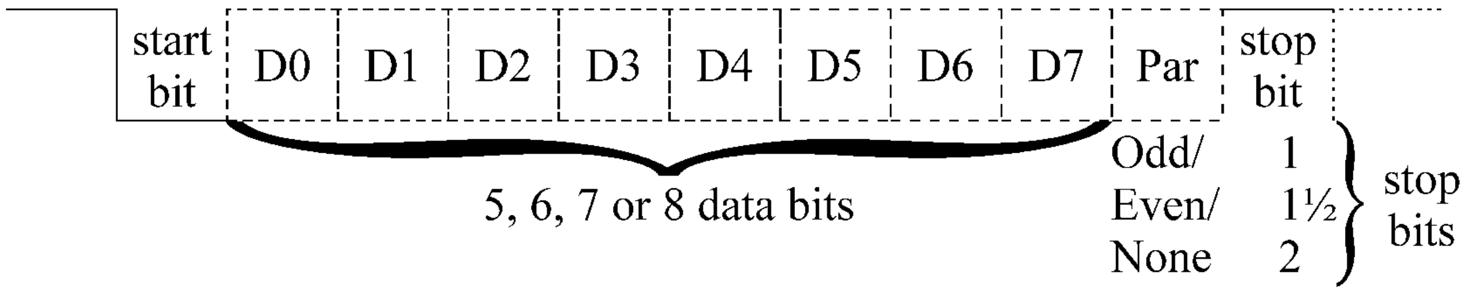
Serial IO

- Transmission model

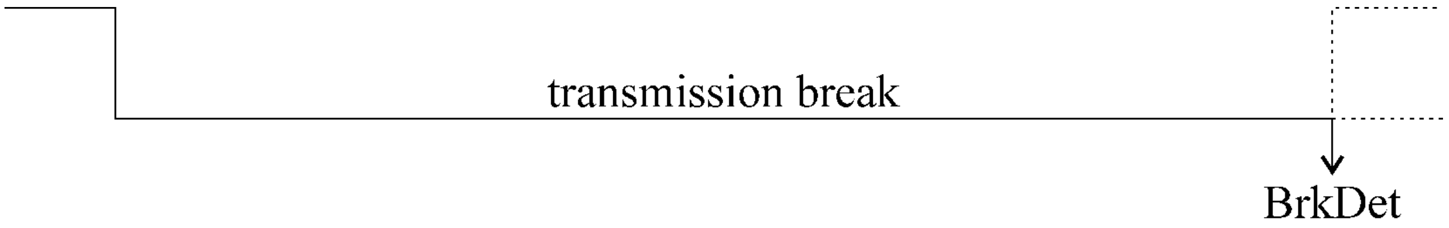


Serial IO

- Asynchronous transmission
  - Character format

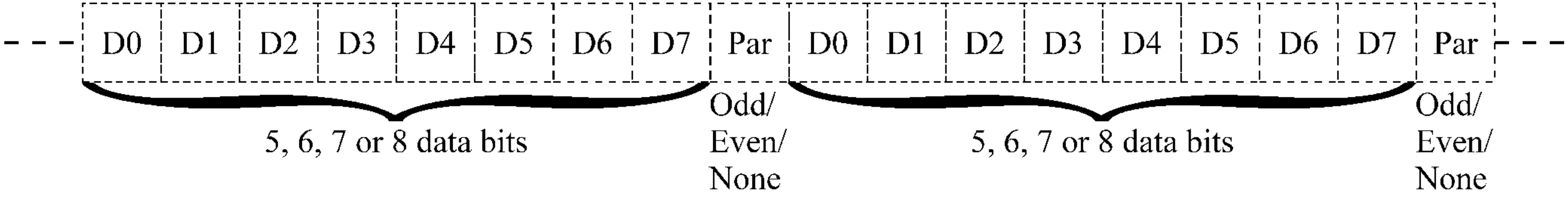


  - Break condition & signalling

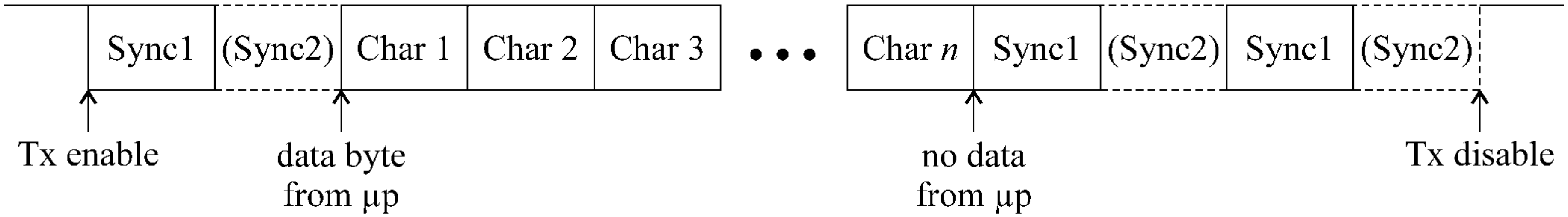


Serial IO

- Synchronous transmission
  - Character format

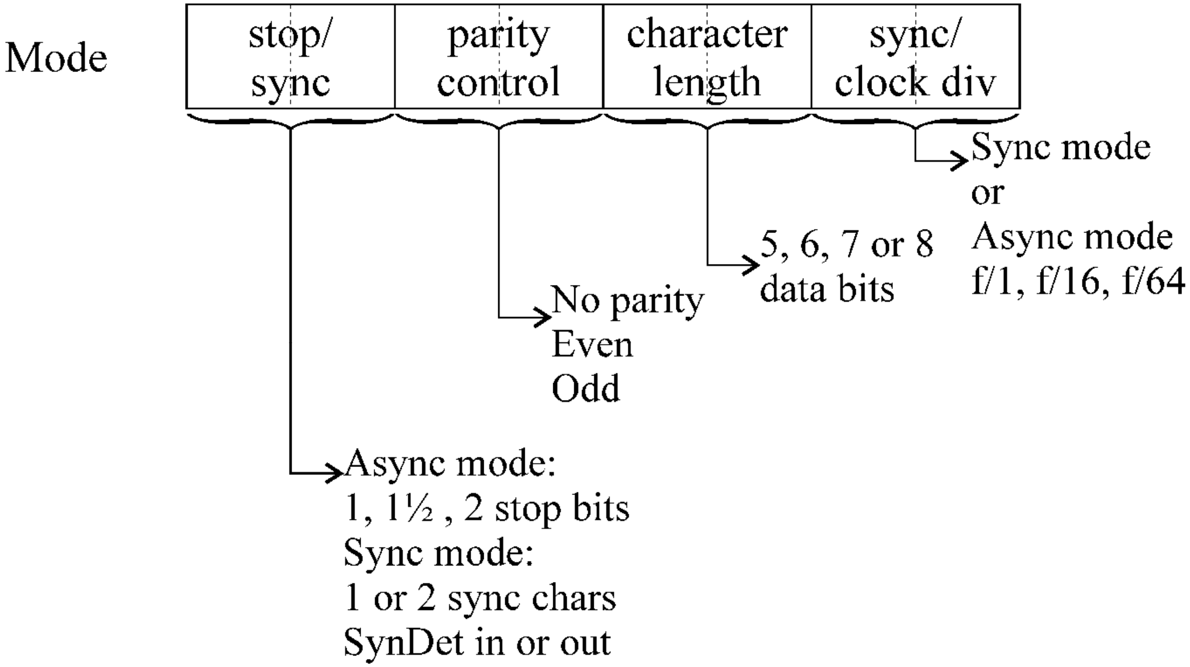


  - Information format



Serial IO

- Programming
  - Mode word



Mode

stop/ sync

parity control

character length

sync/ clock div

Sync mode
or
Async mode
f/1, f/16, f/64

5, 6, 7 or 8
data bits

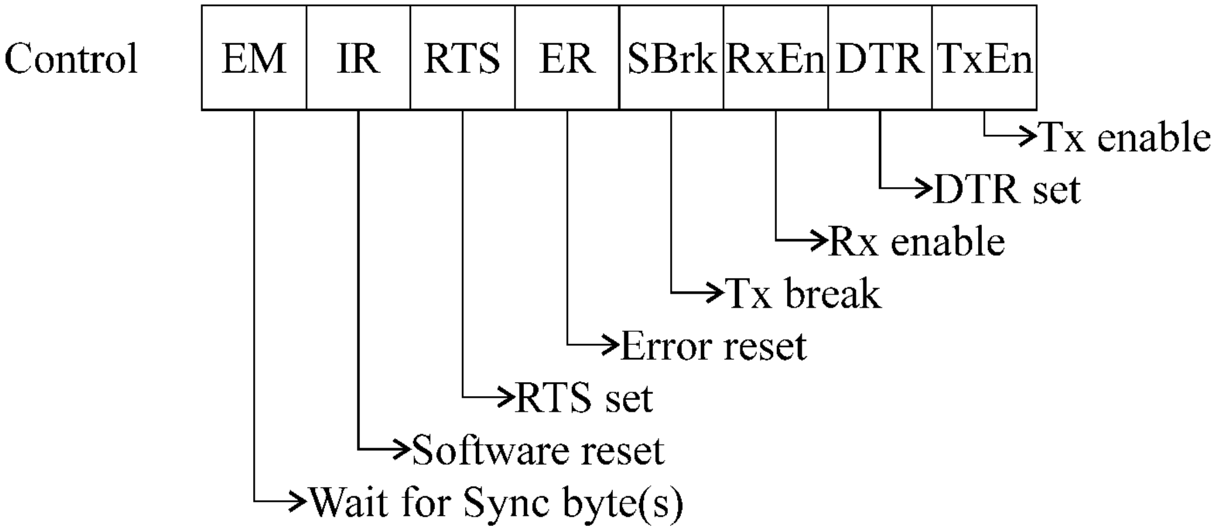
No parity
Even
Odd

Async mode:
1, 1½ , 2 stop bits
Sync mode:
1 or 2 sync chars
SynDet in or out

- If Sync mode selected, after Mode word, 1-2 Sync bytes

Serial IO

- Programming
  - Control word



Control	EM	IR	RTS	ER	SBrk	RxEn	DTR	TxEn

Tx enable

DTR set

Rx enable

Tx break

Error reset

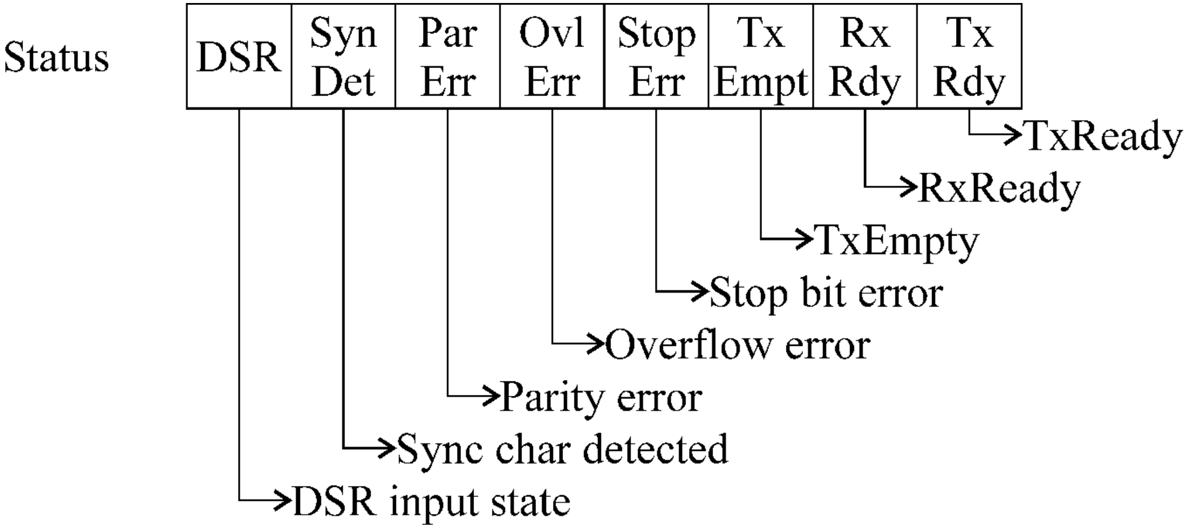
RTS set

Software reset

Wait for Sync byte(s)

Serial IO

- Programming
  - Status word



Status								
	DSR	Syn Det	Par Err	Ovl Err	Stop Err	Tx Empt	Rx Rdy	Tx Rdy

→TxReady

→RxReady

→TxEmpty

→Stop bit error

→Overflow error

→Parity error

→Sync char detected

→DSR input state

Serial IO

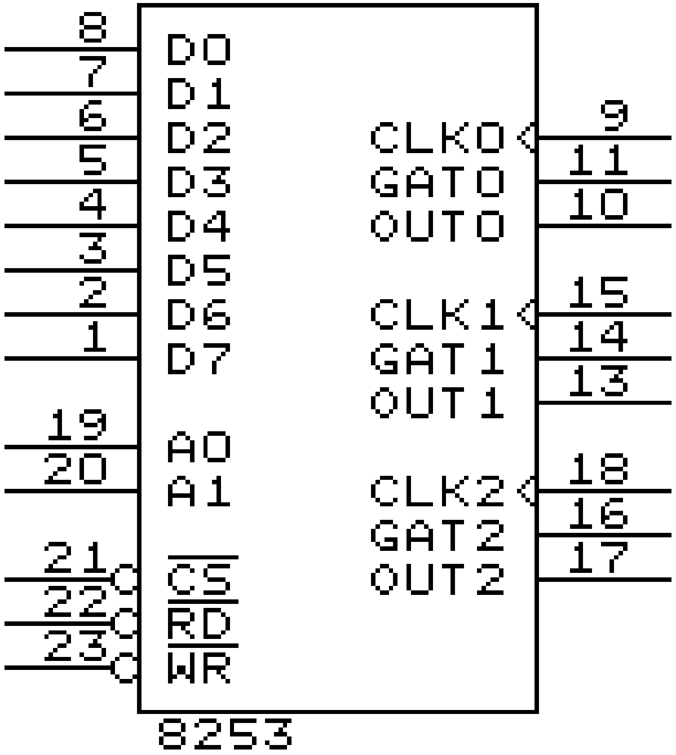
- Other serial transmission IC’s
    - Z80 SIO (*Serial Input/Output*)
        - 2 serial syn/asyn serial ports
            - Asyn: RS-232 compatible
            - Syn: IBM Bisync, SDLC, HDLC, AX.25 protocols
                - » Automatic CRC calculation, transmission and check
                - » Automatic sync character insertion and removal
                - » Bit stuffing
    - 8530/82530
        - Z80 SIO for µp others than Z80
    - 8250/16450/16550…16950
        - Single serial port for PC-class computers

Timers/counters

- Intel 8253
  - 3 independent, 16-bit counters
  - Binary/decimal counting
  - Count from initial value to 0
  - 6 modes
  - Mode-dependent Gate input
    - gate, trigger, clear

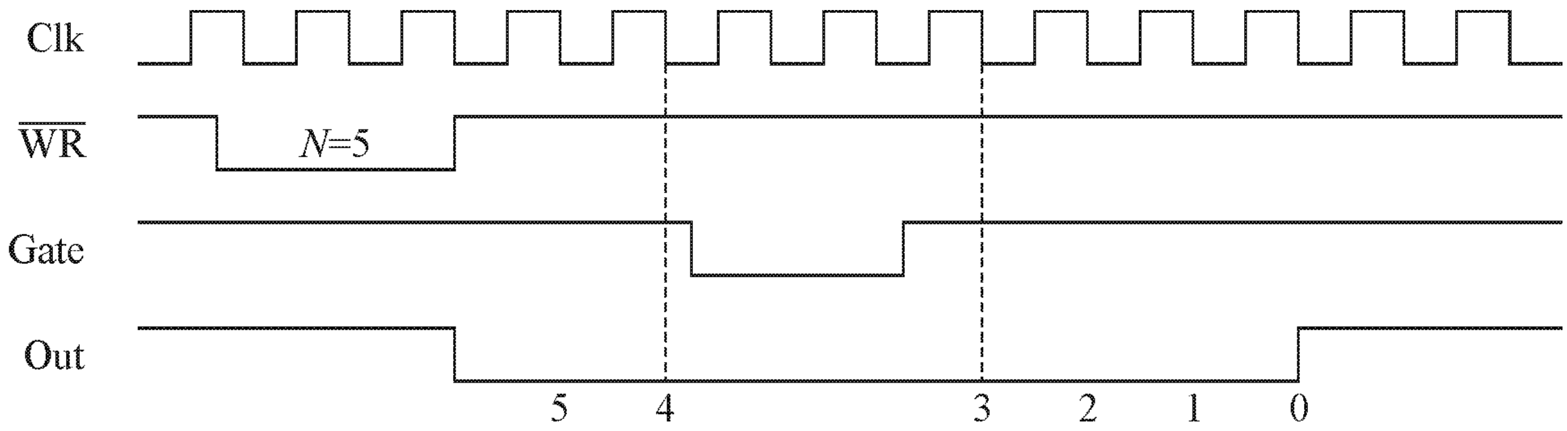
Timers/counters

- Intel 8253 circuit pins



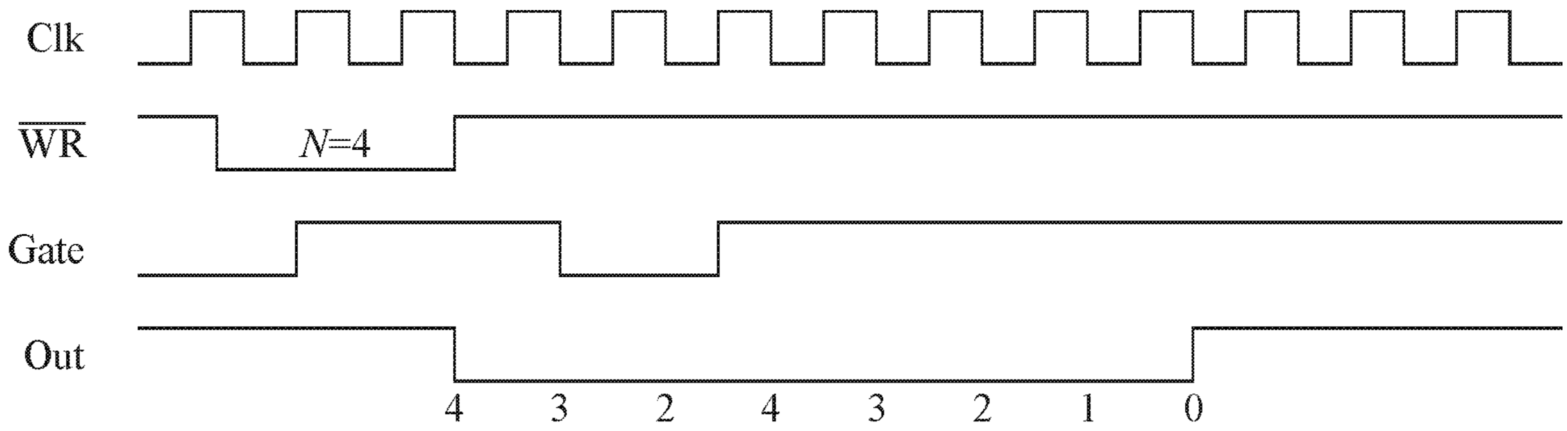
Timers/counters

- Intel 8253 modes
  - Mode 0: „counter”
    - Mode write: Out=0
    - Gate=0: disable count
    - Counted to 0: Out=1 and stop



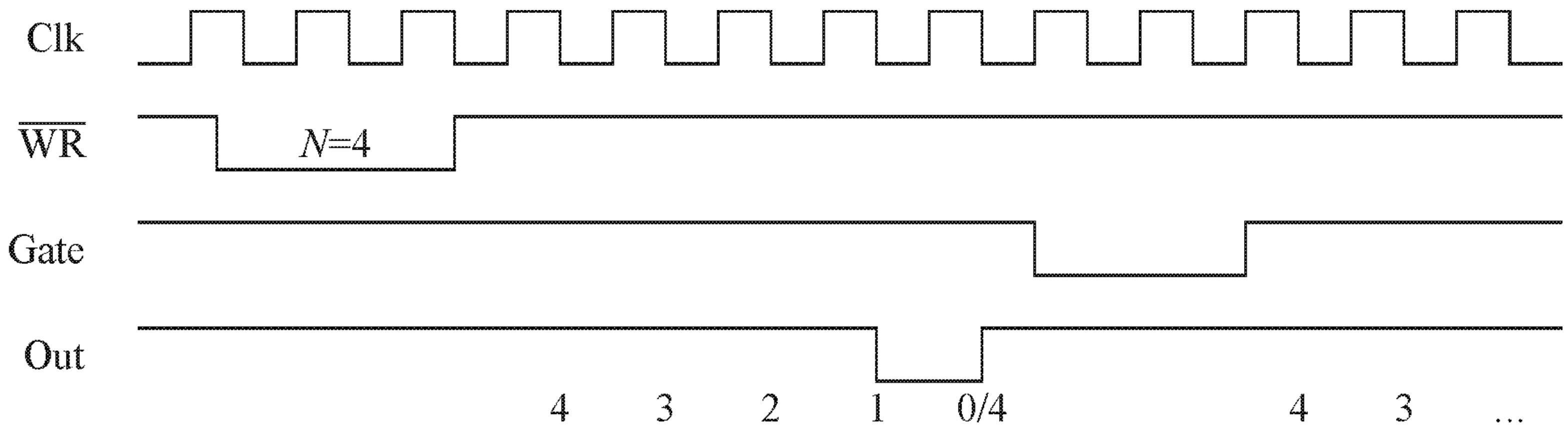
Timers/counters

- Intel 8253 modes
  - Mode 1: „one shot (univibrator)” (retriggerable)
    - Gate 0→1: count start, Out=0
    - Gate 0→1 during count: count restart
    - Counted to 0: Out=1



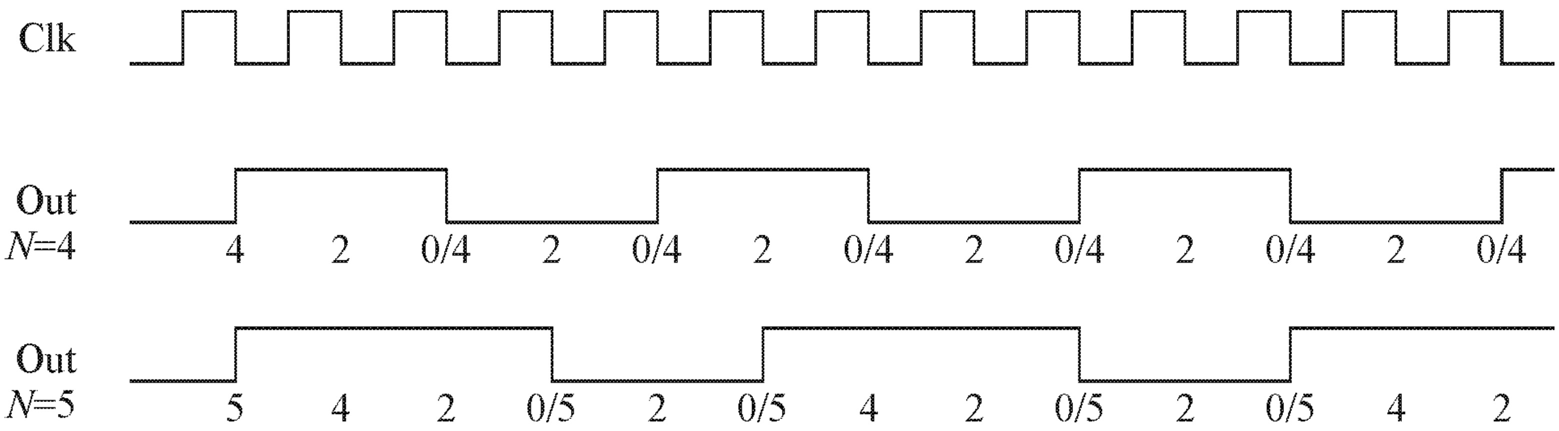
Timers/counters

- Intel 8253 modes
  - Mode 2: „rate generator” (divide-by-N counter)
    - Initially Out=1
    - Counted to 1: Out=0 for 1 T_{clk} and continue
    - Gate=1: enable; Gate=0: disable counting



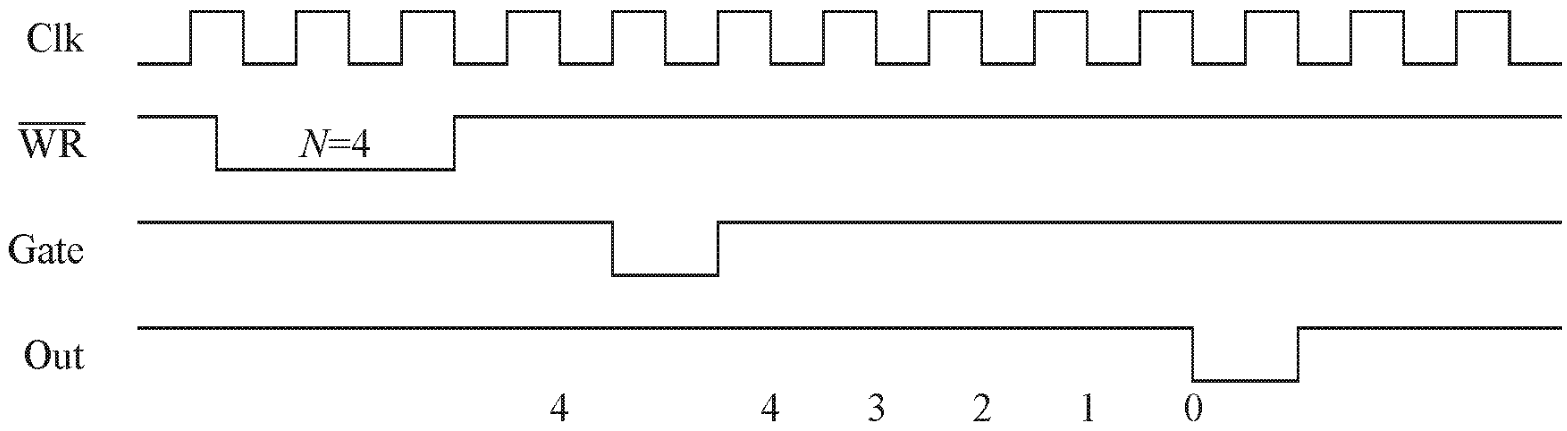
Timers/counters

- Intel 8253 modes
  - Mode 3: „square wave generator”
    - Gate 0→1: start counting (e.g., for synchronisation)
    - Counted to 0: $\mathrm{Out} = \overline{\mathrm{Out}}$
    - For each *N*, T_{Out}=*N*·T_{Clk}



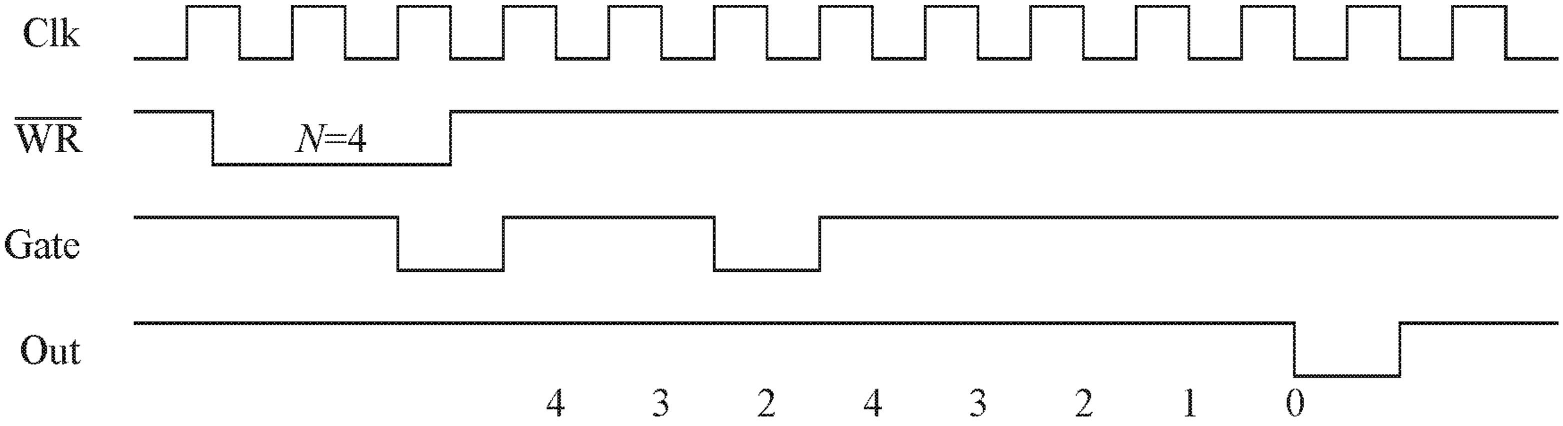
Timers/counters

- Intel 8253 modes
  - Mode 4: „software triggered strobe”
    - Gate=1: count starts after initial value is written
    - Gate=0: count stops
    - Gate 0→1: count reset



Timers/counters

- Intel 8253 modes
  - Mode 4: „hardware triggered strobe”
    - Gate=0→1: count starts
    - Gate=0: count continues
    - Gate 0→1: count reset



Timers/counters

- Intel 8253 – Gate operation summary

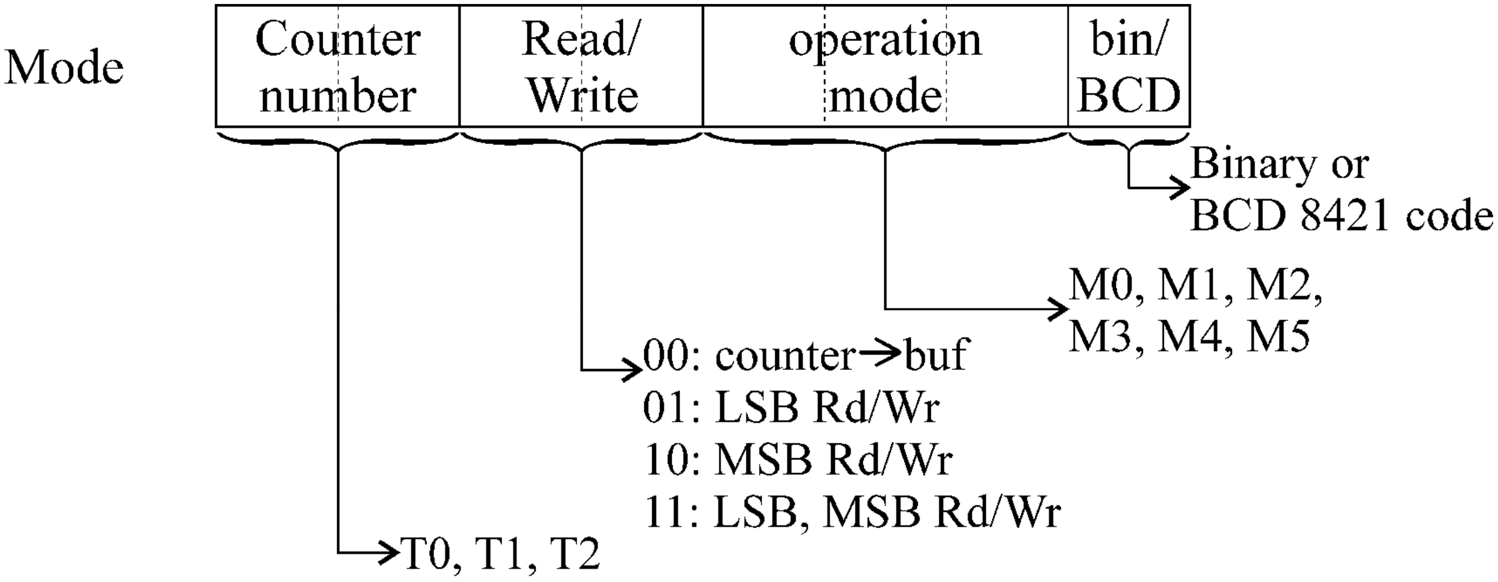
Mode	0, 1→0	0→1	1
0	Disable count		Enable count
1		Initate count Reset output	
2	Disable count Out=1	Reinitiate count	Enable count
3	Disable count Out=1	Reinitiate count	Enable count
4	Disable count		Enable count
5		Initiate count	

Timers/counters

- Intel 8253 programming

A_1A_0	00	01	10	11
Register	T0 data	T1 data	T2 data	Control

  - – Mode/control register



Mode

Counter number

Read/ Write

operation mode

bin/ BCD

Binary or BCD 8421 code

M0, M1, M2, M3, M4, M5

00: counter→buf
01: LSB Rd/Wr
10: MSB Rd/Wr
11: LSB, MSB Rd/Wr

T0, T1, T2

Timers/counters

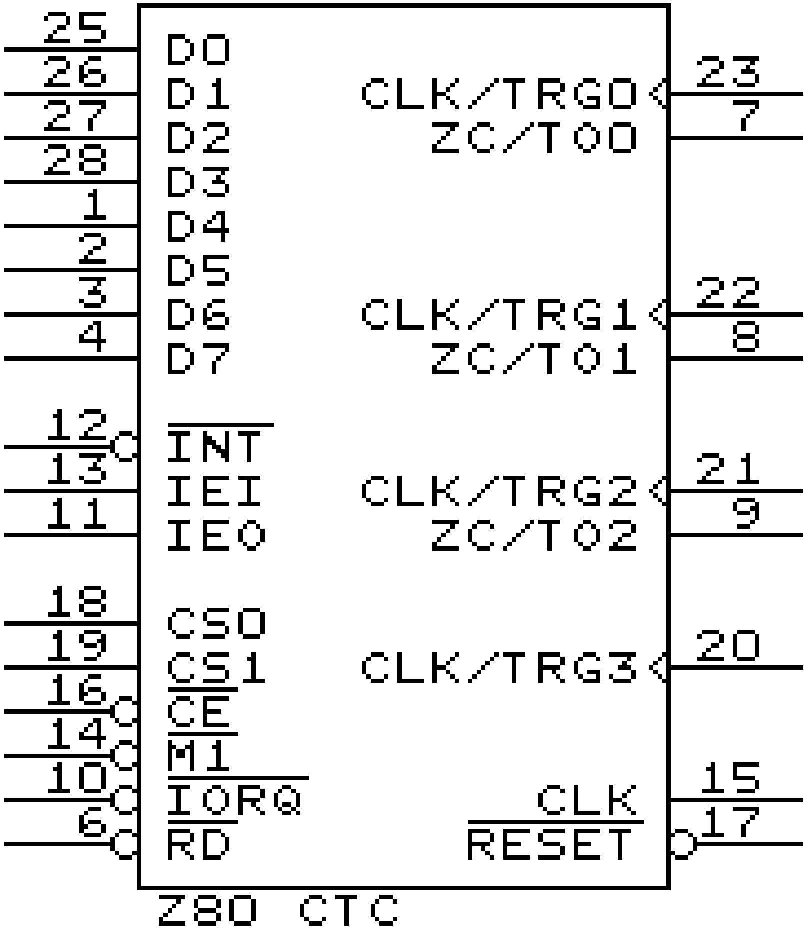
- Intel 8254 programming extensions
  - „Read-back” command
    - Read counter content
    - Read counter mode
    - Store counter content in a register
      - Counters bit-map selectable
  - Status command
    - Out pin status
    - Counter can be read
    - Counter mode / code

Timers/counters

- Zilog Z80 CTC
  - – 4 independent, 8-bit counters
  - – Timer/counter operation
  - – Count from initial value to 0
    - Automatic hardware reload
  - – Counting start can be triggered
  - – Out signal (for 3 counters only)
  - – Interrupt generation
    - Can work as an interrupt controller for non-Z80 family circuits (e.g., 8255, 8253…..)

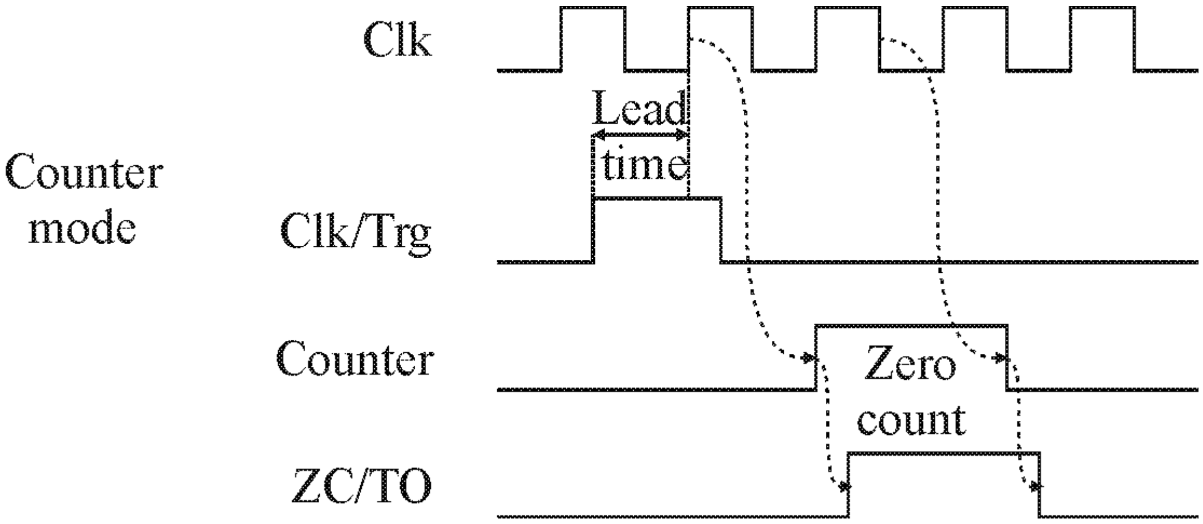
Timers/counters

- Zilog Z80 CTC circuit pins



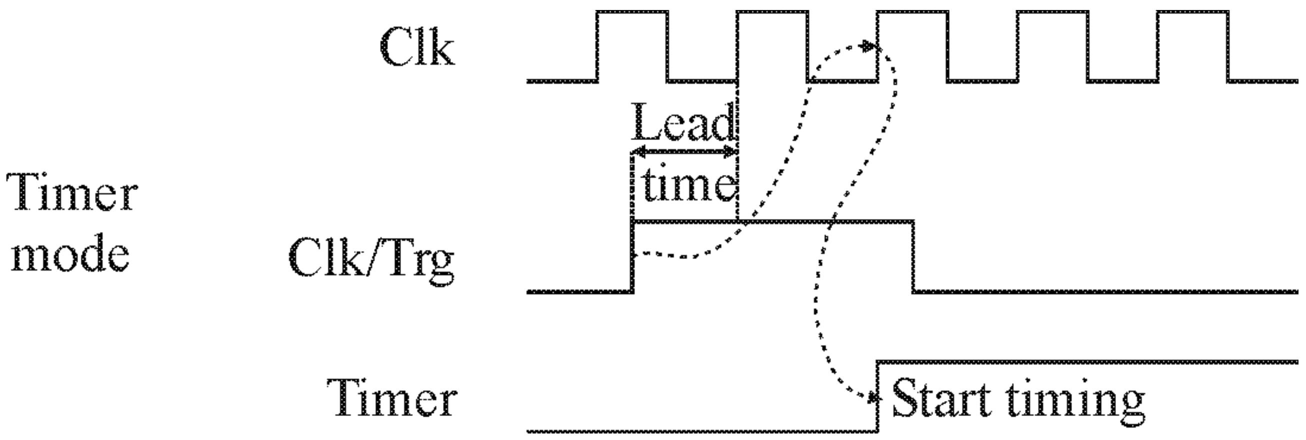
Timers/counters

- Zilog Z80 CTC modes
  - Counter mode
    - Clk/Trg = input (active value software selectable)
    - Counted to 0: Out pulse
    - Can generate interrupt



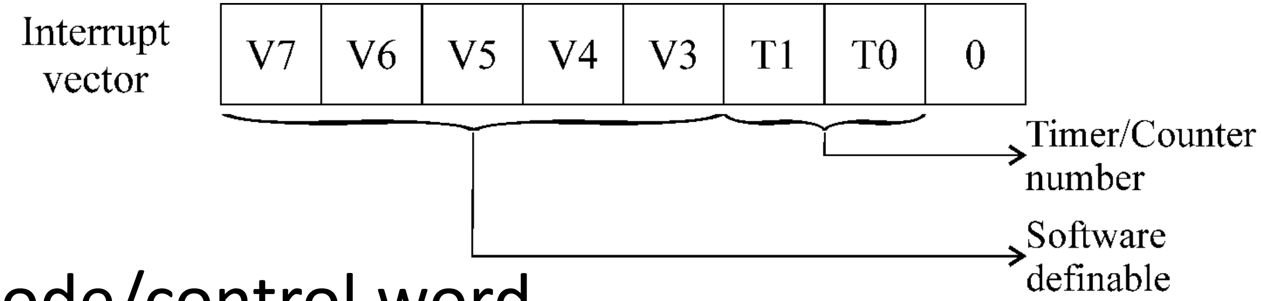
Timers/counters

- Zilog Z80 CTC modes
  - Timer mode
    - Clk/Trg = optional counting start
    - Counted to 0: Out pulses, *η*=½, T=T$_{clk}$ *[16|256]*Tc
    - Can generate interrupt



Timers/counters

- Zilog Z80 CTC programming
  - Interrupt vector
    - Common (software definable) part
    - Timer numer (automatically generated) part
    - One word for all counters

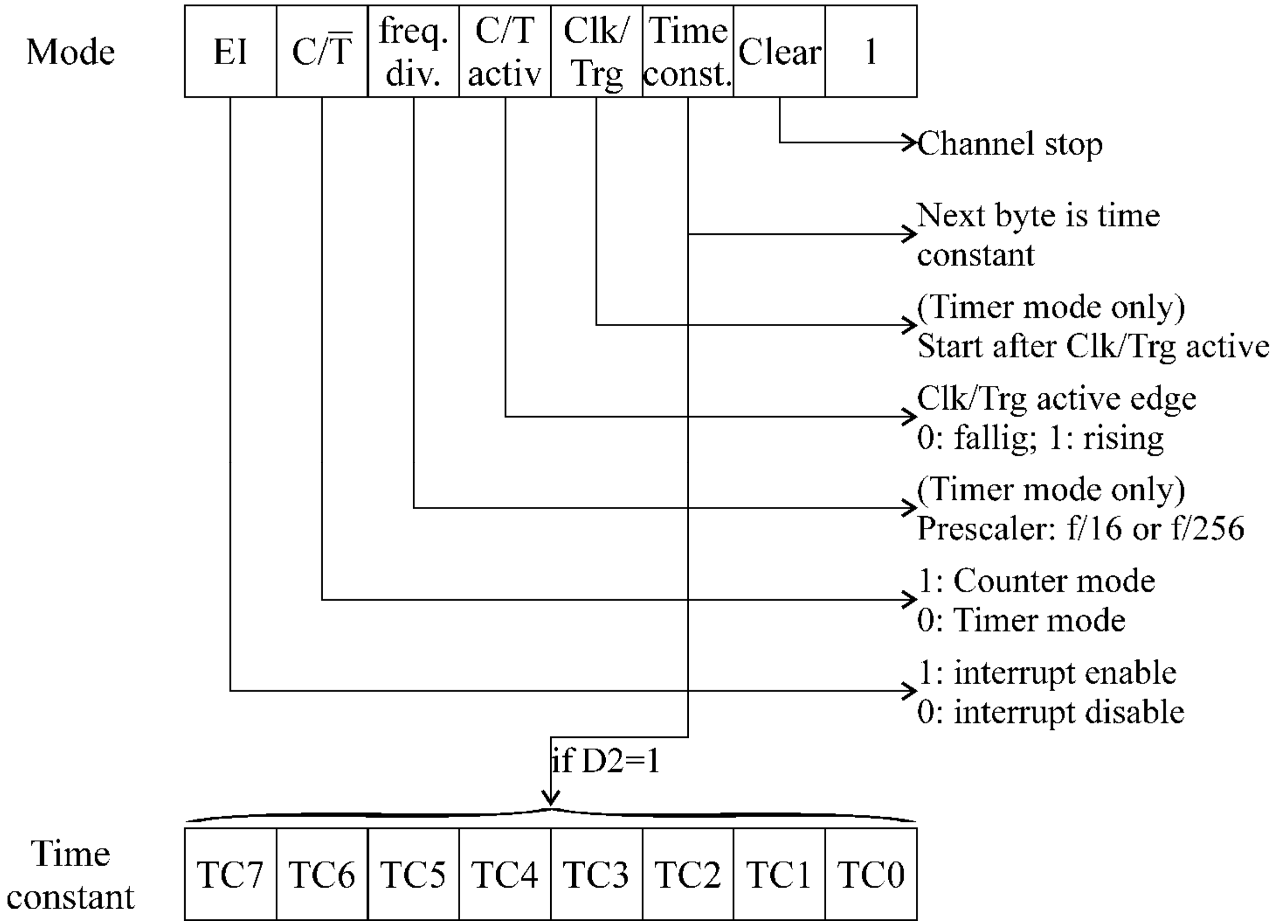


Interrupt vector	V7	V6	V5	V4	V3	T1	T0	0

  - Mode/control word
    - For each timer separately
    - Time constant must be announced
    - Timer read any time

Timers/counters

- Zilog Z80 CTC programming
  - Mode/control



Mode	EI	C/$\overline{T}$	freq. div.	C/T activ	Clk/ Trg	Time const.	Clear	1

Channel stop

Next byte is time constant

(Timer mode only)
Start after Clk/Trg active

Clk/Trg active edge
0: fallig; 1: rising

(Timer mode only)
Prescaler: f/16 or f/256

1: Counter mode
0: Timer mode

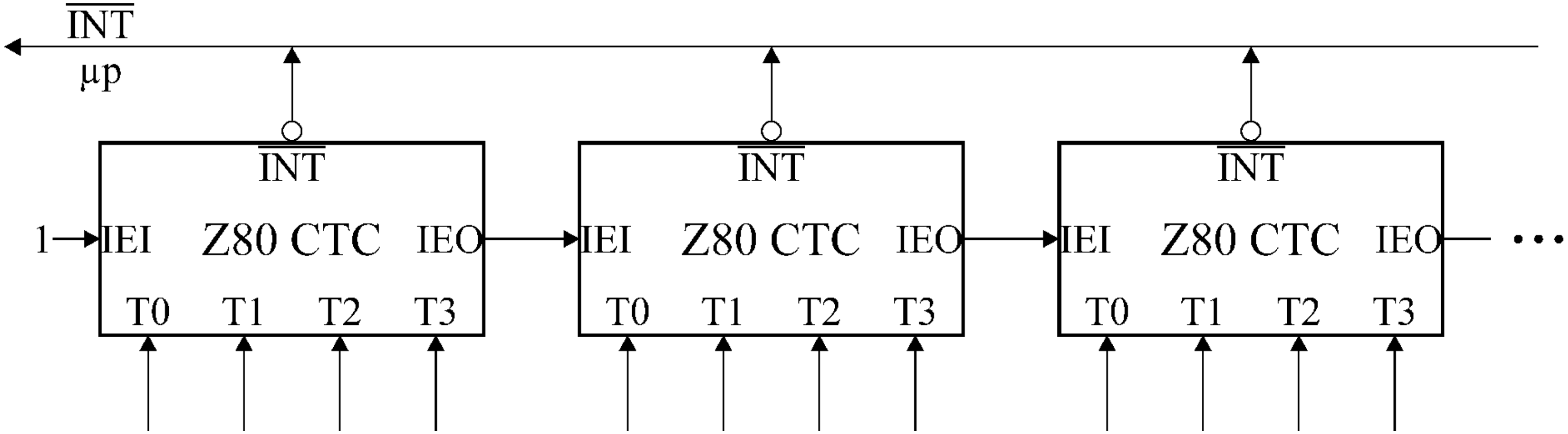
1: interrupt enable
0: interrupt disable

if D2=1

Time constant	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0

Timers/counters

- Zilog Z80 CTC interrupts
  - T0 – highest priority, T3 – lowest priority
  - Individual vectors for each counter
  - May work as an interrupt controller for non-Z80 family IC’s
  - „distributed interrupt controller” concept



Timers/counters

- Zilog Z80 CTC interrupts
  - For „external” interrupt inputs
    - Counter mode
    - Time constant = 1
    - Hardware time constant reload
    - Programmable active interrupt signal edge
    - Software masking
  - For other counters/timers
    - Anything we need

Timers/counters

- Zilog Z80 CTC reset
  - Count operations terminate
  - All interrupts disable
  - ZC/TO and INT lines inactive
  - IEO=IEI
  - Data lines – high impedance