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Microprocessor and Embedded Systems

Faculty of Automatic Control, Electronics and Computer Science, Informatics, Bachelor Degree

Lecture 5

Parallel input/output circuits

Bartłomiej Zieliński, PhD, DSc

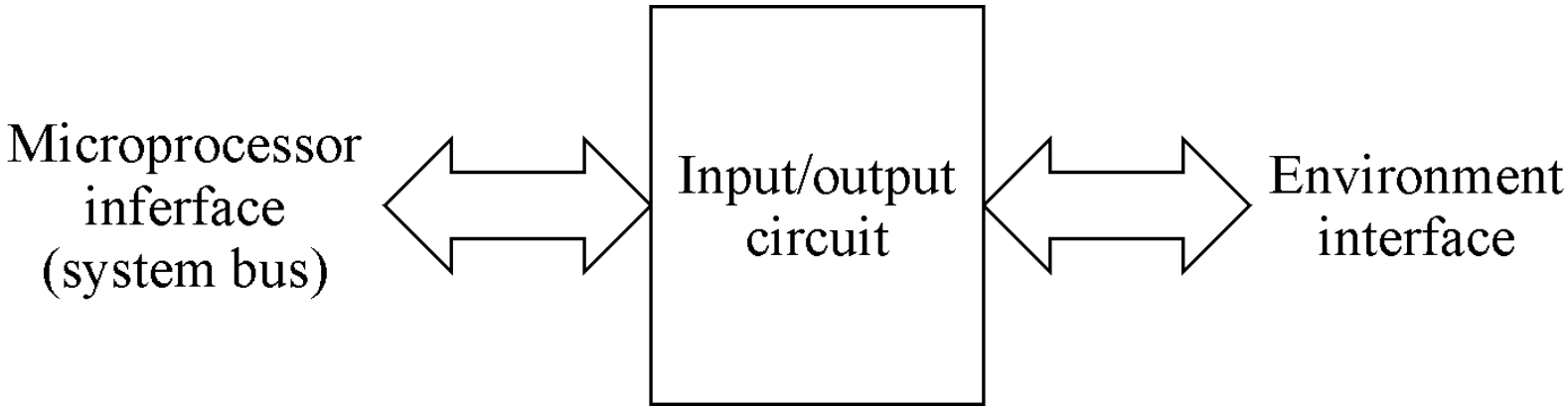
Parallel IO circuits

Program:

- General IO circuit properties
- Simple paralel IO with acknowledge
  - 8212 circuit
  - Register + flip-flop
- Programmable paralel IO circuits
  - Intel 8255
  - Zilog Z80 PIO

Parallel IO circuits

- General concept & properties



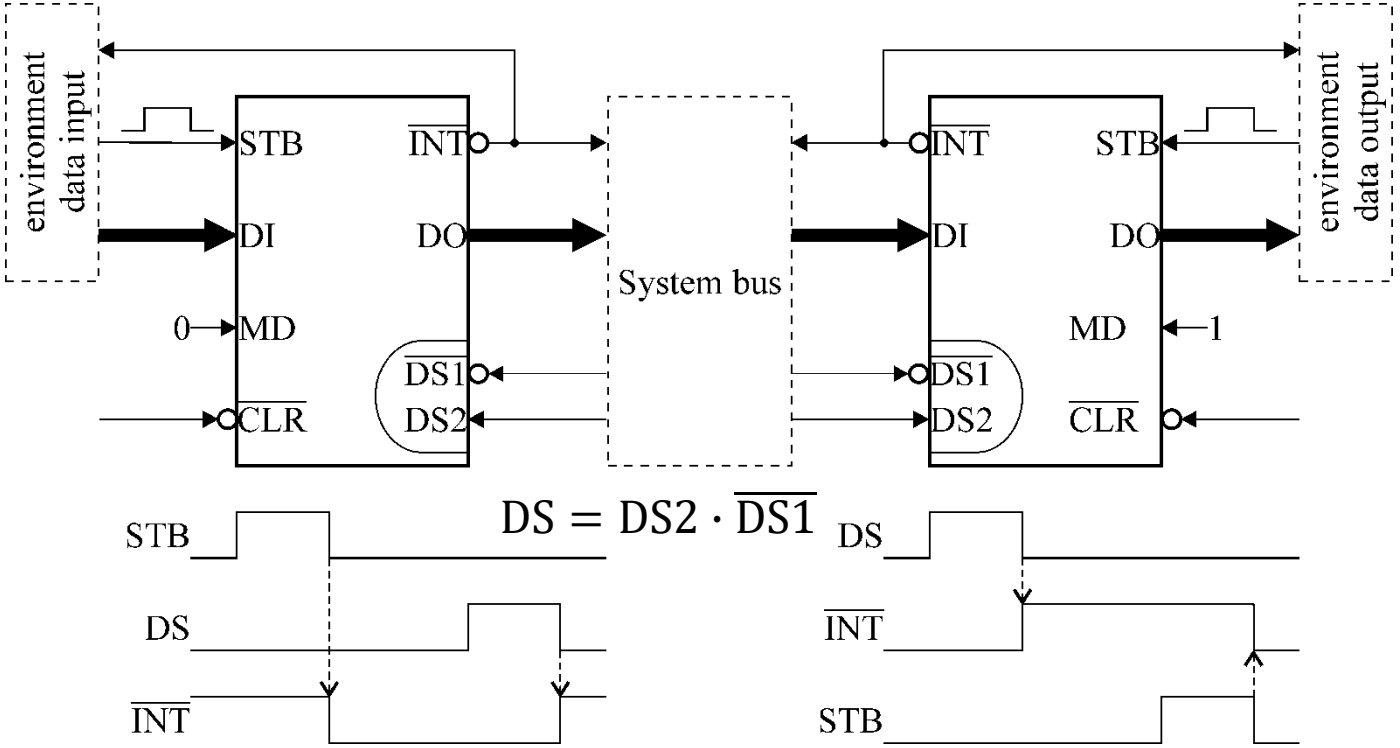
  - Microprocessor interface
    - Simple – works with every µp
    - Dedicated (optimised) – highly µp-dependent
  - Environment interface
    - Highly function-dependent
    - Similar or compatible across various circuits

Parallel IO circuits

- 8212 circuit
  - 8-bit universal I/O register with status signals

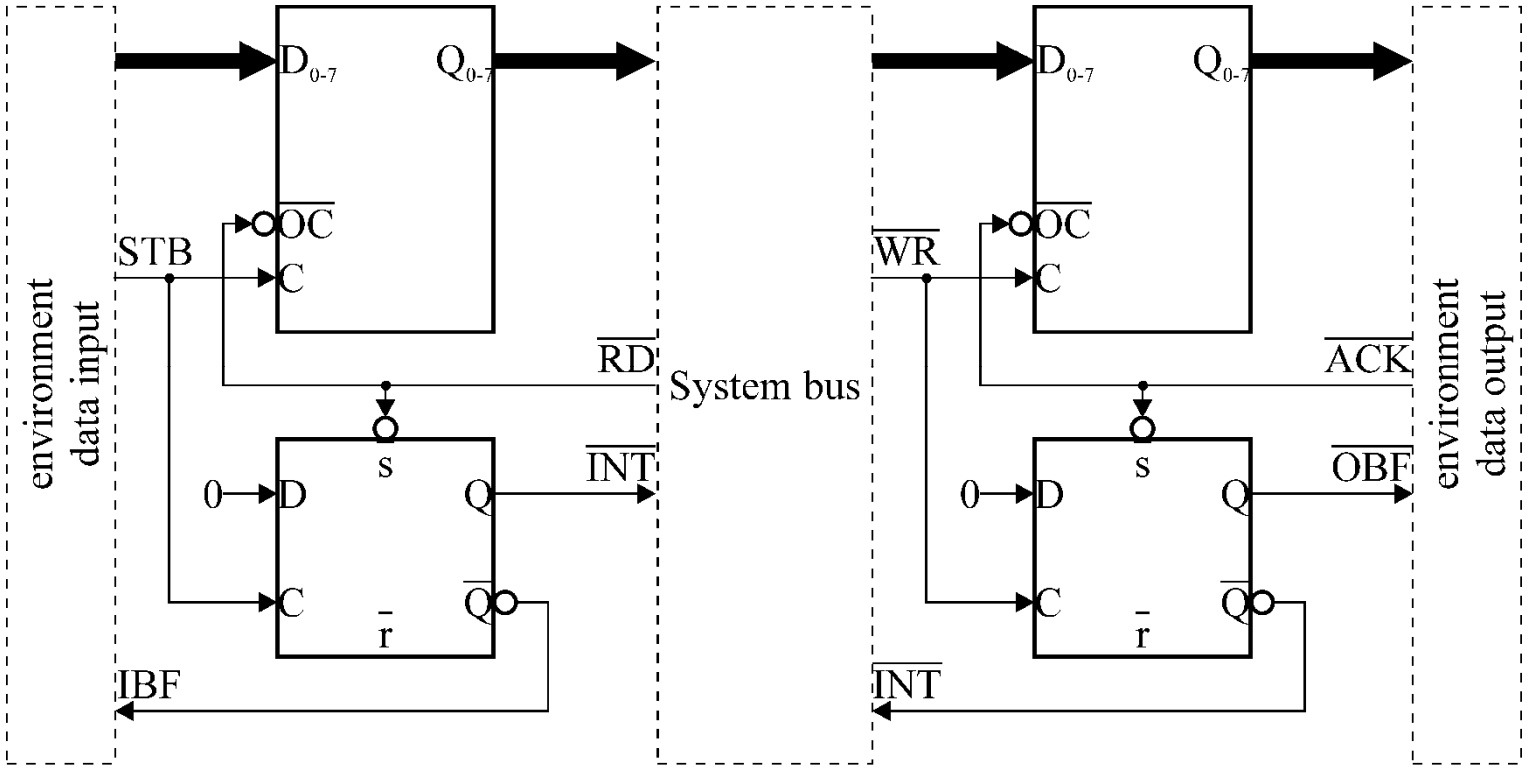
- Parallel input with data ready signal
- DO – three-state

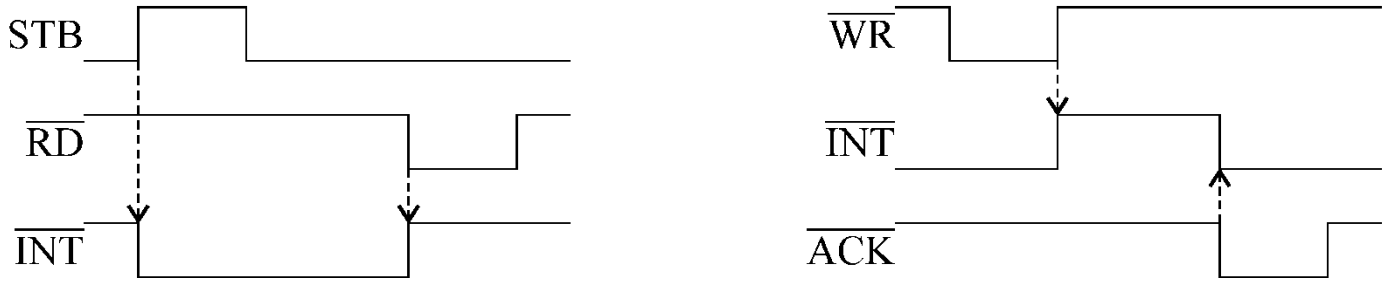
- Parallel output with data request signal
- DO – two-state



Parallel IO circuits

- Register + flip-flop



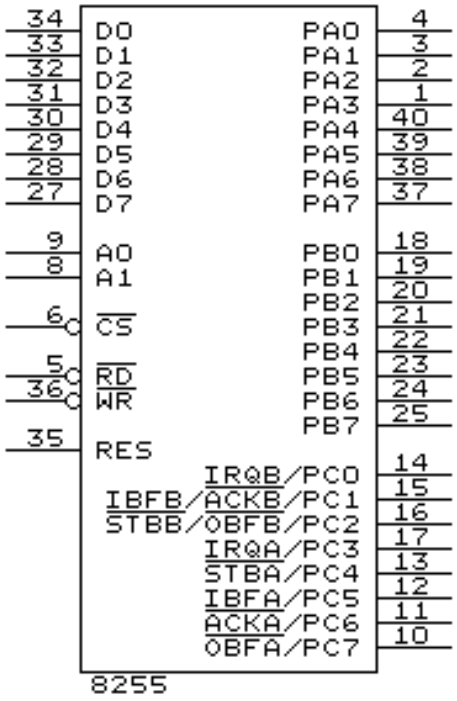


Parallel IO circuits

- Intel 8255 circuit
  - Programmable parallel I/O circuit
  - 3 bi-directional, 8-bit I/O ports
    - Port A – bi-directional
    - Port B – input or output
    - Port C – input or output, control signals for A and B
  - 3 modes
    - Input or output without acknowledge (A, B, CL, CH)
    - Input or output with acknowledge (A, B)
    - Bi-directional with acknowledge (A)

Parallel IO circuits

- 8255 pins

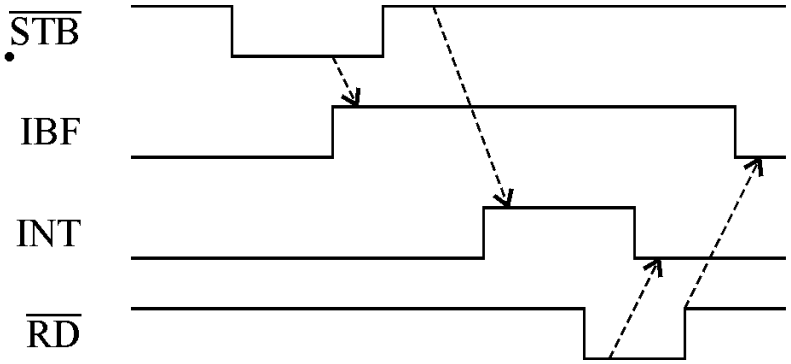


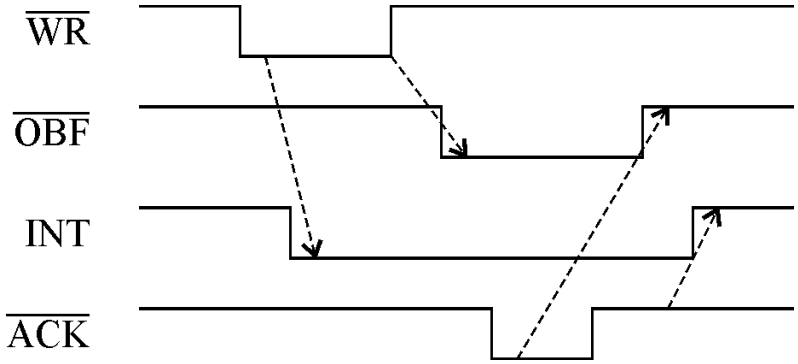
Parallel IO circuits

- 8255 port modes
  - Mode 0
    - No acknowledge
    - Transmission direction set for PA, PB, PCL, PCH
    - Output data stored in a register
    - Input data NOT stored, read directly from the pins
  - Mode 1
    - Acknowledge („hand shake”)
    - Transmission direction set for PA, PB
    - PC – control signals for PA and PB
    - Output data stored in a register
    - Input data also stored in a register

Parallel IO circuits

- 8255 port modes
  - Mode 1 (cont'd)





  - Mode 2
    - Similar to Mode 1
    - Works only for PA
    - Control signals as in Mode 1
    - Input and output data stored in two separate registers

Parallel IO circuits

- 8255 port modes – interrupts
  - Mode 0
    - No built-in interrupt mechanism
    - External circuit can be used
  - Mode 1 interrupts
    - Hardware signal (INT)
    - Software read of PC (polling)
  - Mode 2 interrupts
    - As in Mode 1
    - Common INT line for both directions
  - Requested, when INTE=1
    - Modify INTE → set/reset PC_3 ($INTE_A$) or PC_0 ($INTE_B$)

Parallel IO circuits

- 8255 registers

A_1A_0	00	01	10	11
Register	PA	PB	PC	Control

  - Control register
    - Mode

Bit	Function
7	1
6-5	PA mode
4	PA direction
3	PCH direction
2	PB mode
1	PB direction
0	PCL direction

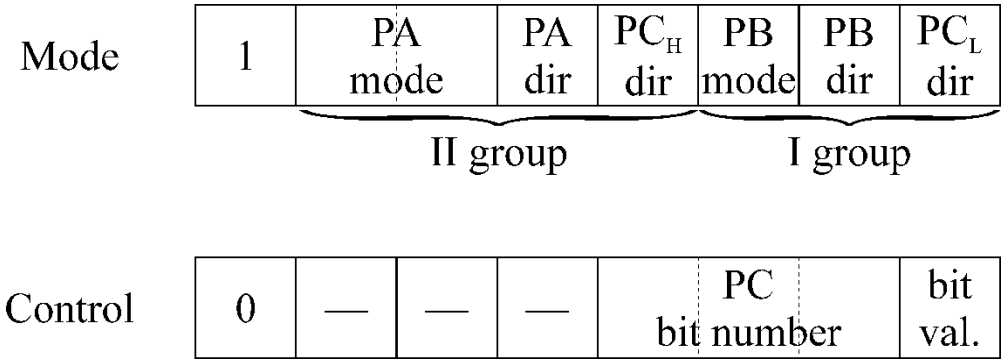
PC control

Bit	Function
7	0
6-4	-
3-1	PC bit numer
0	PC bit value

$$PC_{R_{1..3}} = R_0$$

Parallel IO circuits

- 8255 control register
  - (write only)



  - Direction bits:
    - 1=1nput
    - 0=0utput

Parallel IO circuits

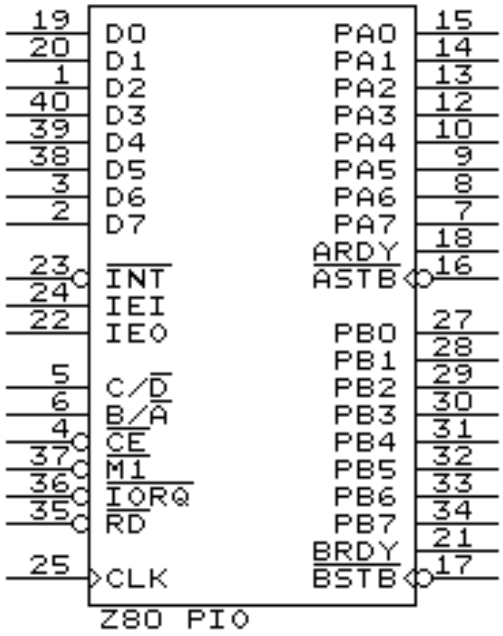
- 8255 reset
  - All ports set as Mode 0, input
    - To avoid outputs conflicts
  - Port lines in high-impedance state

Parallel IO circuits

- Zilog Z80 PIO circuit
  - Programmable parallel I/O circuit
  - 2 bi-directional, 8-bit I/O ports
    - Port A – bi-directional
    - Port B – input or output
  - 4 modes
    - Input with acknowledge (PA, PB)
    - Output with acknowledge (PA, PB)
    - Bi-directional with acknowledge (PA only)
      - PB limited to bit mode
    - Bit (PA, PB)

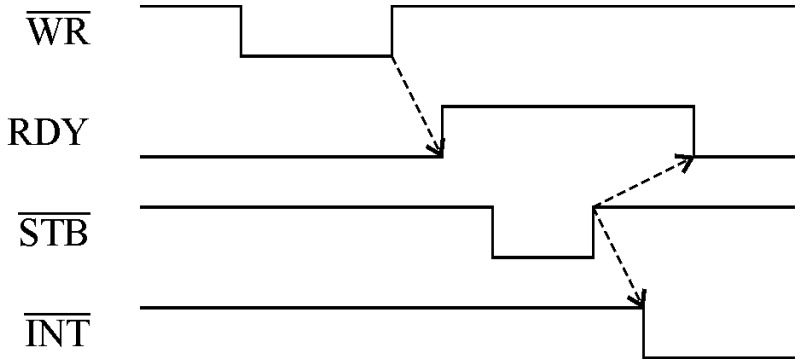
Parallel IO circuits

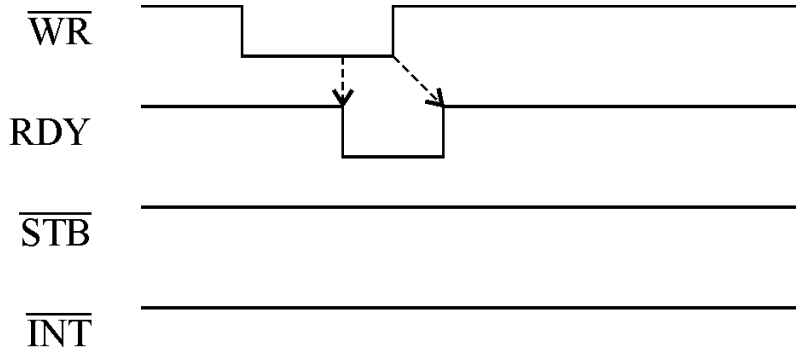
- Z80 PIO pins



Parallel IO circuits

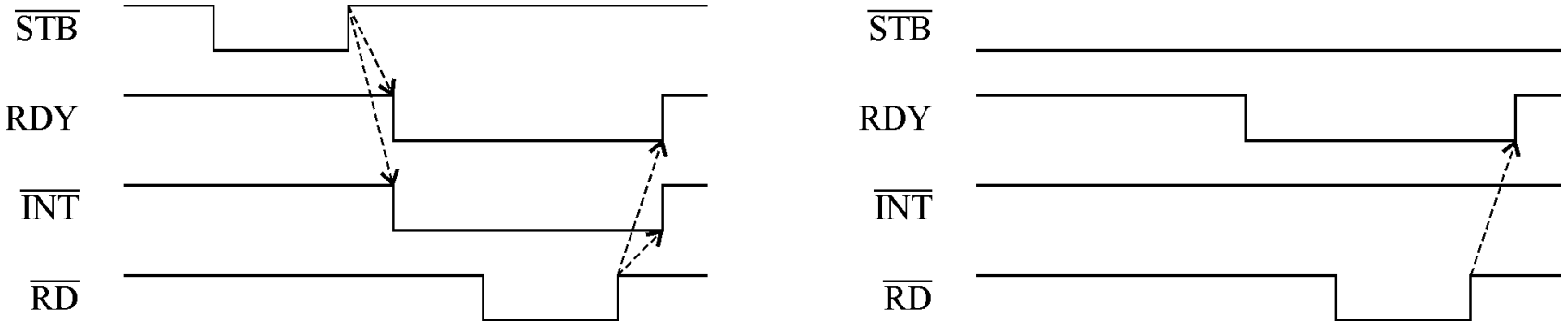
- Z80 PIO port modes
  - Mode 0
    - Output with optional acknowledge
    - Works with PA and PB independently
    - Output data stored in a register
    - After data write, RDY 0→1





Parallel IO circuits

- Z80 PIO port modes
  - Mode 1
    - Input with optional acknowledge
    - Works with PA and PB independently
    - Input data may be stored in a register
    - After data read, RDY 0→1



Parallel IO circuits

- Z80 PIO port modes
  - Mode 2
    - Bi-directional with acknowledge
    - Works with PA only (PB only in bit mode)
    - Data stored in separate registers
    - After data read/write, RDY 0→1
    - ARDY/ASTB – output, BRDY/BSTB – input

Parallel IO circuits

- Z80 PIO port modes
  - Mode 3
    - Bit mode
    - Works with PA or PB independently
    - Each bit set as I or O
    - RDY=0
    - Automatic control function
      - Selected bits
      - Selected function (OR, AND)
      - Selected value (0, 1)
      - When fulfilled → interrupt

Parallel IO circuits

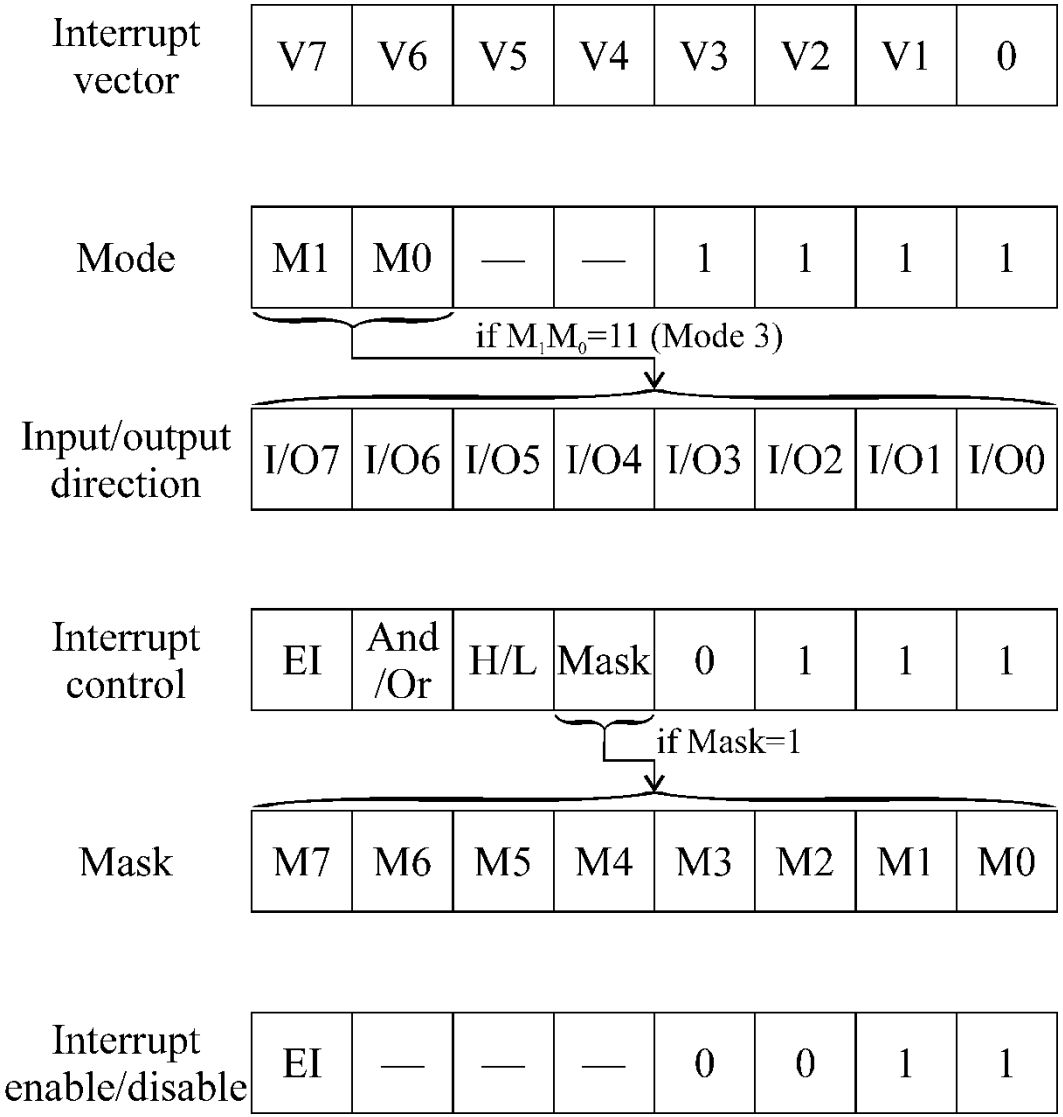
- Z80 PIO programming
  - Registers (for each port separately)
    - Data input (8-b)
    - Data output (8-b)
    - Mode (2-b)
    - Mask (8-b)
    - I/O direction (8-b)
    - Interrupt vector (8-b)
    - Mask control (2-b)

Parallel IO circuits

- Z80 PIO programming
  - Interrupt vector (D_0=0, D_{1-7}=vector)
  - Mode (D_{0-3}=1, D_{6-7}=mode)
    - If mode=3, next byte sets I/O direction (1=out, 0-in)
  - Interrupt control (D_{0-2}=1, D_3=0, D_7=1/0 enable/disable)
    - If mode=3, D_6=AND/OR, D_5=1/0, D_4=mask on/off
    - If D_4 was 1, next byte is mask
  - Interrupt enable/disable (D_{0-1}=1, D_{2-3}=0, D_7=1/0 enable/disable)

Parallel IO circuits

- Z80 PIO programming

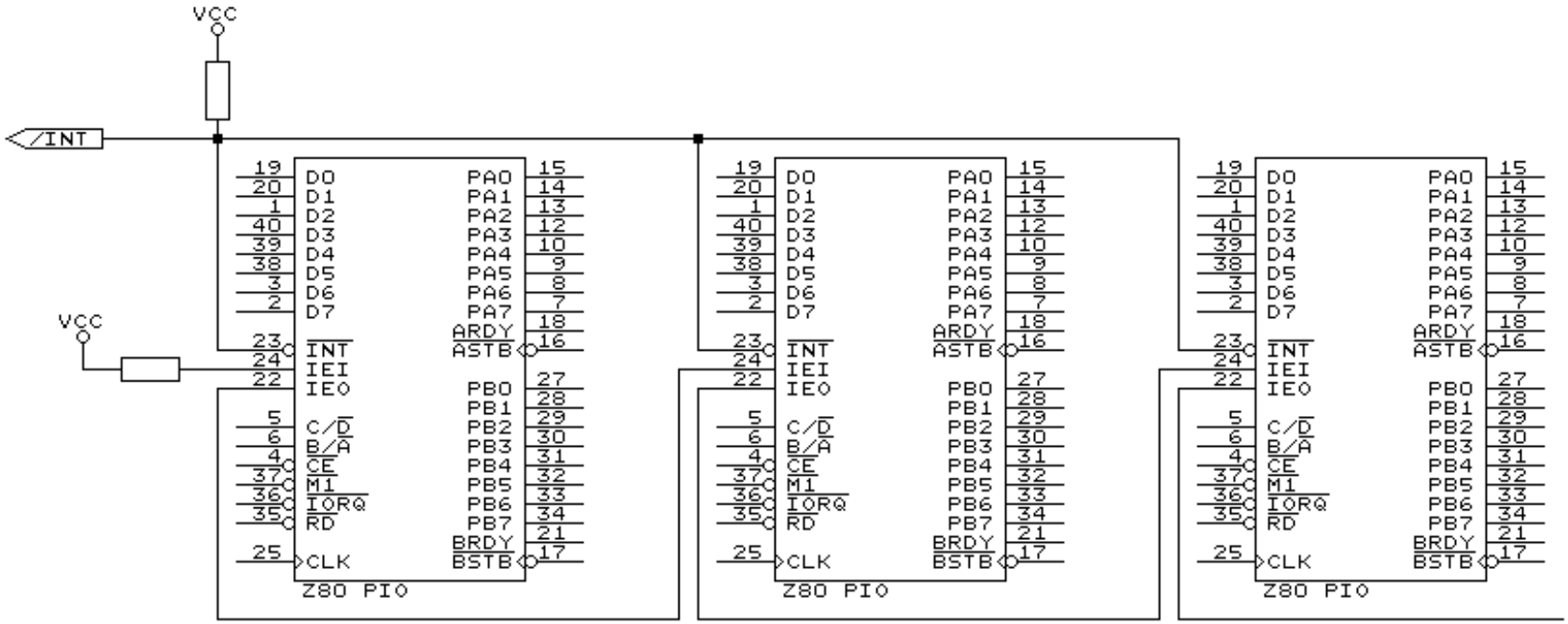


Parallel IO circuits

- Z80 PIO interrupts
  - PA – higher priority
  - Mode 0, 1, 2 – requested when $\overline{\mathrm{STB}}$=0→1
  - Mode 3 – requested when programmed conditions are fulfilled
  - Interrupt accepted → interrupt vector sent to µp
  - RETI command decoding

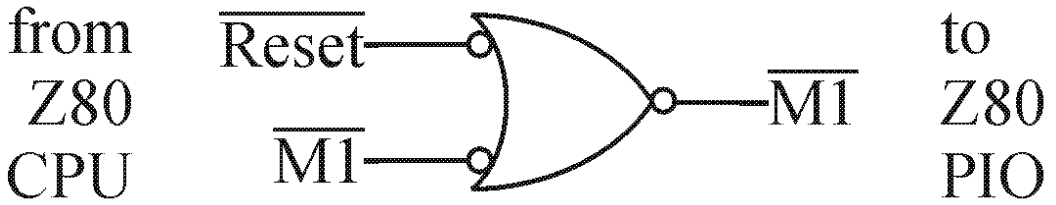
Parallel IO circuits

- Z80 PIO interrupts
  - IEI, IEO, INT lines
  - „daisy-chain” priority



Parallel IO circuits

- Z80 PIO reset
  - All ports set as Mode 1, input
    - To avoid outputs conflicts
  - PA, PB high impedance
  - ARDY=BRDY=0 (inactive)
  - Interrupts disable
  - PA and PB output registers=0
  - Mask registers=0
  - No Reset input (!)



Parallel IO circuits

- More information about Z80 family

  http://z80.info/