Fundusze Europejskie
Wiedza Edukacja Rozwój

Rzeczpospolita Polska

Unia Europejska
Europejski Fundusz Społeczny

Politechnika Śląska jako Centrum Nowoczesnego Kształcenia
opartego o badania i innowacje

POWR.03.05.00-IP.08-00-PZ1/17

Projekt współfinansowany przez Unię Europejską ze środków Europejskiego Funduszu Społecznego

Microprocessor and Embedded Systems

Faculty of Automatic Control, Electronics and Computer Science, Informatics, Bachelor Degree

Lecture 4

8051 single-chip microcomputer
Part 2
Built-in peripherials

Bartłomiej Zieliński, PhD, DSc

8051 (2)

Program:

(last week)

- 8051 structure
- Memory organisation
- Pins and machine cycles

(today)

- Counter/timer circuit
- Serial port
- Interrupt controller

8051 (2)

- Timer/counter circuit
  - T0, T1
    - 4 modes
      - 13-bit with no hardware reload
      - 16-bit with no hardware reload
      - 8-bit with hardware reload
      - T0 acts as two independent counters/timers
    - T1 can clock a serial port
  - T2
    - 16-bit
      - Hardware reload
      - Hardware capture
    - Can clock a serial port

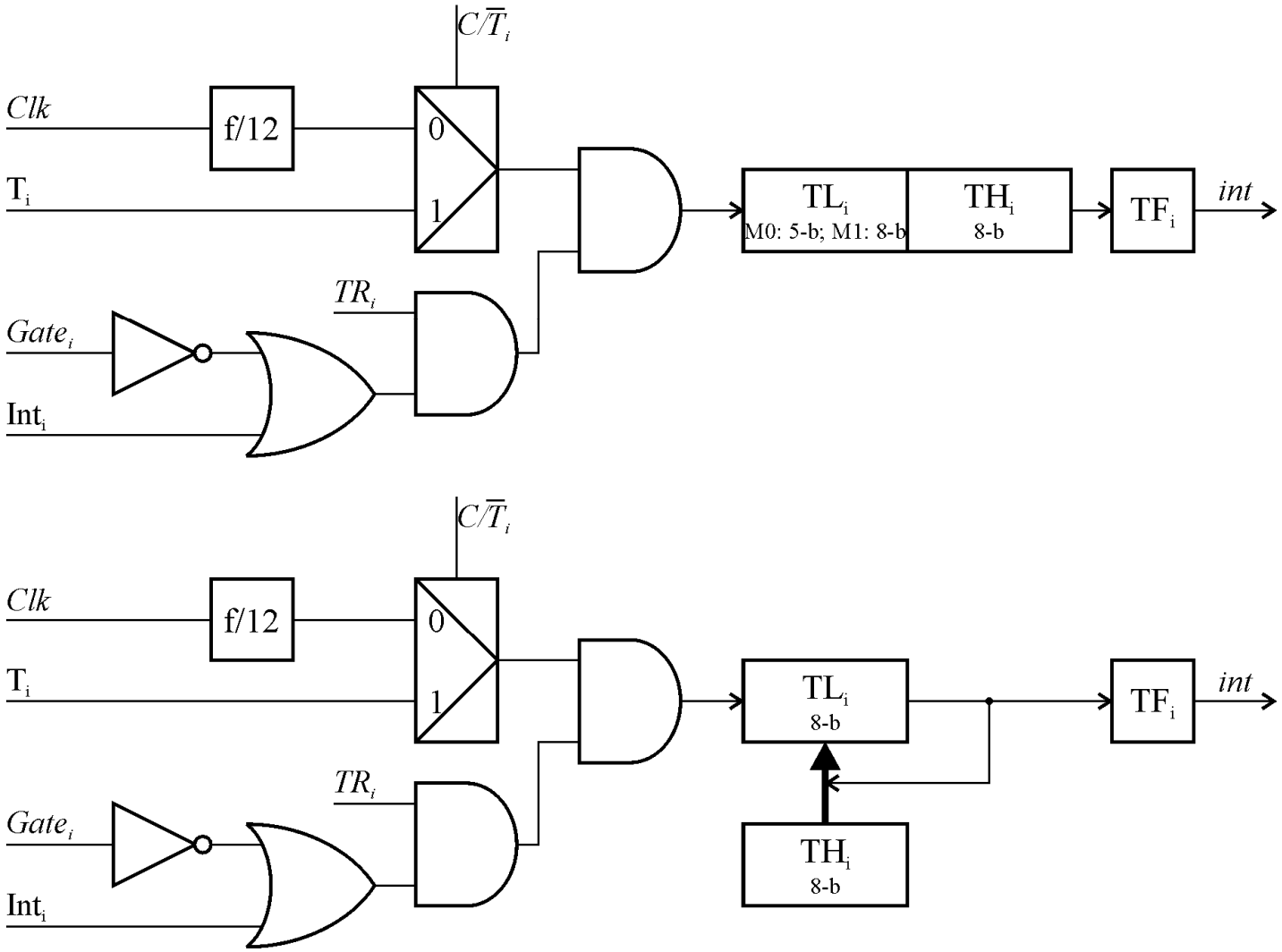
8051 (2)

- T0, T1 control
  - TMOD – mode register
    - Mode 0-3 (2 bits)
    - Counter/timer mode ($C/\overline{T}$)
    - Hardware gating (1 bit)

    } for each counter
  - TCON – control register
    - Timer run (TR) bits
    - Timer flag (TF) bits
    - *IE bits – for external interrupt control*
    - *IT bits – for external interrupt control*

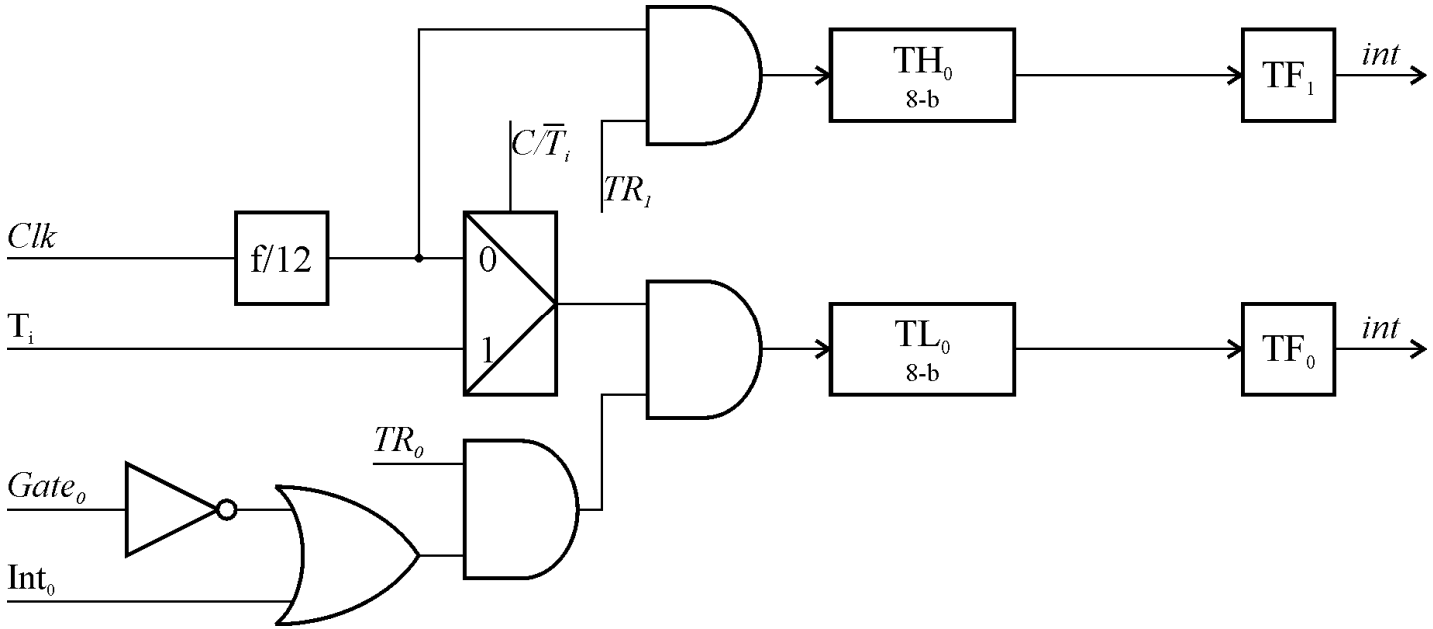
8051 (2)

- T0, T1 – modes 0, 1, 2



8051 (2)

- T0 – mode 3



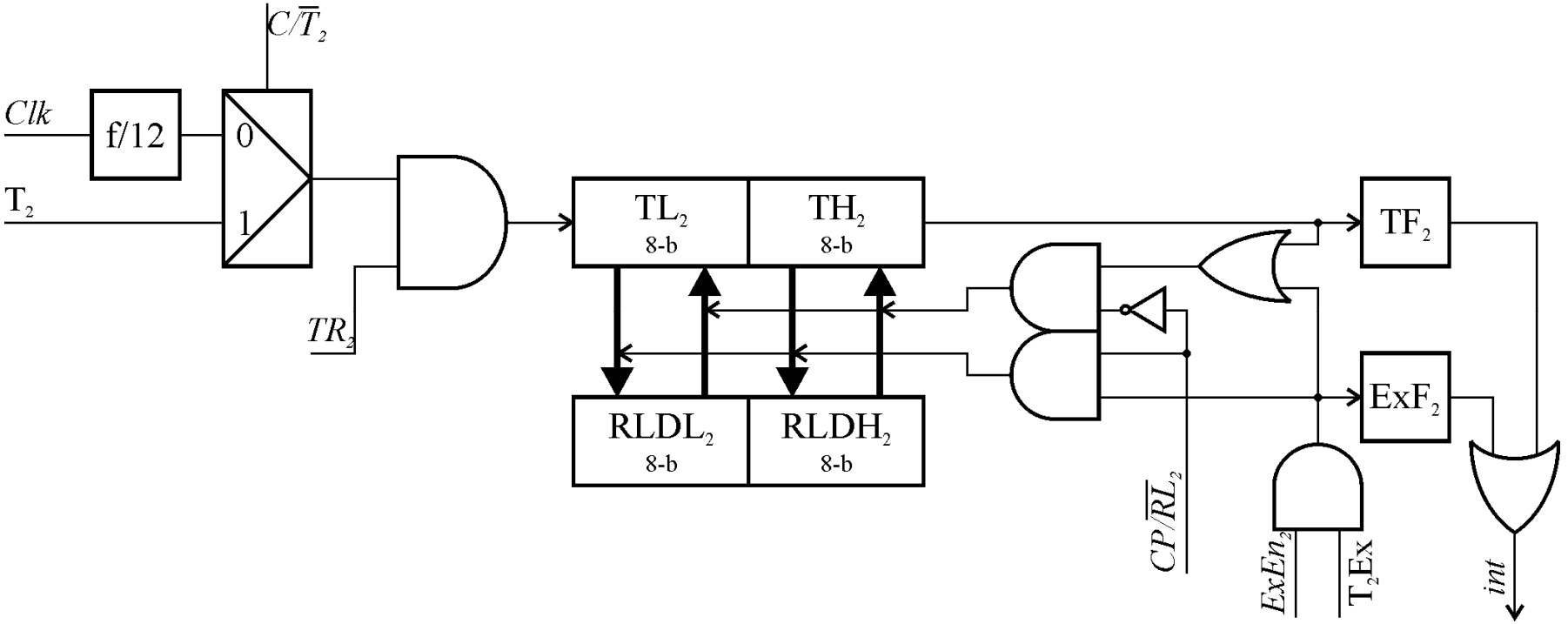
- T1
  - No interrupt
  - No software disable (TR)
  - Pulse source selectable ($C/\overline{T}_1$)

8051 (2)

- T2 control
  - T2CON register
    - Capture/reload function
    - Counter/timer mode (as in T0, T1)
    - TR - Timer run (as in T0, T1)
    - ExEn2 – external event input enable
    - Tclk – transmitter clock (serial port)
    - Rclk – receiver clock (serial port)
    - ExF2 – external event flag
    - TF2 – timer overflow flag (as in T0, T1)

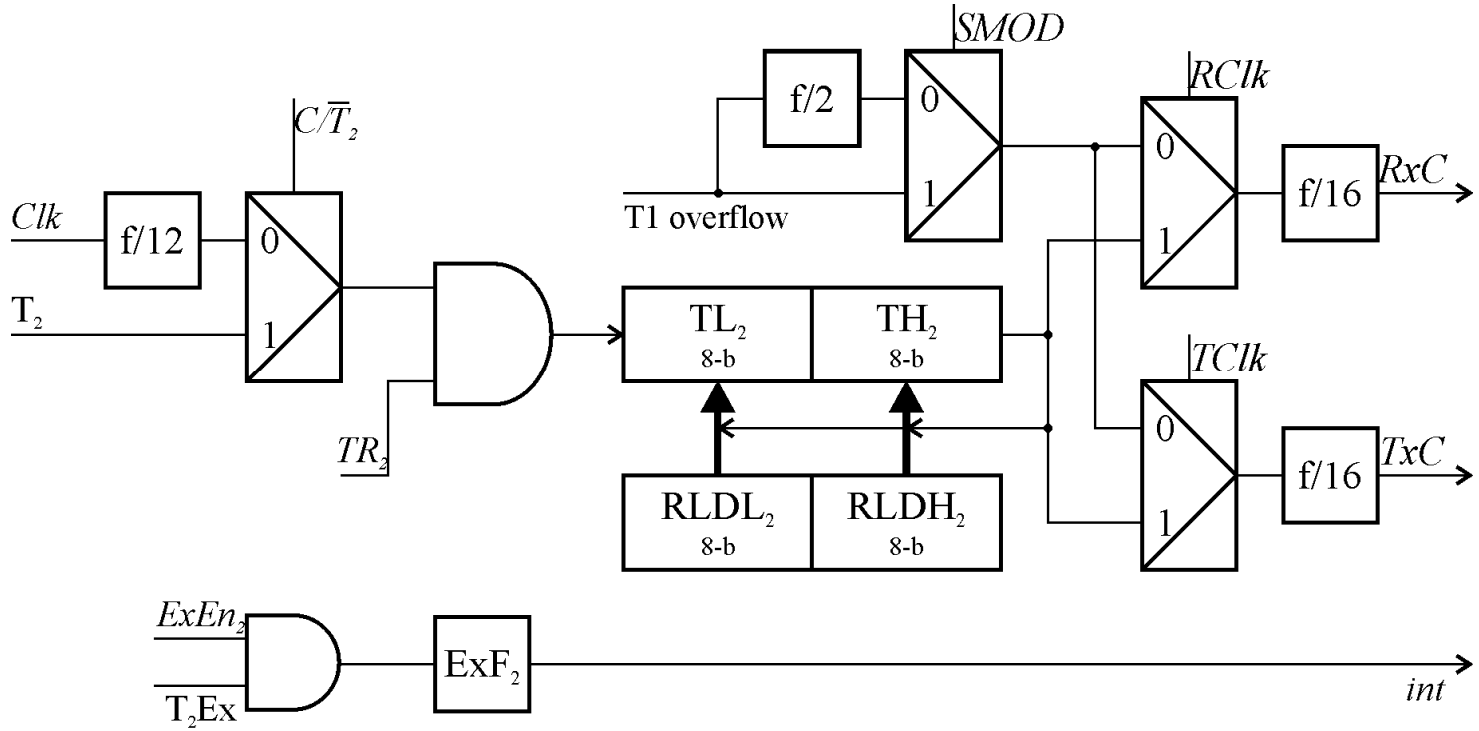
8051 (2)

- T2 structure



8051 (2)

- T2 as a clock source for the serial port



8051 (2)

- Serial port
  - SBUF data in/out register
  - SCON mode/control register
    - SM0, SM1 – mode
    - SM2 – special masking mode
    - REN – receiver enable
    - TB8 – transmit bit 8
    - RB8 – receive bit 8
    - TI – transmitter ready (interrupt flag)
    - RI – receiver ready (interrupt flag)

8051 (2)

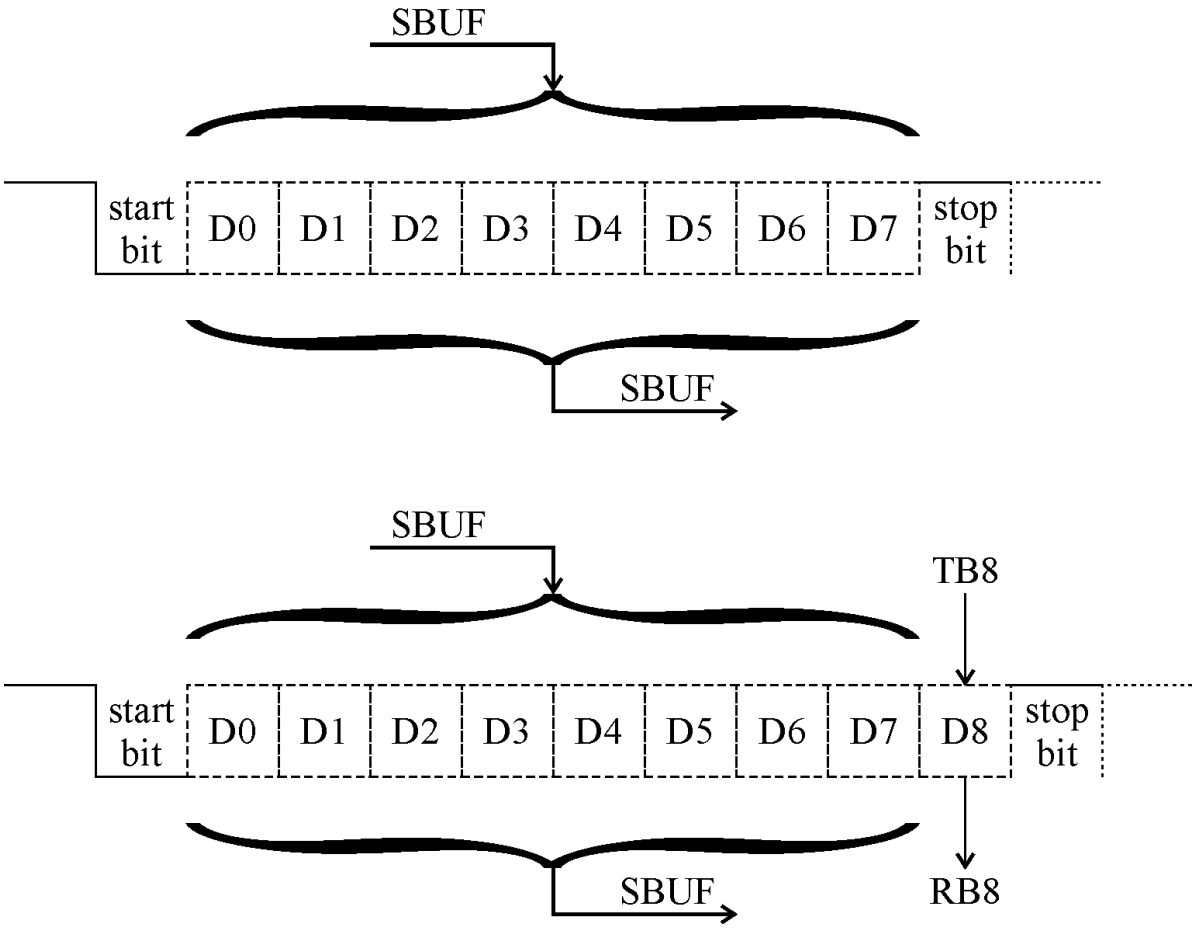
- Serial port modes

Mode	Transmission type	Bits	Transmission rate
0	Synchronous	8	Constant: 1/12 f_{xtal}
1	Asynchronous	8	Programmable (T1 or T2 counter)
2	Asynchronous	9	Constant: 1/32 or 1/64 f_{xtal} (SMOD)
3	Asynchronous	9	Programmable (T1 or T2 counter)

  - Mode 0
    - RxD – bidirectional data
    - TxD – clock output
    - For e.g. shift register

8051 (2)

- Serial port – modes 1, 2, 3
  - asynchronous transmission



8051 (2)

- Serial port – modes 1, 2, 3
  - Serial port clock
    - Modes 1, 3: overflow of T1 or T2 optionally divided by 2 (SMOD=0)
    - Mode 2: ½ f_{xtal} optionally divided by 2 (SMOD=0)
  - Transmission rate = clock/16
    - T1 counter in M2 timer mode

$$R = \frac{f_{xtal}}{(2 - SMOD) * 12 * 16 * (256 - TH1)}$$

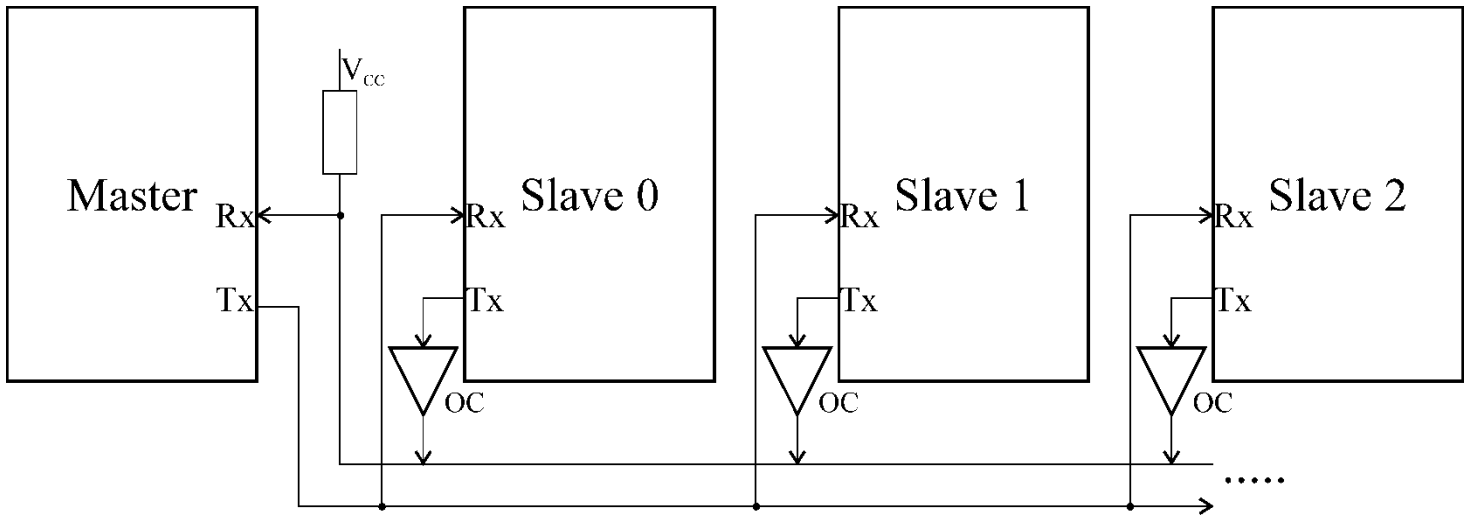
    - T2 counter

$$R = \frac{f_{xtal}}{2 * 16 * (65536 - RLD)}$$

5.75÷375000 bps

8051 (2)

- Serial port – special masking mode



– Mode 2, 3
  - SM2=1:
    – D8=0 ignored
    – D8=1 accepted

- Slaves: SM2=1
- Master: address (D8=1)
- Selected slave(s): SM2=0
- Master: data (D8=0)
- Selected slave(s): SM2=1

8051 (2)

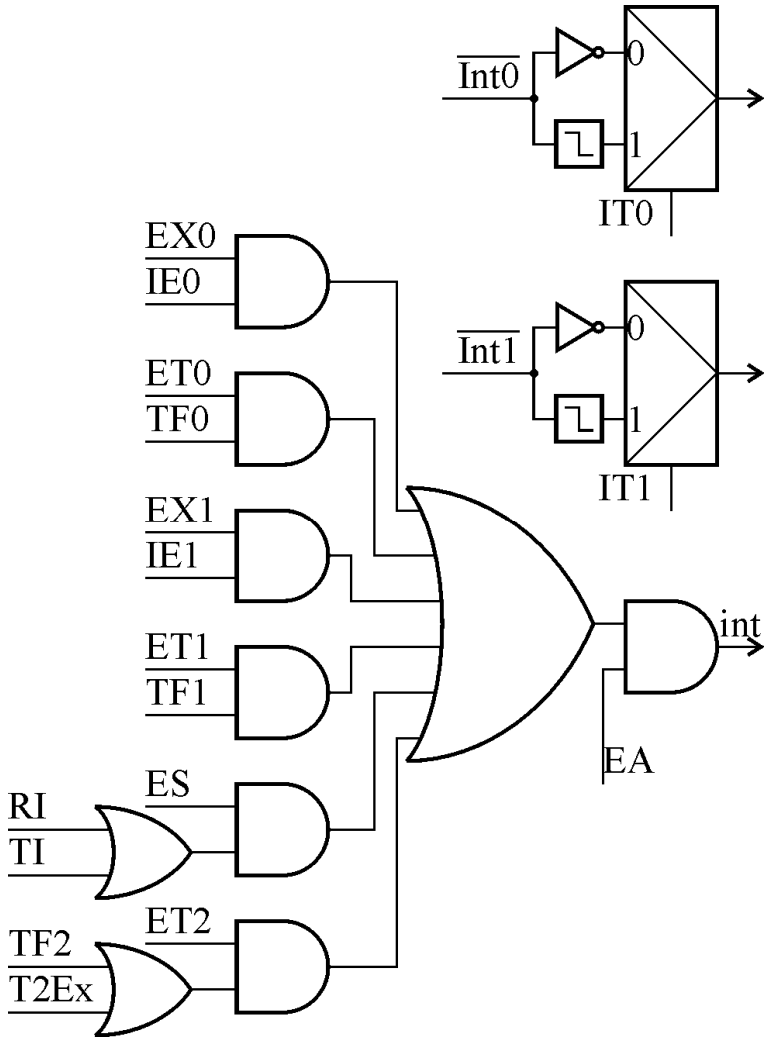
- Interrupt controller
  - Sources
    - External
      - INT0, INT1 – IE0, IE1 flags (TCON)
    - Internal timers/counters
      - T0, T1 overflow – TF0, TF1 flags (TCON)
      - T2 overflow, T2 external event – TF2, ExF2 (T2CON)
    - Internal serial port
      - Transmitter or receiver ready – TI, RI flags (SCON)
  - Flags set automatically, and:
    - One flag per interrupt
      - flag hardware cleared upon interrupt procedure start
    - More flags per interrupt
      - flag must be software cleared in the interrupt procedure
    - Flags can be software set
      - „*manually requested interrupt*”

8051 (2)

- Interrupt controller
  - IE (interrupt enable) register
    - Each interrupt individually masked
    - Global interrupt masking
  - IP (interrupt priority) register
    - Each interrupt individually set as:
      - Interruptable (multi-level interrupt system)
      - Non-interruptable (single-level interrupt system)
  - Part of TCON register
    - IE0, IE1 – external interrupt flag
    - IT0, IT1 – external interrupt level/edge triggered

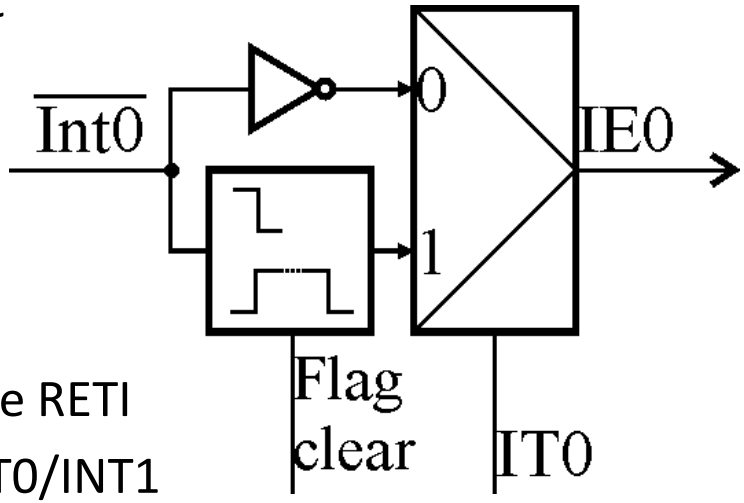
8051 (2)

- Interrupt controller
  - Interrupt not accepted:
    - Not the last machine cycle of the command
    - Command operates on IE, IP or is RETI
    - higher priority interrrupt is being served
  - Interrupt acceptance:
    - Internal priority registers set
    - Flags cleared
    - PC →stack (PSW not)
    - PC = address



8051 (2)

- Interrupt controller
  - External interrupts
    - Edge triggered
      - Edge detected → IE0/IE1 flags set
      - Procedure started → flags reset
      - Flags can be software set
    - Level triggered
      - Low state until procedur starts
      - Low state should disappear before RETI
      - IE0/IE1 flags = complemented INT0/INT1 inputs
      - Flags can't be software set
      - Software set the apropriate P3 bit to manually request an external interrupt



8051 (2)

- Low power modes
  - HMOS
    - Power off, RST/VPD=5V, 10÷15% of power
    - Power on, reset
  - CMOS – software switched
    - Idle (1/8 of power)
      - CPU stops
      - Peripherials operating
      - Exit → interrupt or reser
    - Power down (1/500 of power)
      - Only idata powered
      - V_{DD} >= 2 V
      - Exit → reset 10 ms

8051 (2)

- System extension
  - „classical” – system bus
    - External program memory
    - External data memory
    - Additional I/O circuits
    - Additional external interrupts
  - More equipped versions
    - More IO ports
    - More registers (i.e., additional DPTR)
    - More (and more sophisticated) IO interfaces
      - SPI, I^2C, PWM, ADC, DAC, EEPROM…..