Microprocessor and Embedded Systems

Faculty of Automatic Control, Electronics and Computer Science, Informatics, Bachelor Degree

Lecture 3

8051 single-chip microcomputer
Part 1
General architecture

Bartłomiej Zieliński, PhD, DSc

8051 (1)

Program:

(today)

- Genesis of single-chip μc

- 8051 structure

- Memory organisation

- Pins and machine cycles

- Ports structure

(next week)

- Built-in peripherials

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- ## Single-chip μc
  - ### Optimised for control
    - More logical commands
    - Less arithmetical command
    - More I/O capabilities
  - ### First circuits
    - Texas Instruments – TMS1802NC (1971)
    - Texas Instruments – TMS1000 (1974)
      - 1Kx8 ROM, 64x4 RAM, 23 I/O lines (different versions exist)
    - Intel – 8048 (1976)
      - 1÷4Kx8 ROM/EPROM, 64÷256x8 RAM, 20-27 I/O lines (different versions exist)

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- Basic properties
  - 111 commands (49 1B, 45 2B, 17 3B)
    - Arithmetical (incl. mul/div), logical, bit, jump, i/o
    - Most execute in 1-2 machine cycles (mul/div – 4)
  - Clock up to 12 MHz (machine cycle 1 µs)
  - Separate program and data memories
  - 2-level, 5-source interrupt system
  - Built-in i/o interfaces
    - Timers/counters
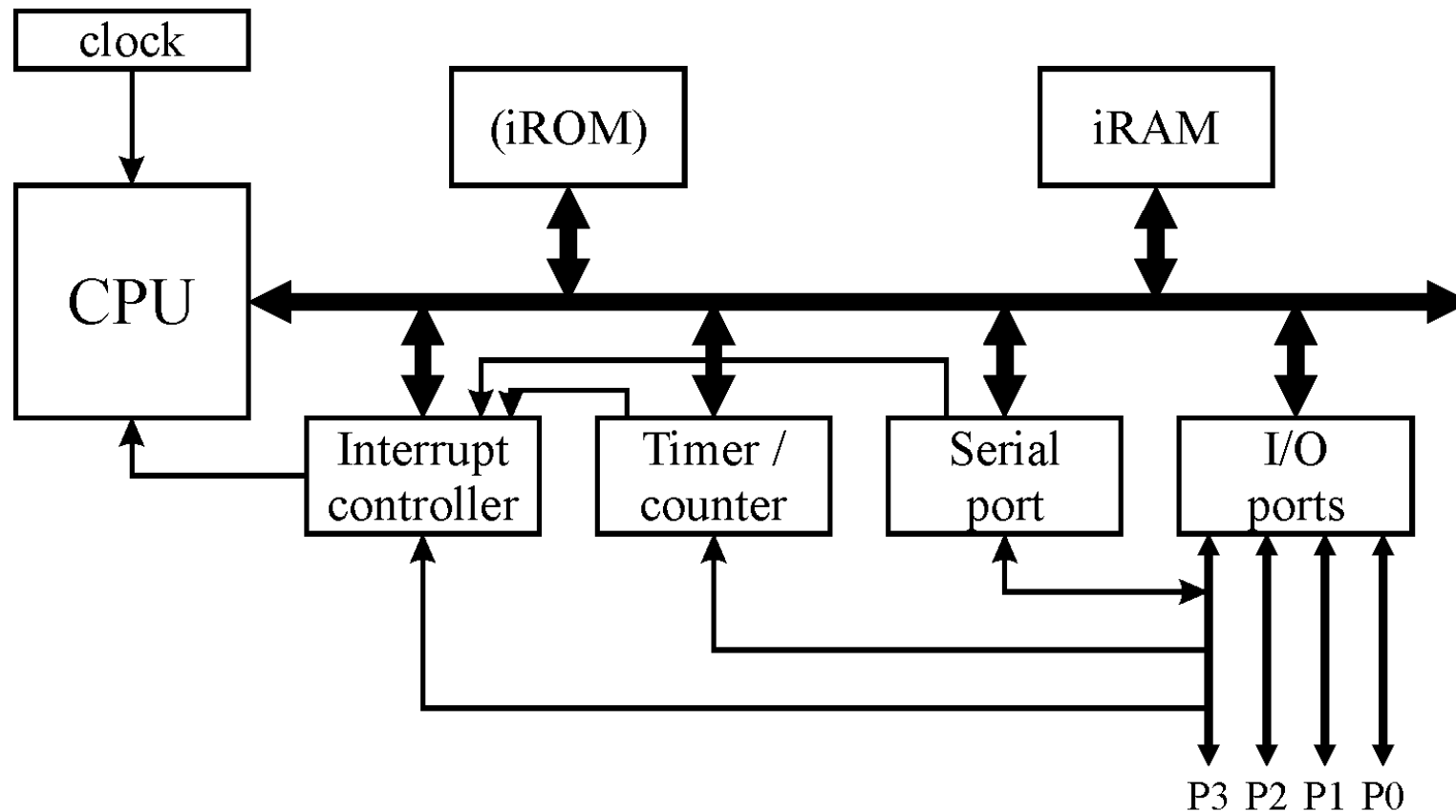   - I/O ports
    - Serial port(s)

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- Extended versions
  - Philips
    - I^2C
  - Siemens
    - CAN
  - Dallas/Maxim
    - Improved structure (works 3 times faster)
    - Double DPTR
  - SMC
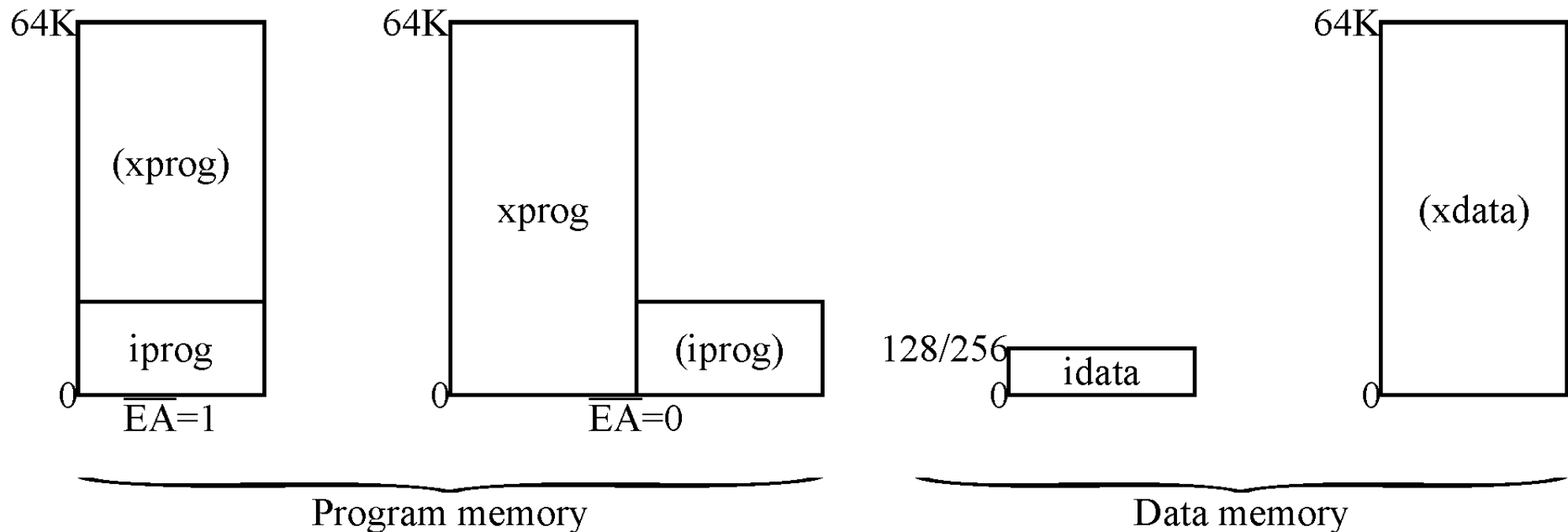   - ArcNET
  - TI
    - 8051 with radio interface

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- General simplified structure
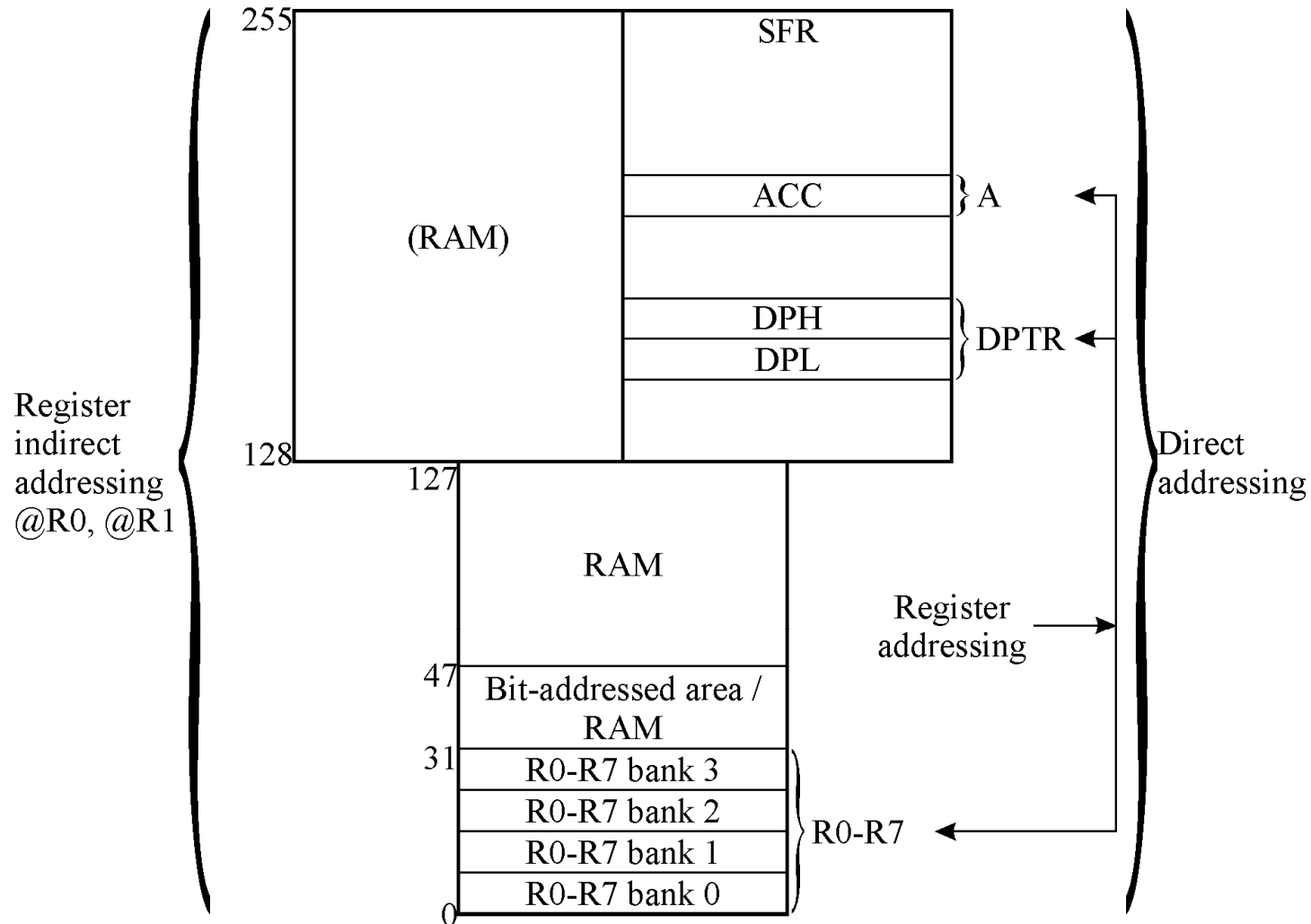
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- Memory organisation
  - Program memory
    - Internal, external, or both
    - Single addressing space
  - Data memory
    - Internal and/or external
    - Separate addressing spaces
    - Different commands and addressing modes

Program memory | Data memory

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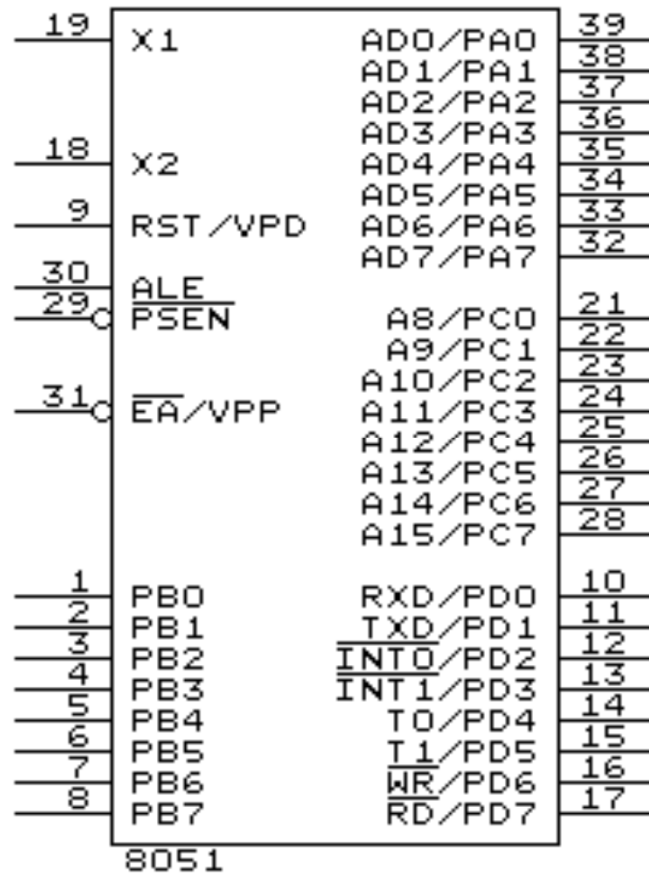
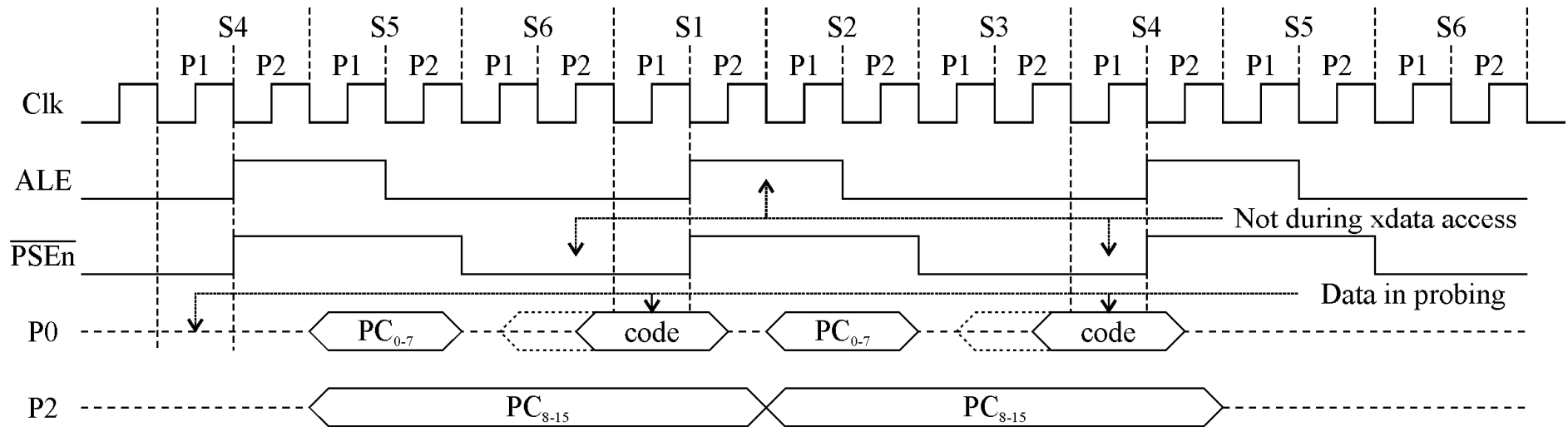- Internal data memory organisation

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- Pinout, signals

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- Machine cycle
  - 6 states (S1-S6) of 2 phases (P1-P2) each
  - S1, S4 – command code fetch
  - S2 – command decode, PC++
  - S4 – argument read, idle next command fetch

  - Almost all commands – 1-2 machine cycles
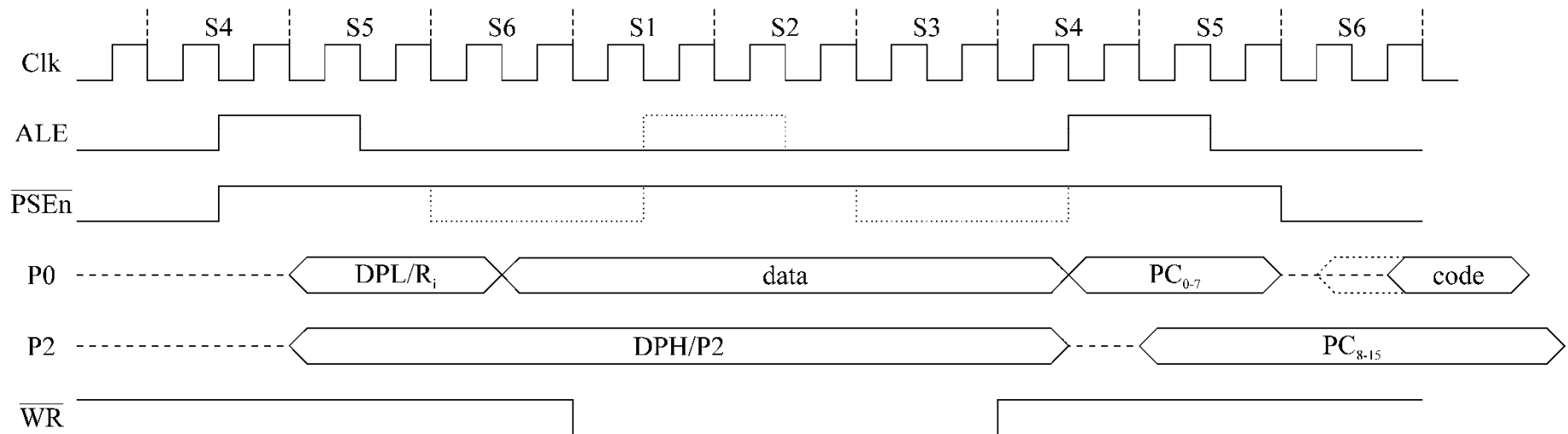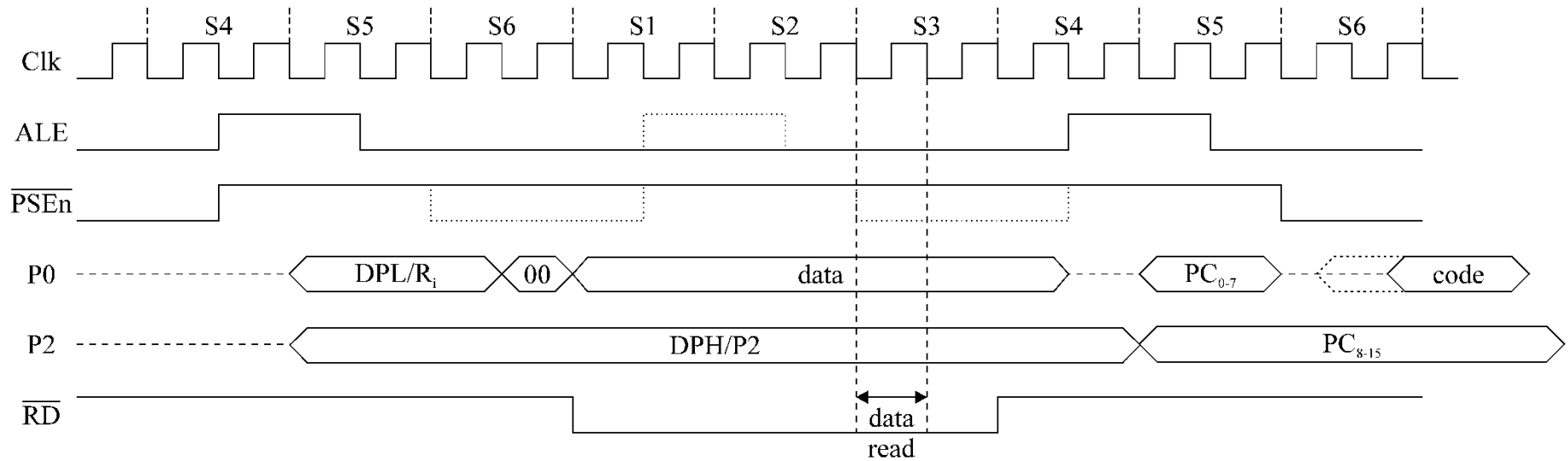 - Mul/div command – 4 machine cycles
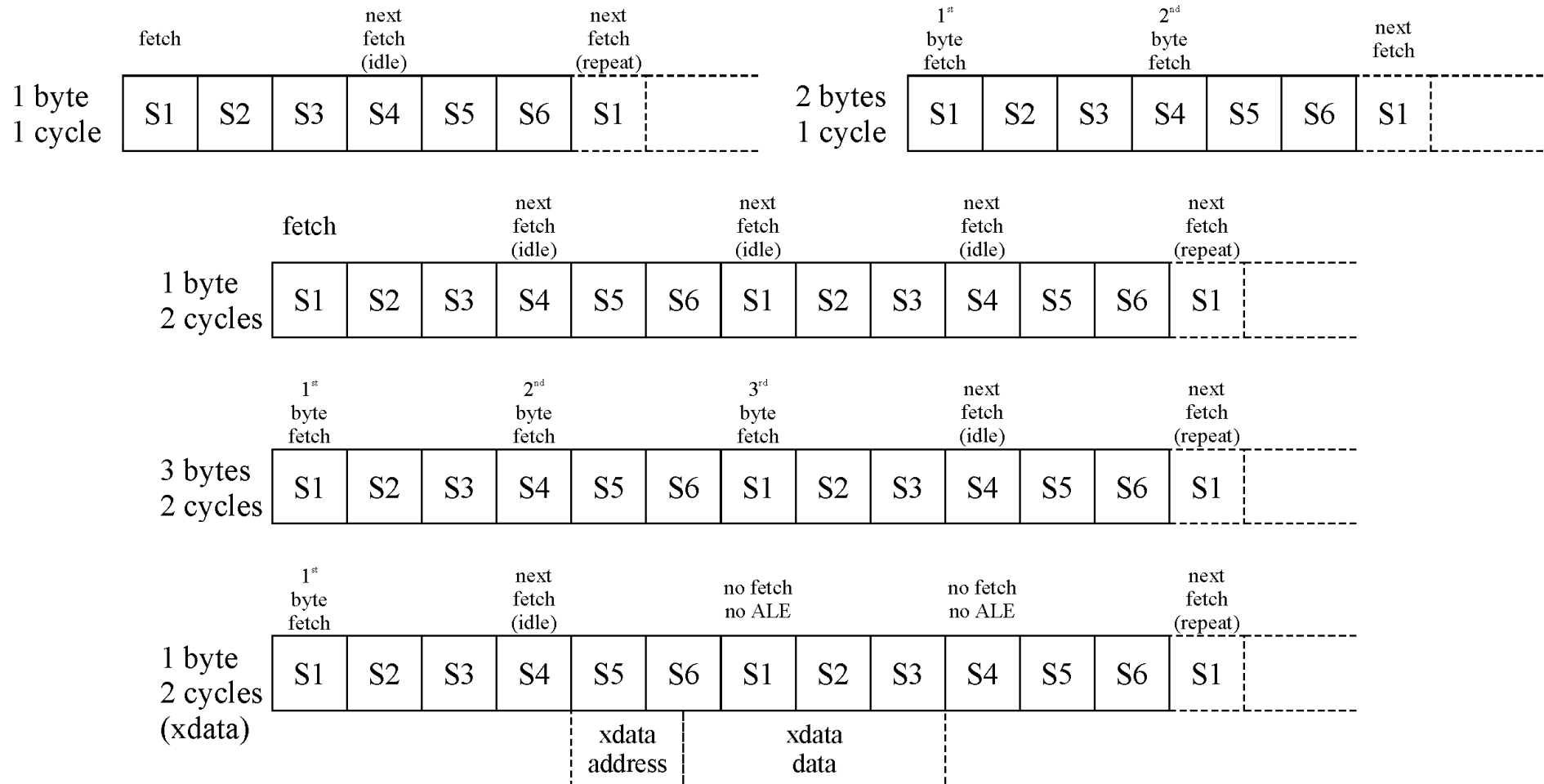
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- Command code fetch machine cycle

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- xdata read/write machine cycles

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- ## Command types and machine cycles

1 byte 1 cycle

fetch						next fetch (idle)	next fetch (repeat)
S1	S2	S3	S4	S5	S6	S1	

2 bytes 1 cycle

1st byte fetch						2nd byte fetch	next fetch
S1	S2	S3	S4	S5	S6	S1	

1 byte 2 cycles

fetch						next fetch (idle)						next fetch (idle)	next fetch (idle)	next fetch (repeat)
S1	S2	S3	S4	S5	S6	S1	S2	S3	S4	S5	S6	S1		

3 bytes 2 cycles

1st byte fetch						2nd byte fetch			3rd byte fetch			next fetch (idle)	next fetch (repeat)
S1	S2	S3	S4	S5	S6	S1	S2	S3	S4	S5	S6	S1	

1 byte 2 cycles (xdata)

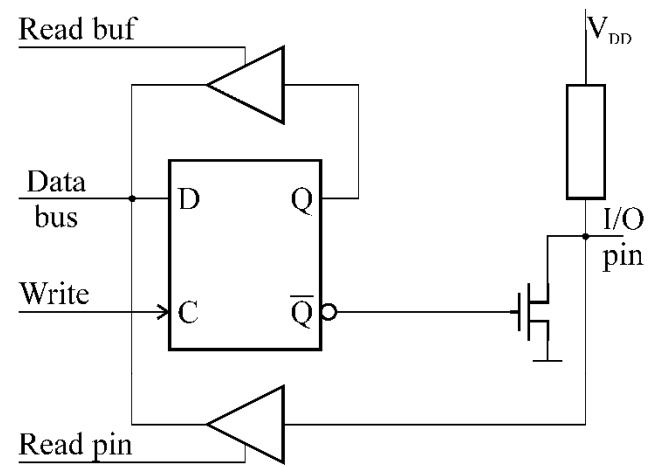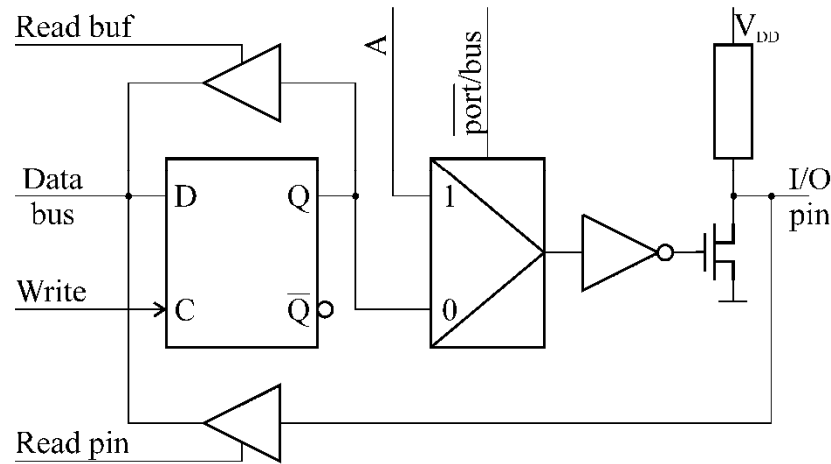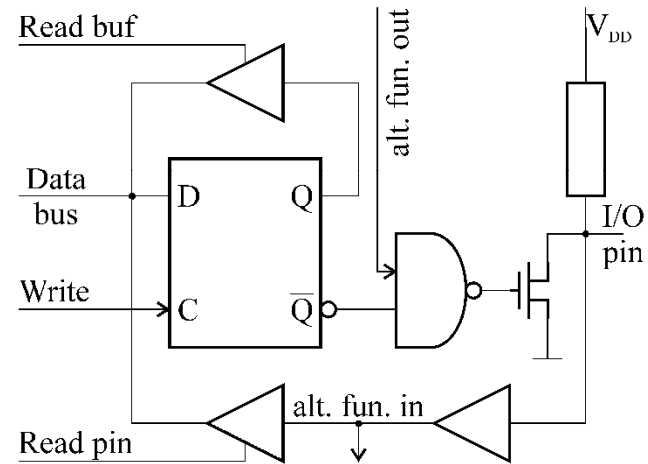| 1st byte fetch						next fetch (idle)			no fetch no ALE			no fetch no ALE	next fetch (repeat)
S1	S2	S3	S4	S5	S6	S1	S2	S3	S4	S5	S6	S1	

xdata address — xdata data

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- ## Ports structure

Port 0

Port 1

Port 2

Port 3