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Microprocessor and Embedded Systems

Faculty of Automatic Control, Electronics and Computer Science, Informatics, Bachelor Degree

Lecture 2

Microprocessor and environment data exchange Z-80 microprocessor

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Data exchange…

Program:

(last week)

- Elements of a microprocessor system
- Fundamental microprocessor structure
- Microprocessor operation cycles
- Basic addressing modes

(today)

- Data exchange between a microprocessor and its environment
- Z-80 microprocessor

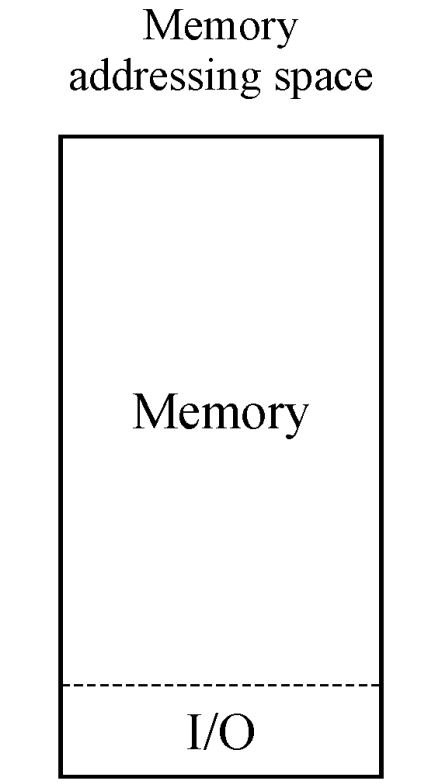
Data exchange…

- Microprocessor system environment
  - Office
    - Keyboard, mouse, display (monitor), computer network, printer, scanner, ploter, pendrive, portable hard disk….
    - But also built-in hard disk
  - Measurement and control
    - Controlled object
      - Digital inputs, analogue inputs (A/D converters), pulse inputs, bi-state inputs, etc.
      - Digital outputs, analogue outputs (D/A converters), pulse outputs (e.g., PWM), bi-state outputs, etc.

Data exchange…

- External devices connect via I/O interfaces
  - I/O interfaces:
    - **Simple IO**: output registers, input buffers, no status information, for „always ready” devices
    - **Universal programmable IO**: higher integration IC’s, programmable operation modes, status information present
    - **Dedicated controllers**: for high-complexity devices that require specialized control (HDD, monitor, network…)
    - **IO coprocessors** (e.g., modern graphic adapters?)
  - I/O interface selected with address

Data exchange…

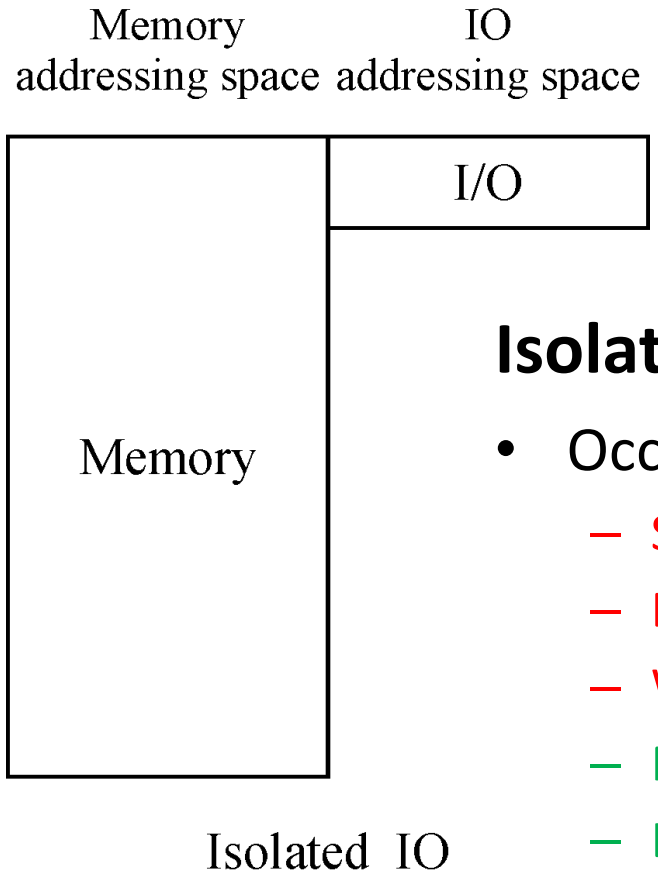


Memory-mapped IO

Memory-mapped IO

- Occuppies part of the memory addressing space
  - The same commands
  - The same addressing modes
  - Works with every microprocessor
  - Less memory
  - More complex address decoding
  - (!) less stability

Data exchange…



Isolated IO

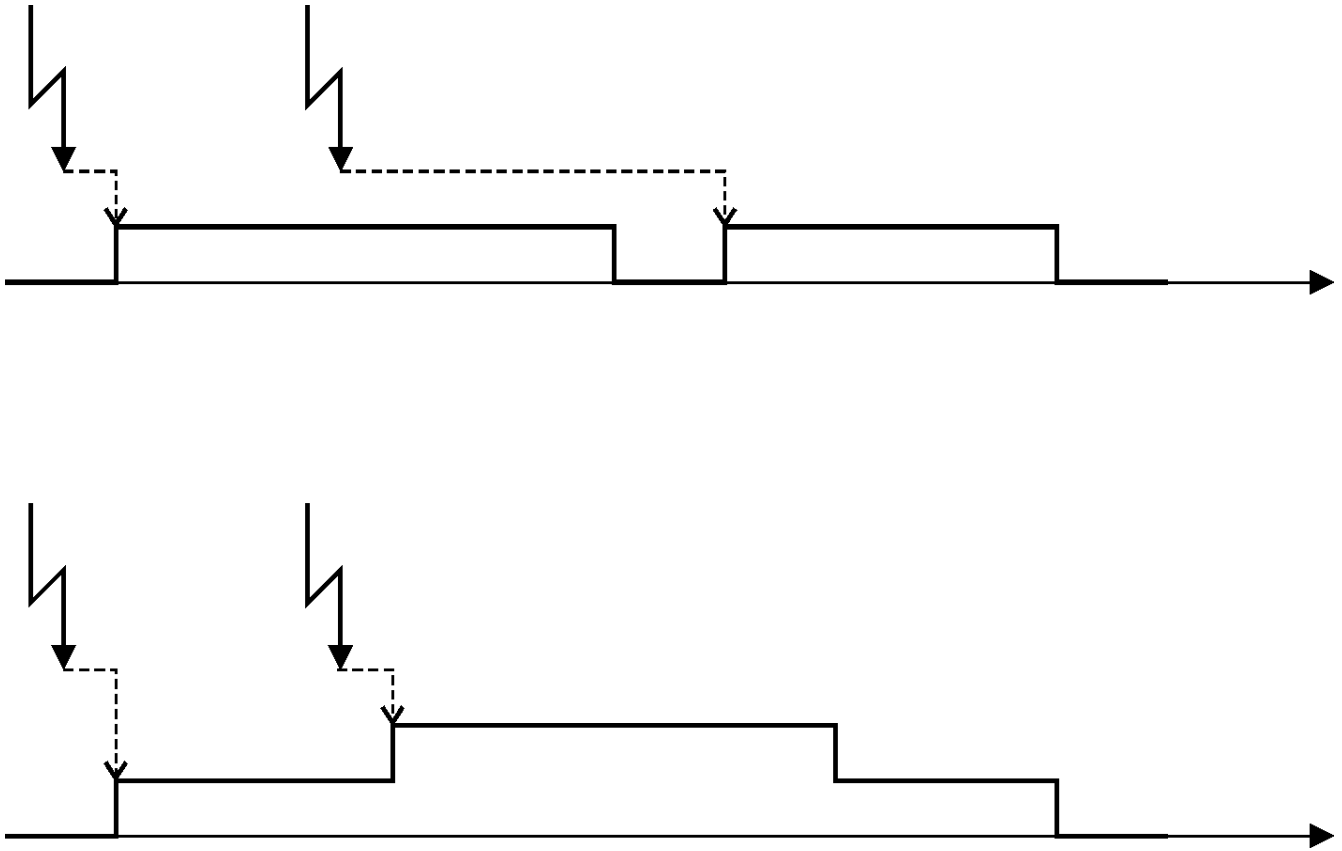
- Occuppies separate addressing space
  - Specialised commands
  - Different addressing modes
  - Works with NOT every microprocessor
  - More memory
  - Less complex address decoding
  - (!) more stability

Data exchange…

- Data exchange methods
  - Polling
    - Cyclic software read of all status registers
  - Interrupts
    - Requested by the ready devices
    - Hardware/software identification
    - Single level/multi-level
    - Hierarchical/round-robin priorities
    - Maskable/non-maskable interrupts (NMI)
  - Direct memory access (DMA)
    - Bus controlled by a DMA controller, not a microprocessor

Data exchange…

- Single level vs multi-level interrupt system

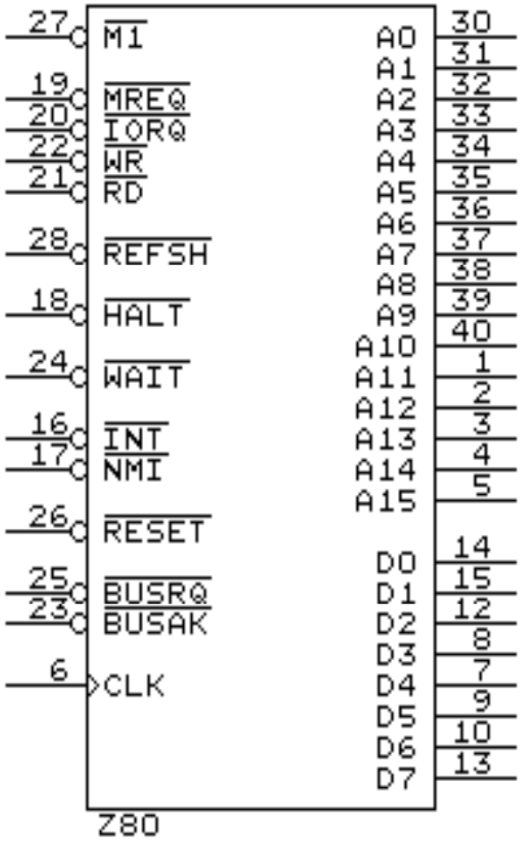


Z-80 microprocessor

- Basic properties
  - Single power voltage
  - 16 adress lines, 8 data lines
  - Clock 2.5 to 10 MHz (currently up to 20 MHz)
  - Single power voltage
  - 158 commands + undocumented command list
  - Two interchangeable register sets
  - 2 interrupt inputs, 3 interrupt modes
  - DRAM refresh

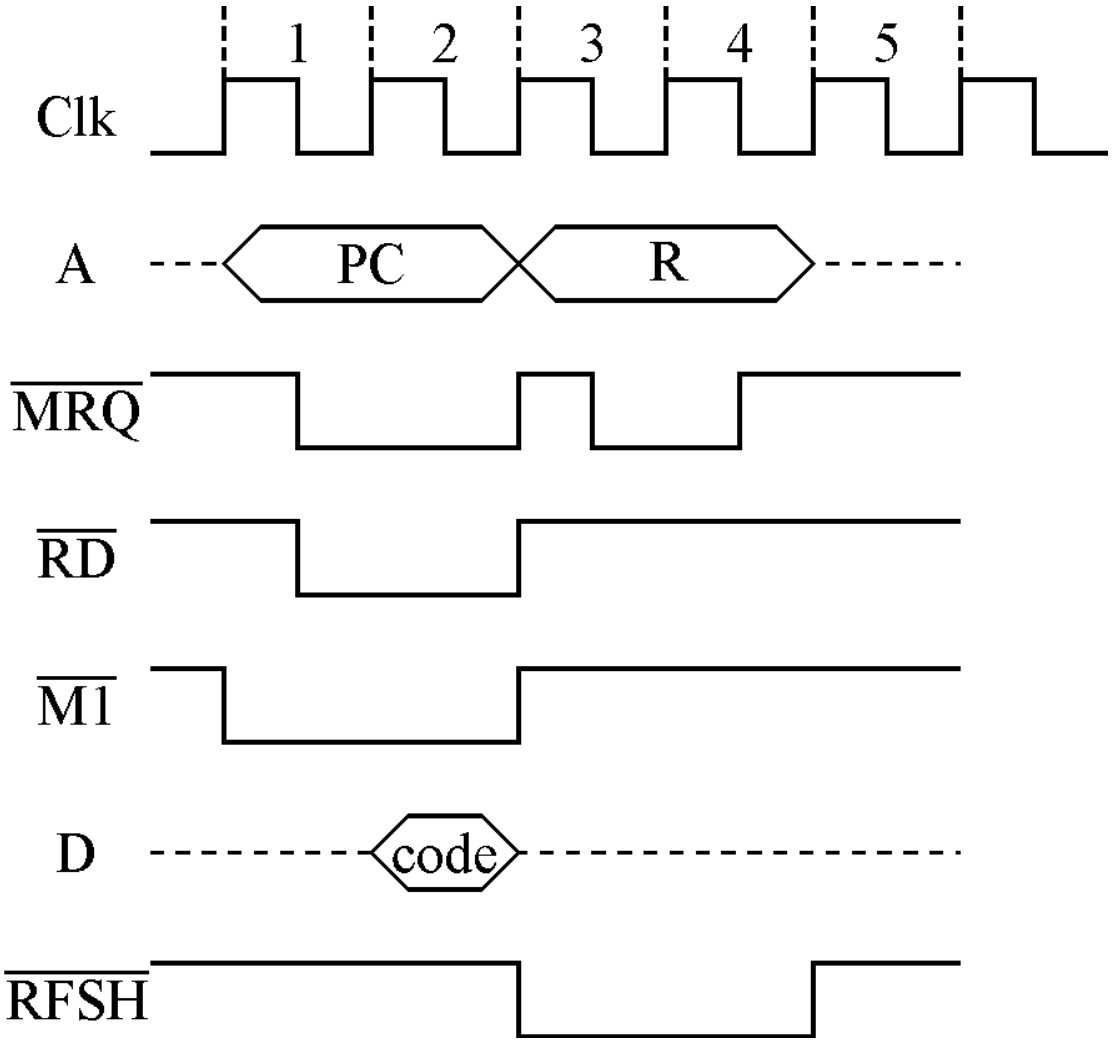
Z-80 microprocessor

- Pinout



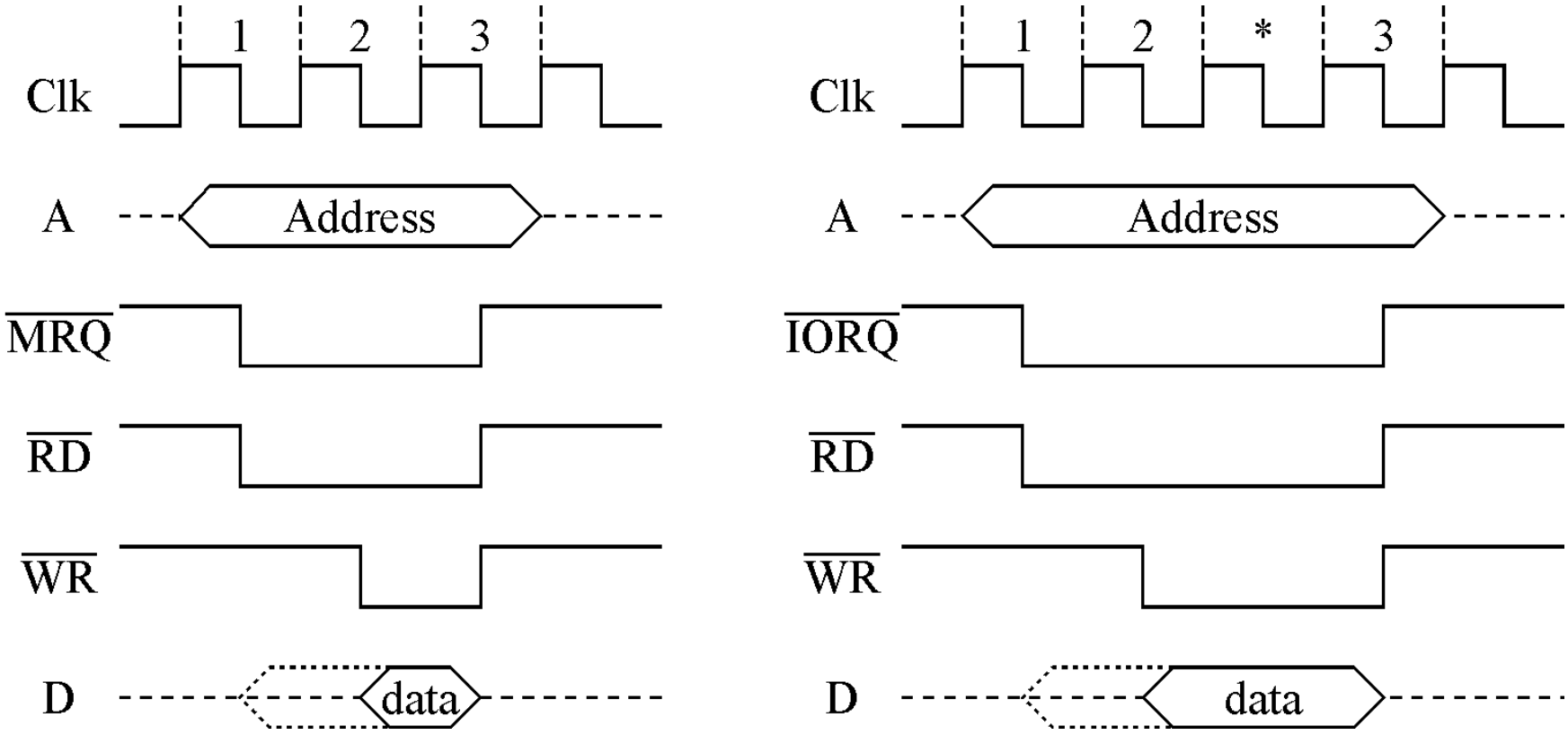
Z-80 microprocessor

- M1 cycle



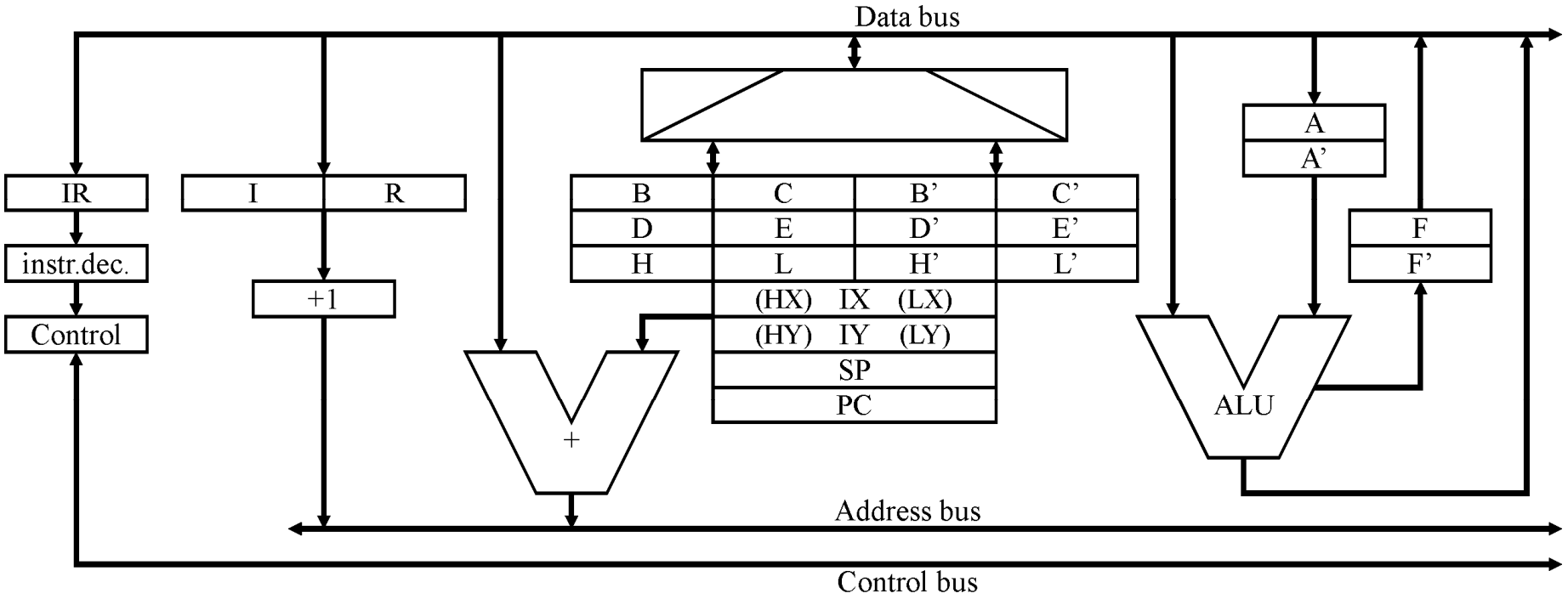
Z-80 microprocessor

- Mem/IO Rd/Wr cycles



Z-80 microprocessor

- Simplified structure



Z-80 microprocessor

- Registers:
  - A – accummulator
  - F – flags
  - BC, DE, HL – joined 8-bit registers, unequally used
    - H, L – traditional name from 8080 µp
    - HL – jump commands, 16-b accummulator
    - BC – counter, IO address
    - IX, IY – index registers

Z-80 microprocessor

- Flags:
  - C – carry/borrow (also in shift and rotation)
  - Z – zero (result = 0)
  - S – sign (A_7 bit)
  - P/V – parity/overflow
    - After logical command – 1, if even numer of 1's in A
    - After arithmetical command – 1, if overflow
  - H – half carry/borrow from A_3
    - used for decimal correction
  - N – substract (1 immediately after substraction)
    - used for decimal correction

Z-80 microprocessor

- Commands:
  - 1B or 2B data transfer
  - Exchange
  - Arithmetical/logical 1B, arithmetical 2B
  - Shift, rotation
  - Data block (string)
  - Single bit
  - Jump, procedure call, return
  - Microprocessor control
  - i/o

Z-80 microprocessor

- Addressing modes
  - Implied, e.g. `CPL`; `LD SP,IY`; `SUB 10` (A=A-10)
  - Immediate: `ADD A,n`; `XOR n`; `LD IXL, n`
  - Extended immediate: `LD HL, nn`; `JP nn`
  - Register: `RL r`; `AND r`
  - Register indirect: `LD A, (BC)`; `INC (HL)`
  - Extended (direct): `LD A, (nn)`; `LD (nn), HL`
  - Modified page zero: `RST p`
  - Relative: `JR Z, d`
  - Indexed: `AND (IX + d)`; `LD (IY + d), N`
  - Bit: `SET 0, B`; `SET 7, (HL)`

https://8bitnotes.com/2017/05/z80-addressing-modes/

Z-80 microprocessor

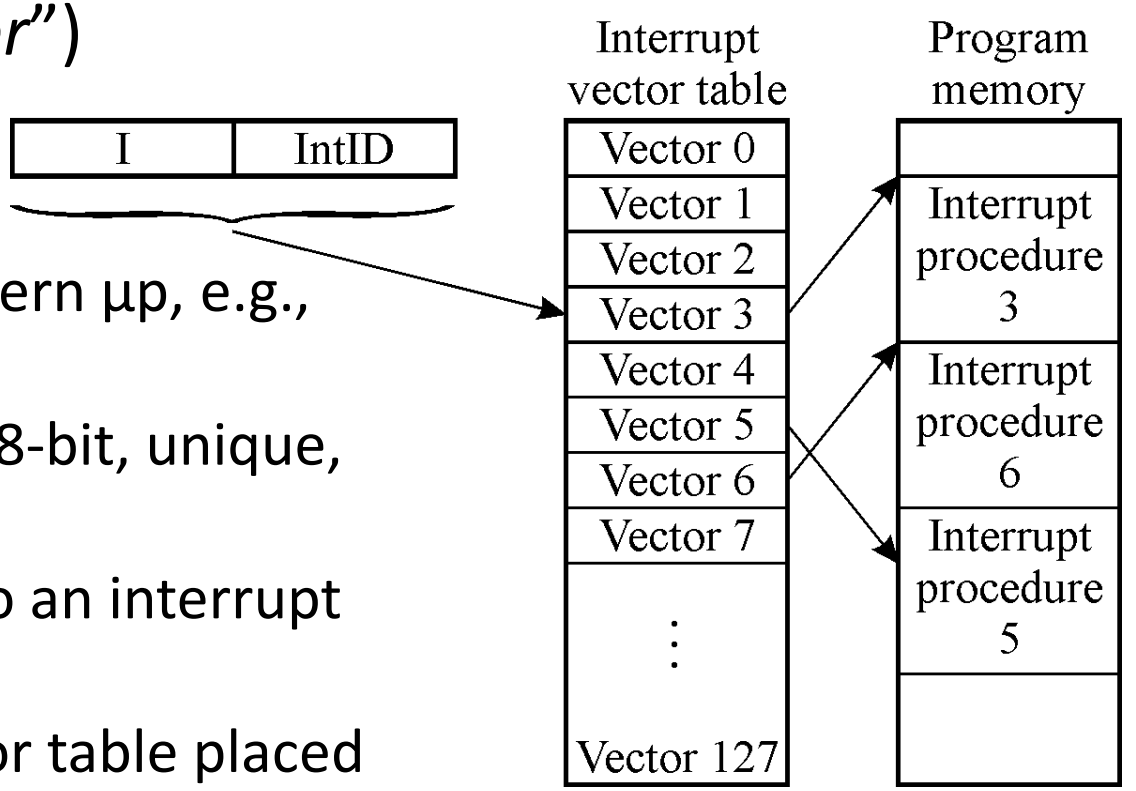
- Interrupts
  - NMI
    - non-maskable
    - Higher priority
    - Procedure starts at 0066h
    - Accepted always if $\overline{\mathrm{BUSRQ}}$=1
  - INT
    - Maskable
    - Lower priority
    - When accepted, $\overline{\mathrm{IORQ}}$=$\overline{\mathrm{M1}}$=0
    - Three different service modes

Z-80 microprocessor

- Maskable interrupt service modes
  - Mode 0 („*historical*”)
    - As in 8080
    - µp expects `RST p` command
    - Procedures start at `p`
      - `p`=(0..7)×8=0, 8, 16, 24…56
    - 8 hardware recognised interrupts
  - Mode 1 („*single chip*”)
    - µp expects nothing
    - Procedure starts at 0038h

Z-80 microprocessor

- Maskable interrupt modes
  - Mode 2 („*vector*”)



- Similar to modern µp, e.g., 8086 family
- µp expects an 8-bit, unique, interrupt ID
- IntID – index to an interrupt vector table
- Interrupt vector table placed in memory at location pointed by the content of I register

Z-80 microprocessor

- Z80 IC family
  - PIO, CTC, DMA, SIO, DART…
  - Z80 clones
- Z80 applications
  - Home µc (ZX Spectrum, Amstrad, CP/M-based)
  - Embedded systems (e.g., TNC controllers)
- Z80 as a single chip µc
  - CPU + PIO + CTC + SIO in a single IC
  - Add some memory and you get a complete µc
  - Many original IC disadvantages fixed