

Rzeczpospolita Polska

Unia Europejska Europejski Fundusz Społeczny



Politechnika Śląska jako Centrum Nowoczesnego Kształcenia opartego o badania i innowacje

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Microprocessor and Embedded Systems

Faculty of Automatic Control, Electronics and Computer Science, Informatics, Bachelor Degree

Lecture 1

Microprocessor systems structure and elements

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Program:

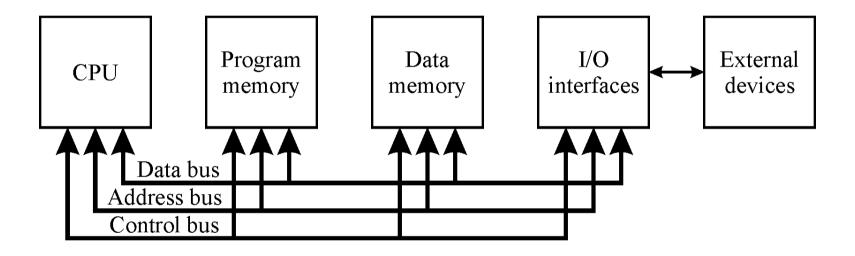
(today)

- Elements of a microprocessor system
- Fundamental microprocessor structure
- Microprocessor operation cycles
- Basic addressing modes

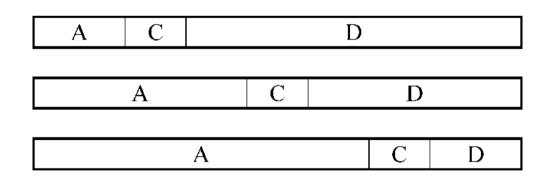
(next week)

 Data exchange between a microprocessor and its environment

• Elements of the computer system



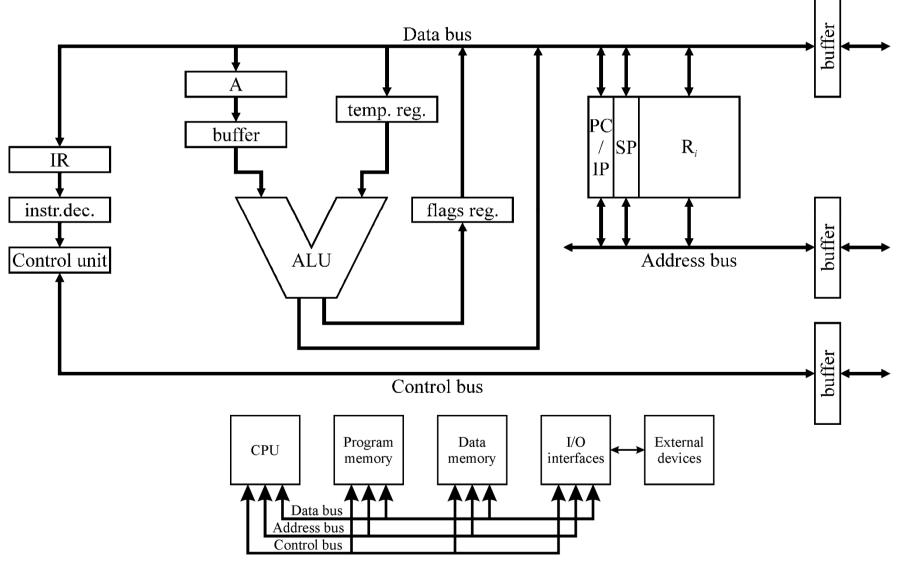
- Elements of the computer system
 - Bus
 - Parallel
 - Separate address, data, control signals
 - Serial
 - Common signals for address, data & control



- Elements of the computer system
 - CPU (μp)
 - Data processing centre
 - Capabilities depend on command list
 - CISC/RISC
 - Functionally complete: can implement every algorithm
 - Algorithm \rightarrow program
 - Algrorithm = elementary operations sequence
 - Elementary operation \rightarrow command
 - Commands sequence = program
 - Commands executed after μp reads its binary code

- Elements of the computer system
 - Program memory
 - RAM or ROM?
 - Single-purpose vs. multi-purpose µp system
 - Single-purpose: program \rightarrow ROM (EPROM, FLASH)
 - Multipurpose: program \rightarrow RAM
 - Data memory
 - RAM or ROM?
 - Data change more frequently than code
 - Really always?

• Von Neumann architecture



- Von Neumann architecture
 - μp operates on "words"
 - Word \rightarrow elementary data unit
 - Command code, data in some format, etc.
 - Length (*typically*): 4, 8, 16, 32, 64... bits
 - Data bus
 - For data transfer
 - State determined by μp or environment
 - Address bus
 - To specify the address
 - State determined mostly/exclusively by μp

- Von Neumann architecture
 - ALU
 - Processes data
 - ADD, SUB, AND, OR, NOT, SHL, SHR, CMP, ...
 - Result may influence on command exec. sequence
 - Flags
 - "popular" flags
 - Carry
 - Auxilliary carry/half carry
 - Zero
 - Sign
 - Parity
 - Overflow
 - Can be set, reset or tested \rightarrow conditional jumps

- Von Neumann architecture
 - A(accumulator)
 - Outlined register for most of operations
 - Arithmetical, logical, $M \leftrightarrow IO$, etc.
 - Input argument, result
 - In some µp's
 - Shorter execution time
 - Shorter command code
 - *n*-bits in accumulator \rightarrow *n*-bit µp

- μp operation cycles
 - Clock cycle
 - μp is a sequential synchronous circuit
 - f_{max}
 - f_{min} (dynamic/static μp's)
 - Machine cycle
 - Operation performed on bus
 - Fetch, MemRd, MemWr, IORd, IOWr, ...
 - Command cycle
 - Fetch phase \rightarrow 1..few Fetch machine cycles
 - Execution phase \rightarrow 0..many machine cycles

- Addressing modes
 - Methods of data address determination

