Fundusze Europejskie
Wiedza Edukacja Rozwój

Unia Europejska
Europejski Fundusz Społeczny

Politechnika Śląska jako Centrum Nowoczesnego Kształcenia
opartego o badania i innowacje

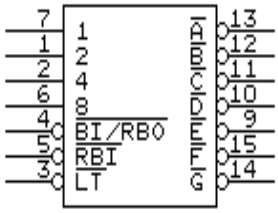
POWR-03.05.00-00-Z098/17-00

Digital Circuits Design

Faculty of Automatic Control, Electronics and Computer Science / Informatics, Engineer Degree, sem. 3

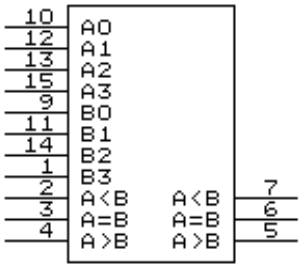
Materiały dydaktyczne współfinansowane przez Unię Europejską ze środków Europejskiego Funduszu Społecznego

7-segment display controllers

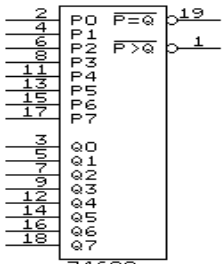


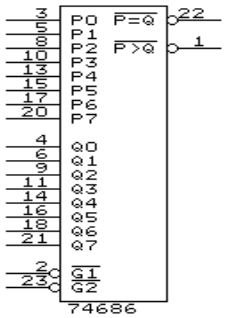
Digit comparators

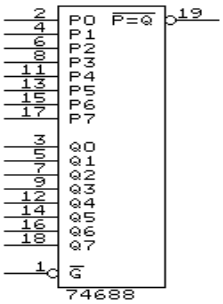
4-bit comparator



8-bit comparators







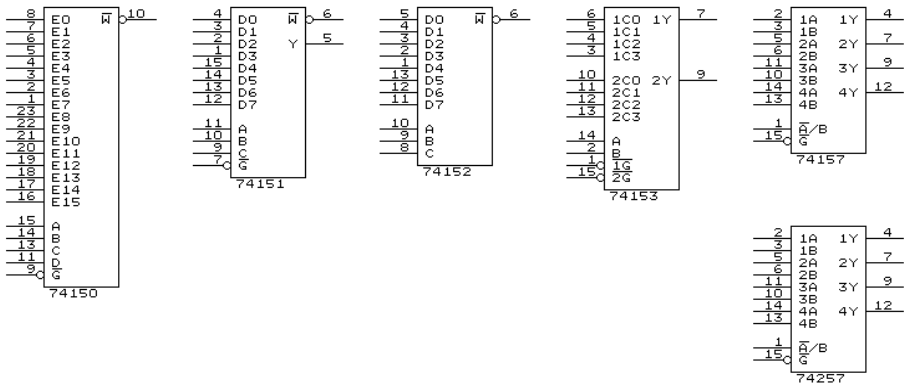
Properties of 8-bit comparators

Curcuit	gate inputs	output type	numer of outputs	pull-up resistors	Schmitt inputs
74682	-	totem-pole	2	yes	yes
74683	-	open collector	2	yes	yes
74684	-	totem-pole	2	-	yes
74685	-	open collector	2	-	yes
74686	2	totem-pole	2	-	yes
74687	2	open collector	2	-	yes
74688	1	totem-pole	1	-	-
74689	1	open collector	1	-	-

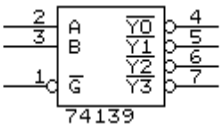
comparator outputs states

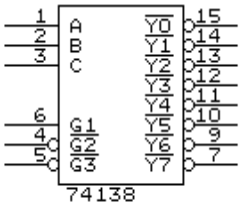
relations	$\overline{P = Q}$ output	$\overline{P > Q}$ output
P<Q	„1”	„1”
P=Q	„0”	„1”
P>Q	„1”	„0”

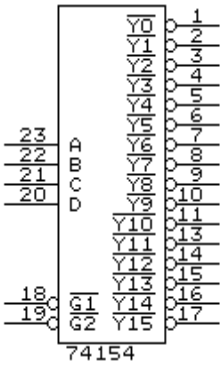
Multiplexers



Demultiplexers


2
3
1
A
B
G
Y0
Y1
Y2
Y3
4
5
6
7
74139

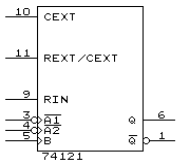

1
2
3
6
4
5
A
B
C
G1
G2
G3
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
15
14
13
12
11
10
9
7
74138


23
22
21
20
18
19
A
B
C
D
G1
G2
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
Y10
Y11
Y12
Y13
Y14
Y15
1
2
3
4
5
6
7
8
9
10
11
13
14
15
16
17
74154

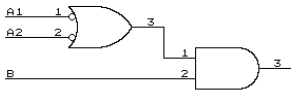
Time circuits

74121

$t_w = C_T \cdot R_T \cdot \ln 2.$

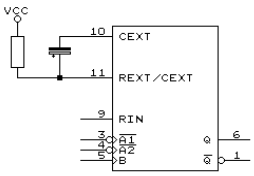


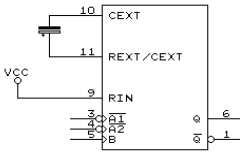
pins



trigger function

delay time determination



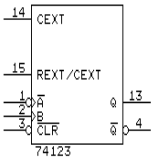


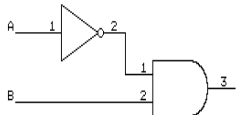
74123

$$t_w[\text{ns}] = a \cdot C_T[\text{pF}] \cdot R_T[\text{k}\Omega] \cdot \left(1 + \frac{0{,}7}{R_T[\text{k}\Omega]}\right),$$

a=0,32, R_T=5-50 kΩ, C_T≥1000 pF; if diode is connected a=0,28, R_T <30 kΩ.

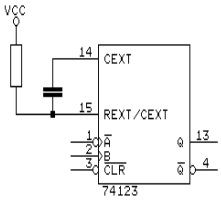
pins

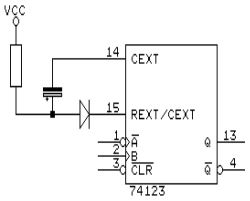




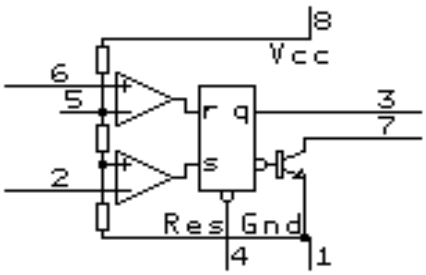
trigger function

delay time determination

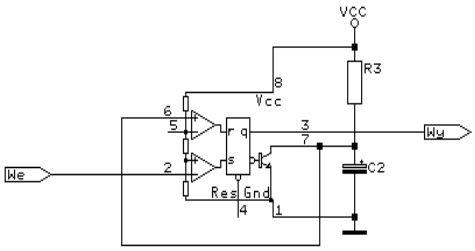


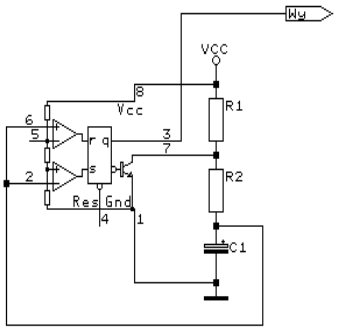


NE555



Pin number	Function
1	ground
2	trigger voltage
3	output
4	reset/clear (active low)
5	control voltage
6	threshold

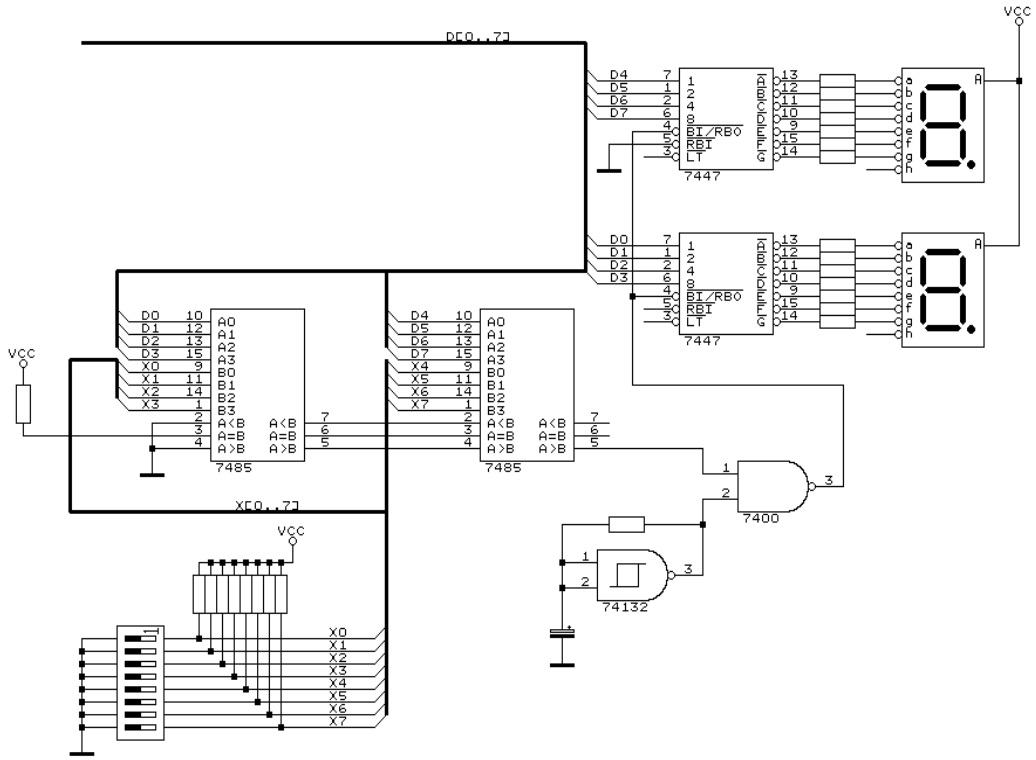

VCC
R3
8
Vcc
6
5
2
r
q
s
3
7
Wy
We
C2
Res
Gnd
4
1


Wy
VCC
8
Vcc
R1
6
5
2
r
q
s
3
7
R2
Res
Gnd
4
1
C1

Examples

Ex. 1

Design a circuit that displays two-digit decimal number. Digits are encoded in BCD 8421 code. If the number exceeds some limit, the display should pulse with few Hz frequency. Non-significant zeroes should be blanked.



Ex. 2

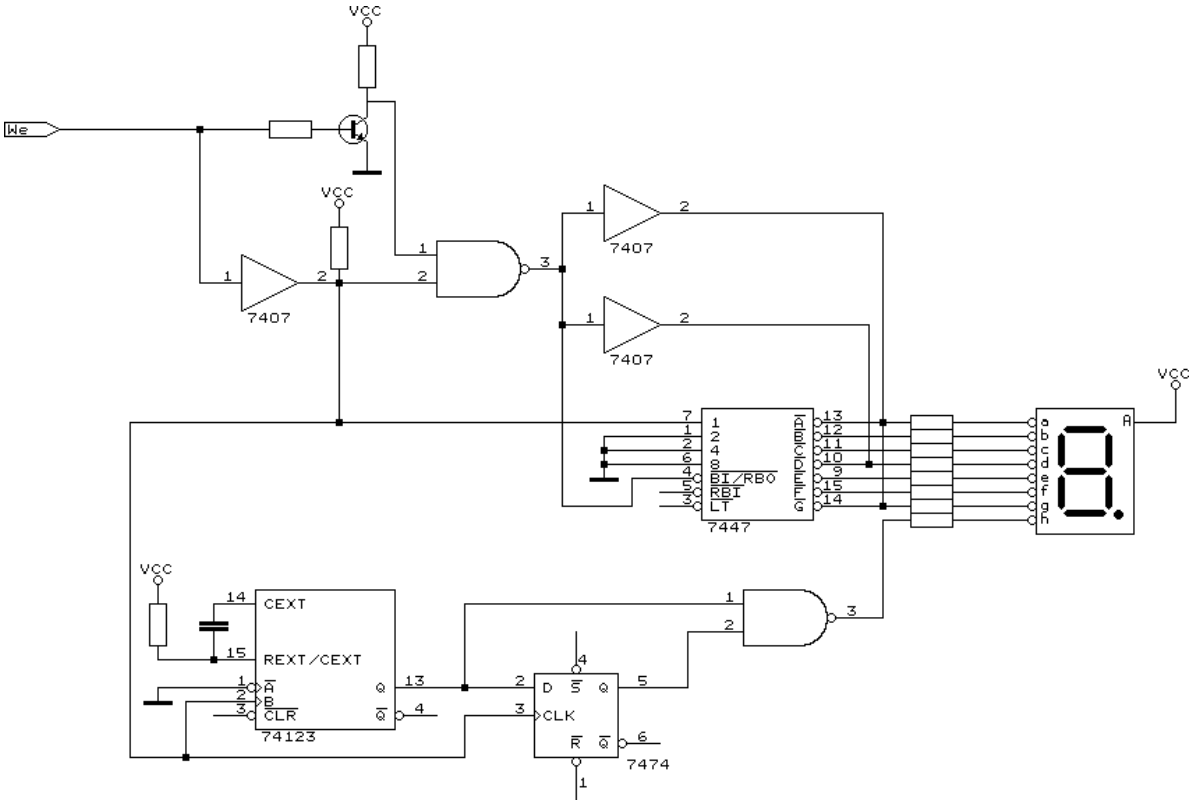
Desing a „logic pen”. The information should be displayed as shown below.

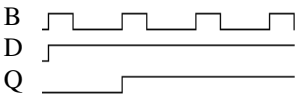
logic
high

high
impedance

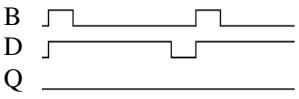
logic
low

f ≥20 Hz
square wave





f > 20 Hz



f < 20 Hz

Ex. 3

Desing a frequency generator using a single ‘121 circuit.

Ex. 4

Desing a 2-phase frequency generator using two ‘123 circuits: a) gated at the beginning of period, b) gated at the beginning of each phase.

Ex. 5

Desing a short pulse sequence generator using a single ‘123 circuit.

Ex. 6

Desing a frequency generator using short pulse sequence generator.