Fundusze Europejskie
Wiedza Edukacja Rozwój

Rzeczpospolita Polska

Unia Europejska
Europejski Fundusz Społeczny

Politechnika Śląska jako Centrum Nowoczesnego Kształcenia
opartego o badania i innowacje

POWR.03.05.00-IP.08-00-PZ1/17

Projekt współfinansowany przez Unię Europejską ze środków Europejskiego Funduszu Społecznego

Digital Circuits Design

Faculty of Automatic Control, Electronics and Computer Science, Informatics, Bachelor Degree

Lecture 6

Counters

Bartłomiej Zieliński, PhD, DSc

Counters

Program:

- Counter types
- Counter parameters
- Asynchronous counters
- Synchronous counters
- Counters of a shortened cycle length

Counters

- Counter
  - Counts and remembers the numer of input pulses given within a given time to the clock input
  - Control inputs
    - Reset/clear
    - Load
    - Direction selection
    - (syn/asyn)
    - Gate/enable
    - Write max state
    - ….

Counters

- Counters classification (1)
  - By operation rules
    - Modulo *s* (frequency divider by s)
    - Up to *s* (restart possible after initial state is forced)
  - By counting code
    - Decimal (BCD)
    - Binary
    - Others (octal, Johnson, etc.)
  - By cycle length
    - Constant
    - Configurable (variable)

Counters

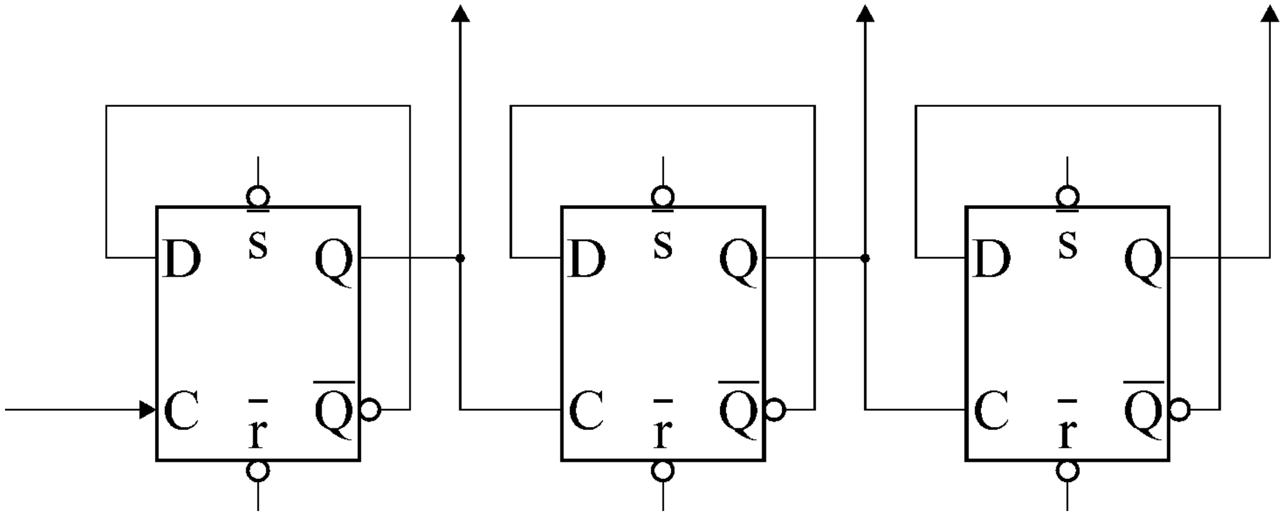
- Counters classification (2)
  - By counting direction
    - Unidirectional
      - Forward (inc)
      - Backward (dec)
    - Bidirectional
      - Direction selection input
      - Separate inc/dec inputs
  - By clock input influence on counter flip-flops
    - Asynchronous (only 1st flip-flop)
    - Synchronous (all flip-flops)
    - Syn-asyn (some flip-flops)

Counters

- Counters classification (3)
  - By carry generation inside and outside of the counter
    - Serial (*Serial Carry*, *Ripple Carry*) – simpler, slower
    - Parallel (*Parallel Carry*, *Look-Ahead Carry*) – more complex, faster
    - Serial-parallel

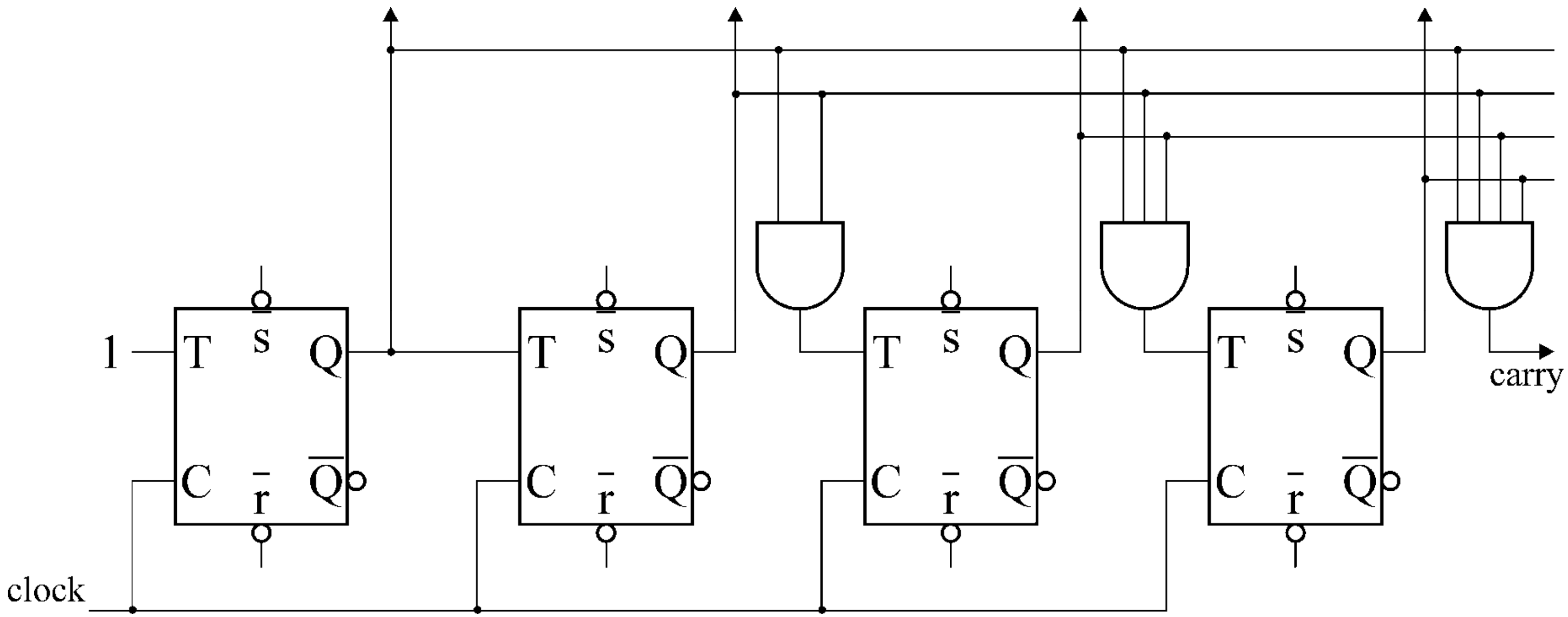
Counters

- Asynchronous counter



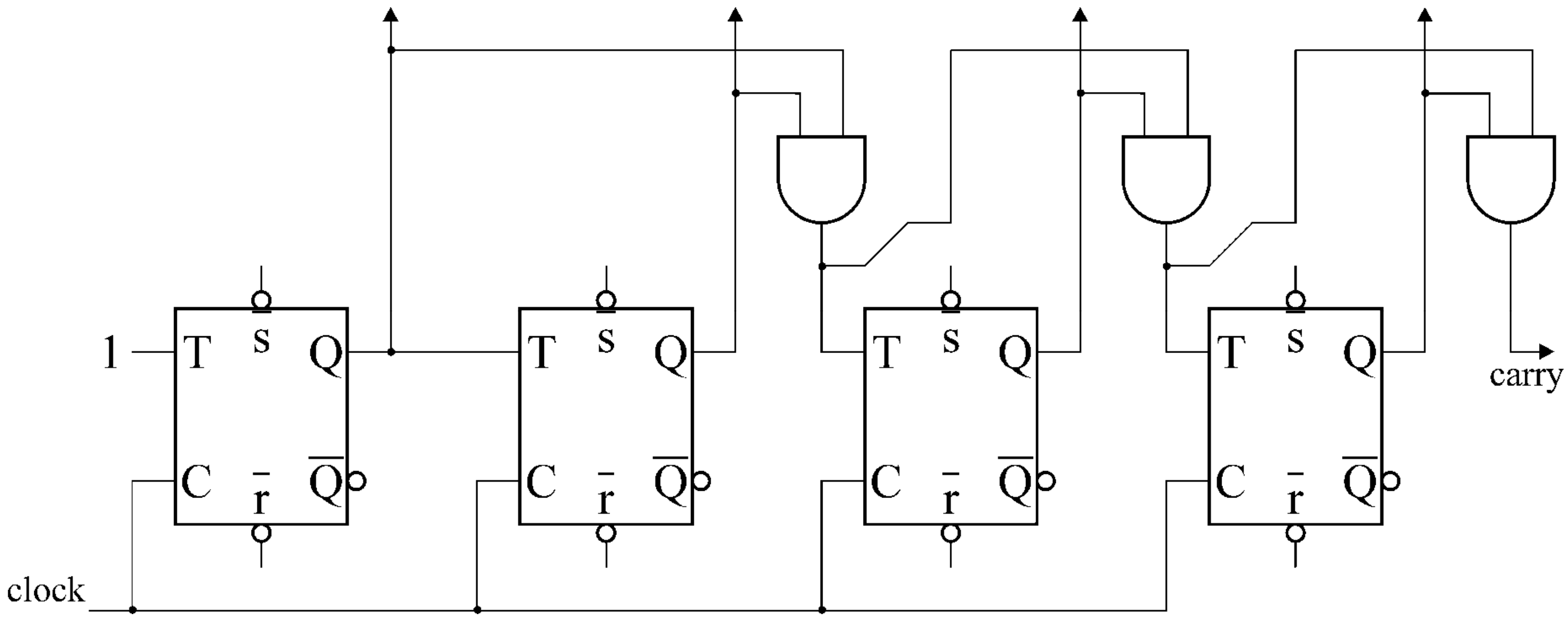
Counters

- Synchronous counter, parallel carry



Counters

- Synchronous counter, serial carry

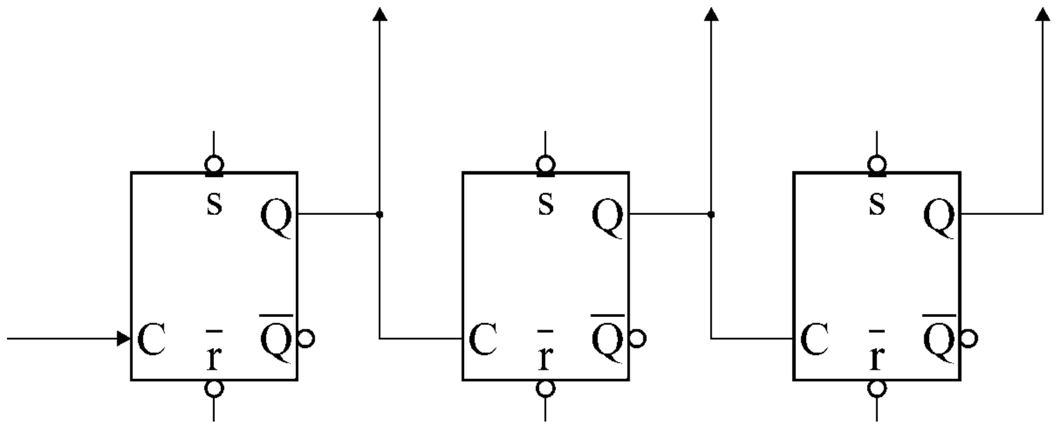


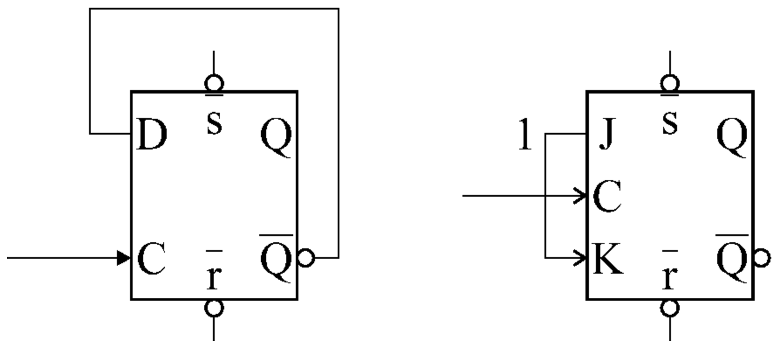
Counters

- Counters parameters
  - Operation speed → f_{max} of clock pulses
  - Content set time
- For asynchronous counters
  - $F_{max} < f_{max}$ of 1st flip-flop
  - Set time = Σt_p of all flip-flops: $f_{max} = {}^{1}/_{(nt_{pD}+t_o)}$
- For synchronous counters
  - Set time = Σt_p of carry generation circuit
  - Parallel carry: $f_{max} = {}^{1}/_{(t_{pD}+t_{pg})}$
  - Serial carry: $f_{max} = {}^{1}/_{(t_{pD}+(n-2)t_{pg})}$

Counters

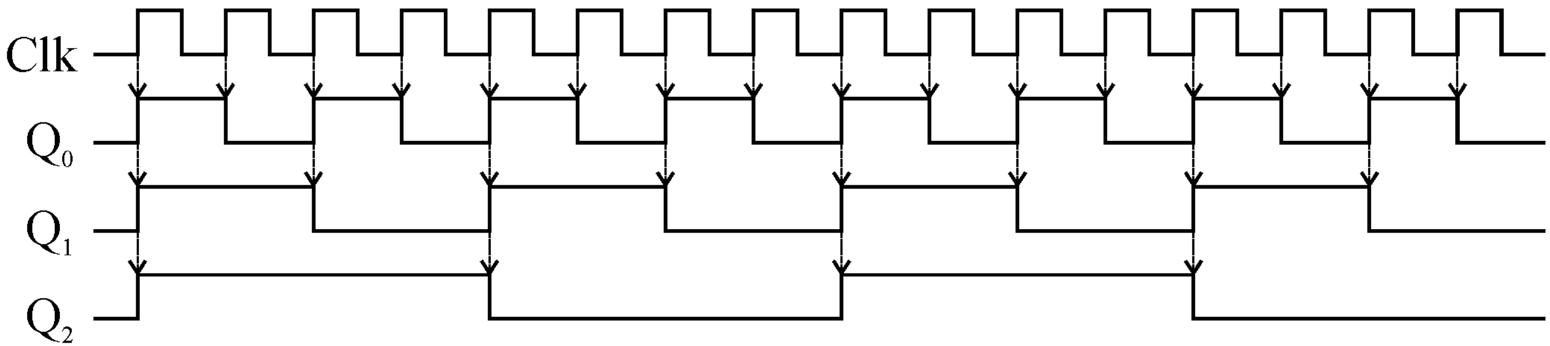
- Asynchronous counter

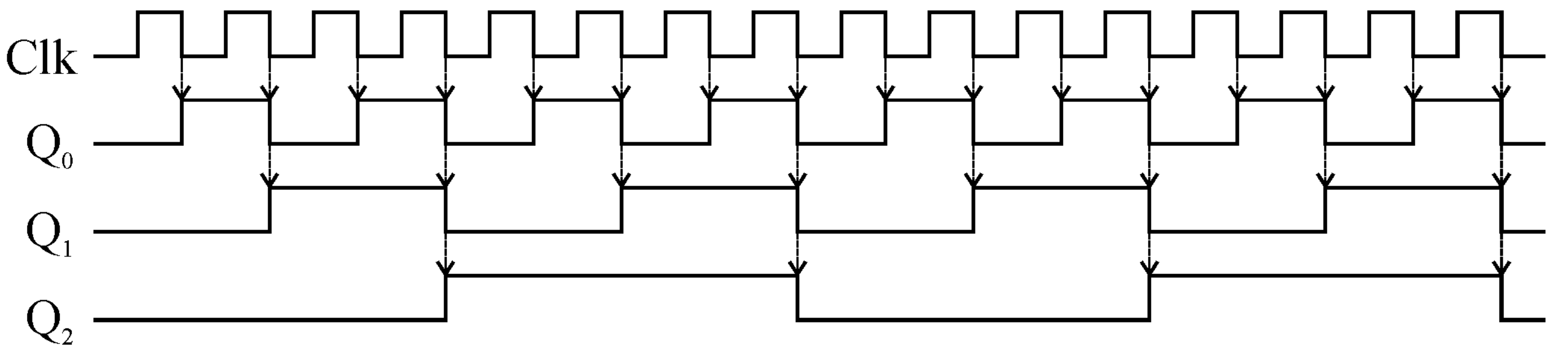




Counters

- Asynchronous counter

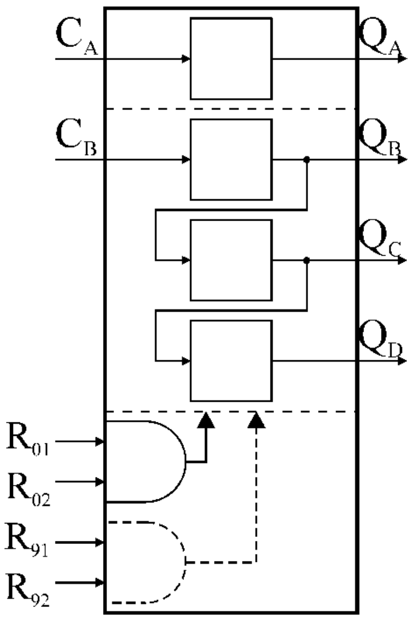


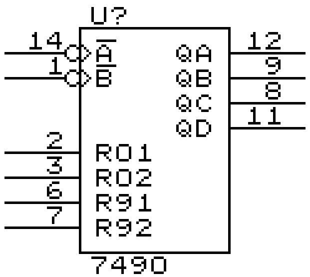


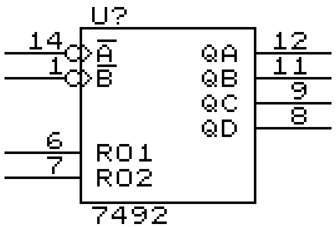
Counters

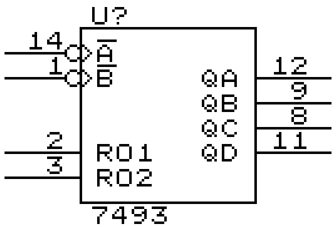
- Asynchronous counters
  - 749x family

Counter	Type	Counter	Code
7490	Decimal	Mod 2 mod 5	8421, 5421
7492	Dozenal	Mod 2 mod 6	6421, 6321
7493	Binary	Mod 2 mod 8	8421



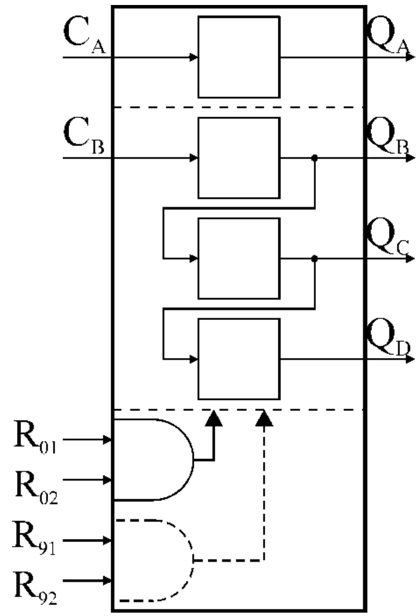






Counters

- Asynchronous counters
  - 7490:
    - $Q_A \rightarrow C_B$: 8421 code
    - $Q_D \rightarrow C_A$: 5421 code, η=½
  - 7492:
    - $Q_A \rightarrow C_B$: 6421 code
    - $Q_D \rightarrow C_A$: 6321 code, η=½
  - 7493:
    - $Q_A \rightarrow C_B$: 8421 code, η=½
    - $Q_D \rightarrow C_A$: 8421 code, η=½

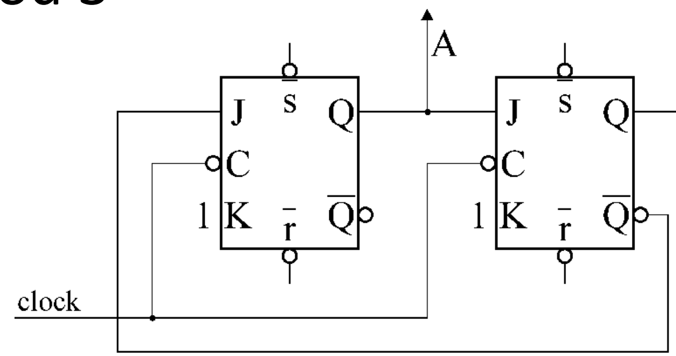


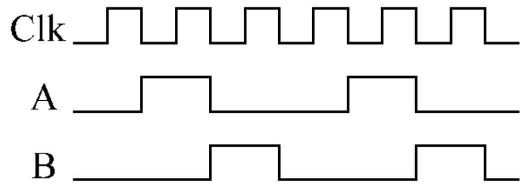
Counters

- Counters of a shortened cycle
  - Design a dedicated sequential circuit
  - Use a binary or decimal counter
    - Last cycle state detected → reset
      - Asynchronous reset → detect illegal state
      - Synchronous reset → detect last legal state

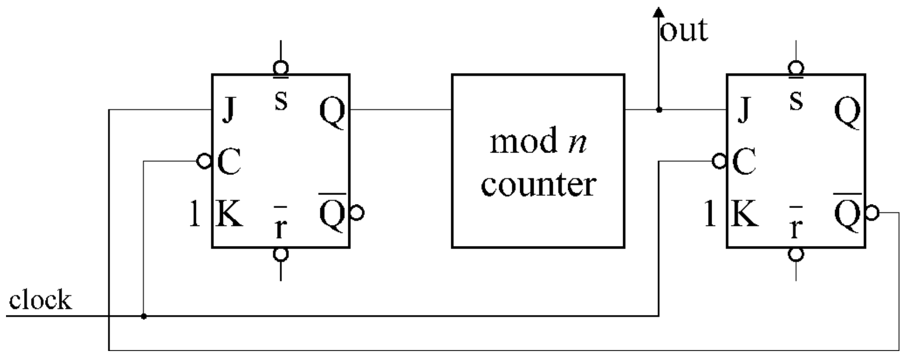
Counters

- Counters of a shortened cycle
  - Design a dedicated sequential circuit
    - Mod 3





    - Mod (2*n*+1)

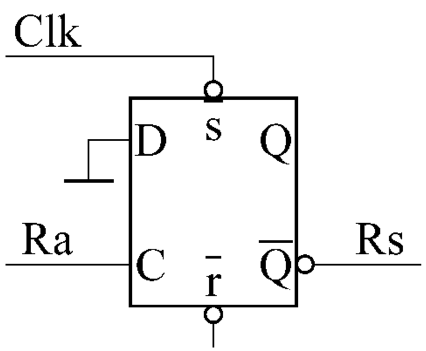


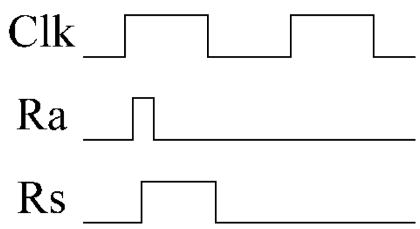
Counters

- Counters of a shortened cycle
  - Detect a forbidden state and reset
    - „Mod *n*” counter → detect *n* and immediately reset
      - Forbidden state exists for a short time
      - Zero state lasts for less than a clock period
      - Acceptable or not, depending on application

Counters

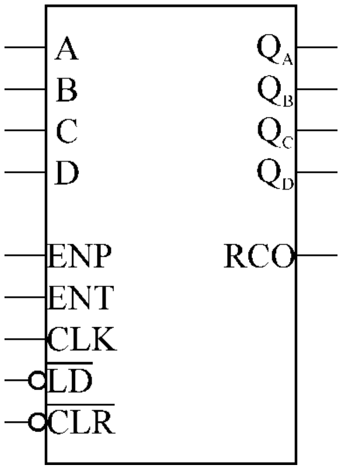
- Counters of a shortened cycle
  – Detect a forbidden state and reset
    - Multiple counters → reset can be too short
      – Some flip-flops are already cleared
      – Reset signal inactive
      – Some flip-flops may remain not reset
      → make reset signal longer
        » Pulse generators (121, 123, 555, …)
        » RC + Schmitt gates
        » Clock-synchronised flip-flop



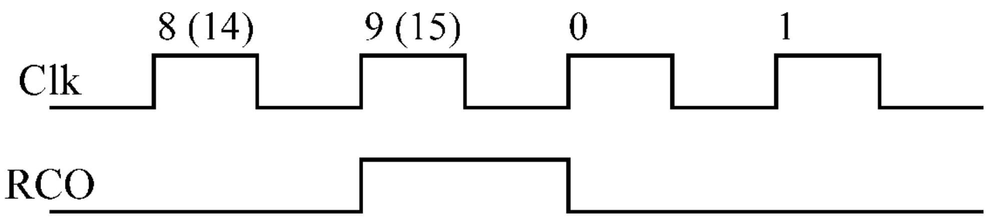


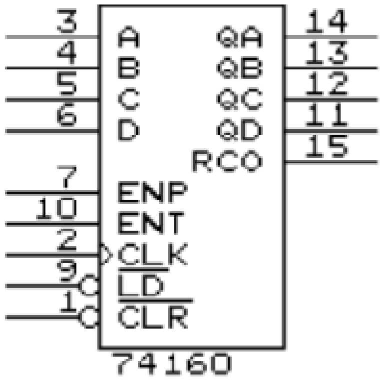
Counters

- Synchronous counters
  - Unidirectional counters – 16x family



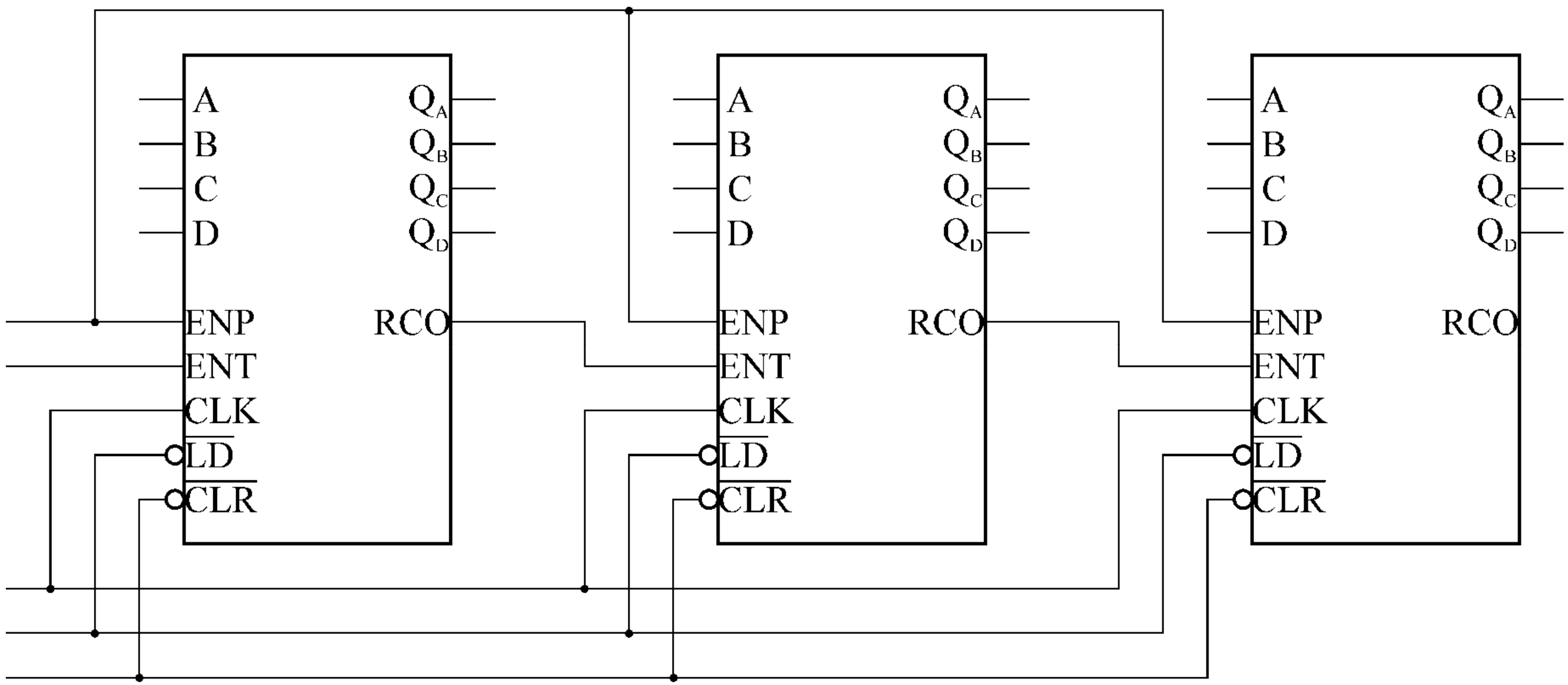
Circuit	Counter	Load	Clear
74160	Decimal	Synchronous	Asynchronous
74161	Binary	Synchronous	Asynchronous
74162	Decimal	Synchronous	Synchronous
74163	Binary	Synchronous	Synchronous





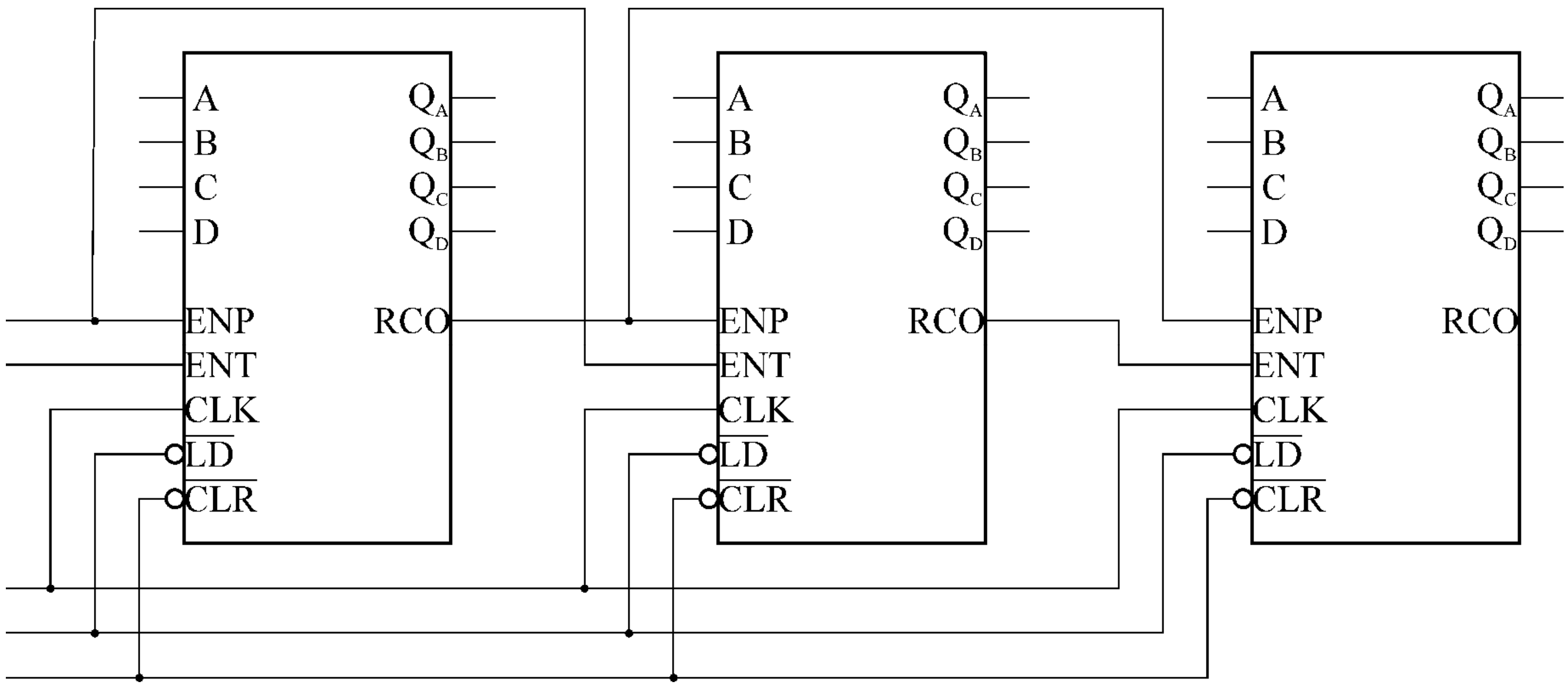
Counters

- Synchronous counters
  - Unidirectional counters – 16x family
    - Ripple mode carry circuit



Counters

- Synchronous counters
  - Unidirectional counters – 16x family
    - Carry look-ahead circuit



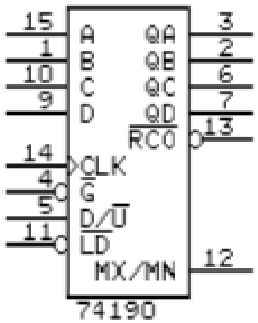
Counters

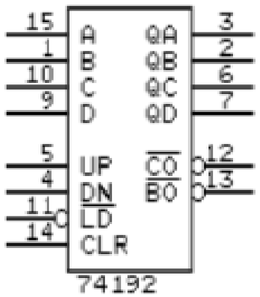
- Synchronous counters
  - Unidirectional counters – 16x family applications
    - Mod *N* counter, counter from 0 to *N*-1
      - Synchronous or asynchronous clear
    - Counter from A to max (9 or 15)
      - Synchronous load of A
    - Counter from A to B

Counters

- Synchronous counters
  - Bidirectional counters – 19x family

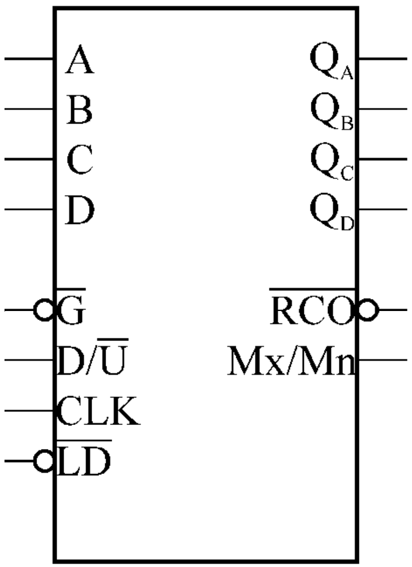
Circuit	Counter	Direction	Load	Clear
74190	Decimal	Direction selection input	Asynchronous	*None*
74191	Binary		Asynchronous	*None*
74192	Decimal	Separate up/down inputs	Asynchronous	Asynchronous
74193	Binary		Asynchronous	Asynchronous

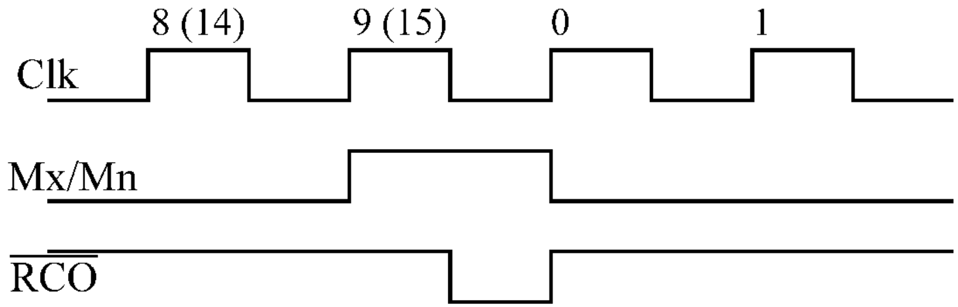


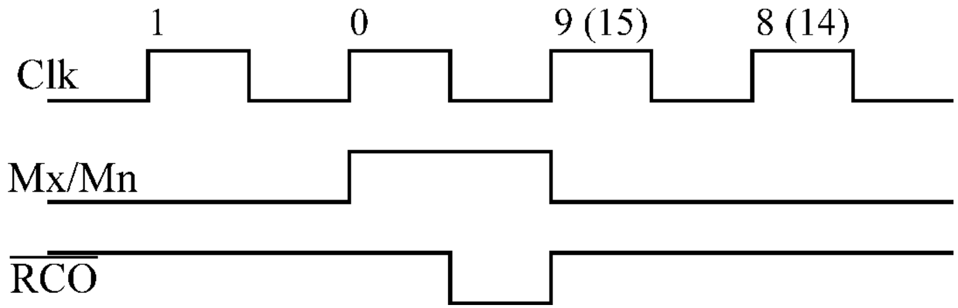


Counters

- Synchronous counters
  - Bidirectional counters – 190, 191

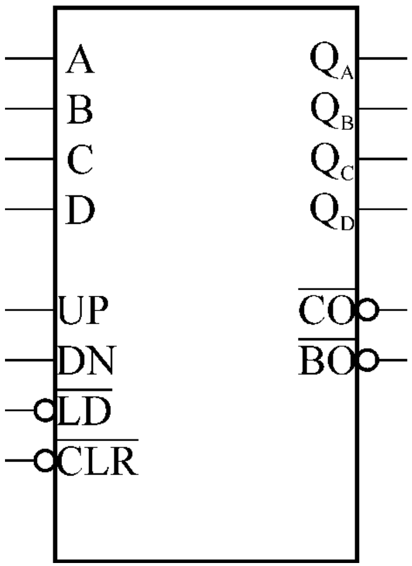


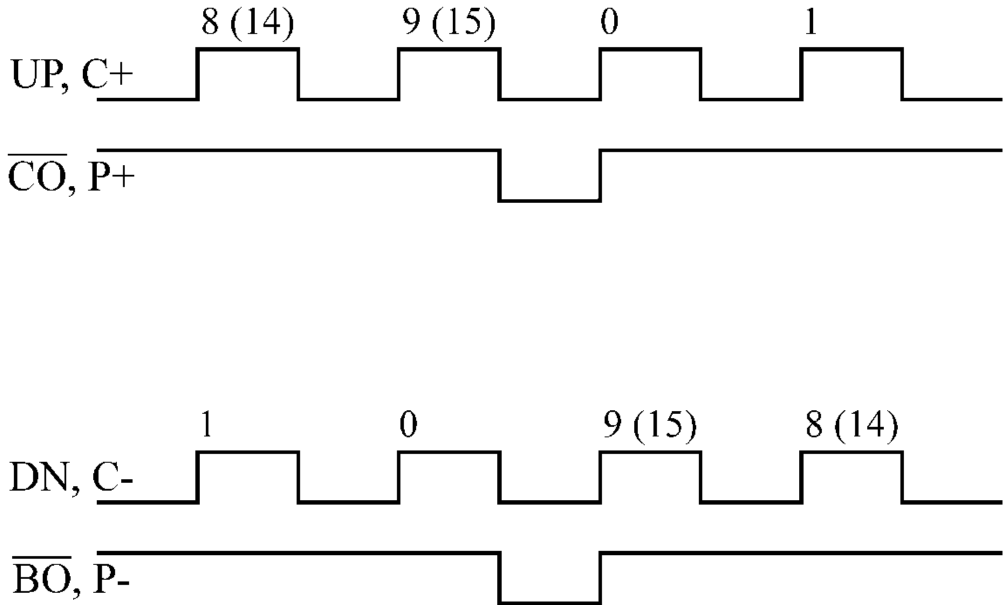




Counters

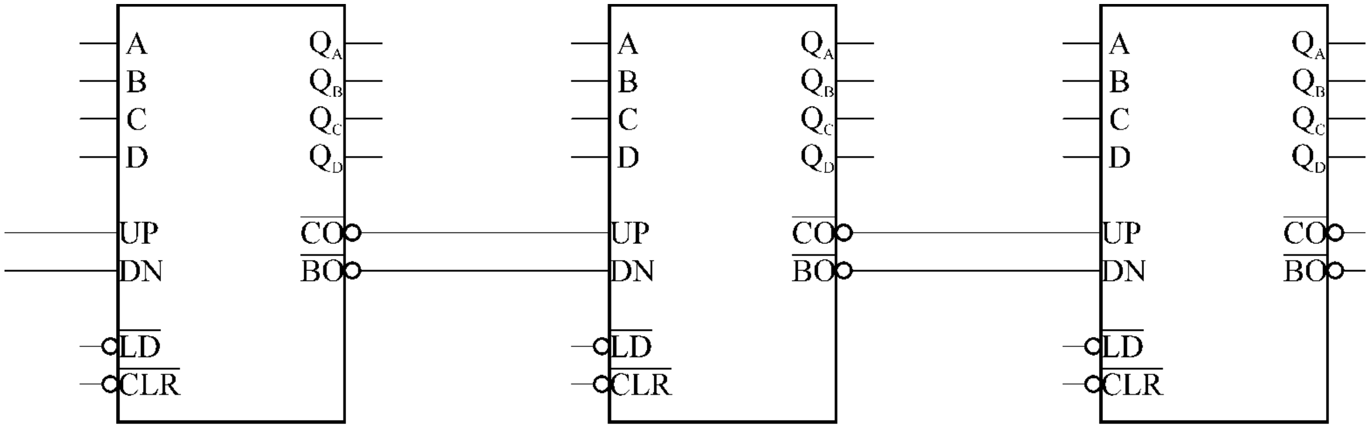
- Synchronous counters
  - Bidirectional counters – 192, 193

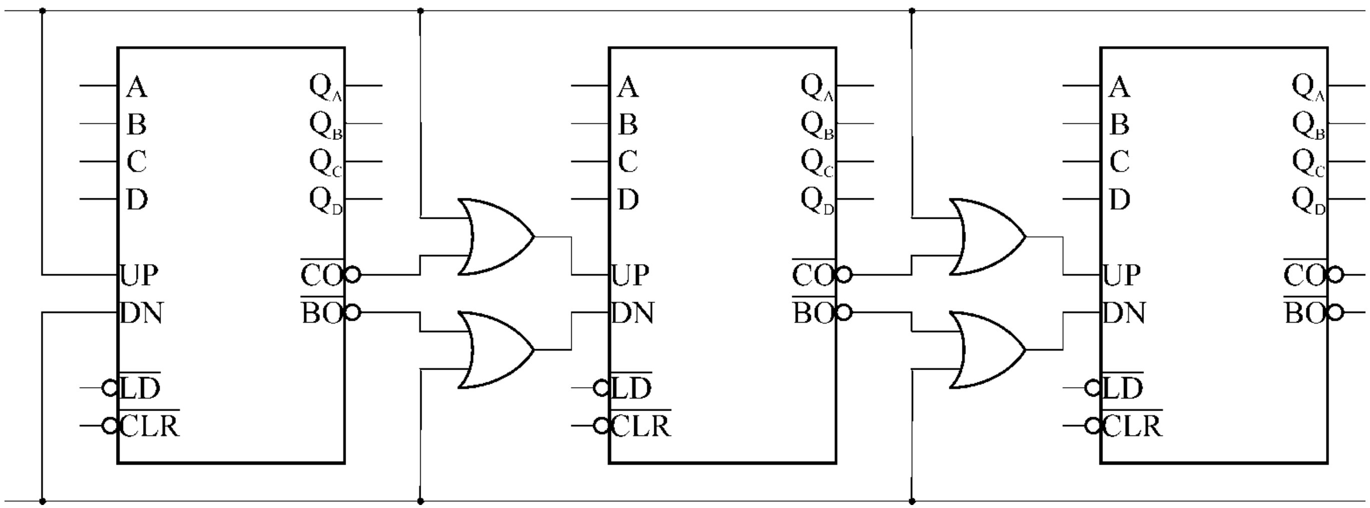




Counters

- Synchronous counters
  - Bidirectional counters – 192, 193

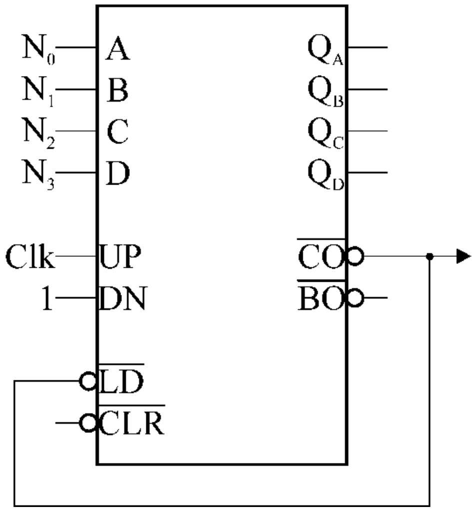




Counters

- Synchronous counters
  - Bidirectional counters – applications
    - Programmable frequency divider

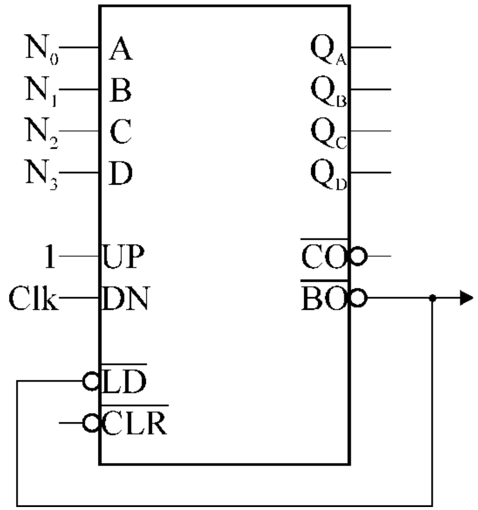
N→max



$$f_{bin} = \frac{f_{Clk}}{16 - N}$$

$$f_{dec} = \frac{f_{Clk}}{10 - N}$$

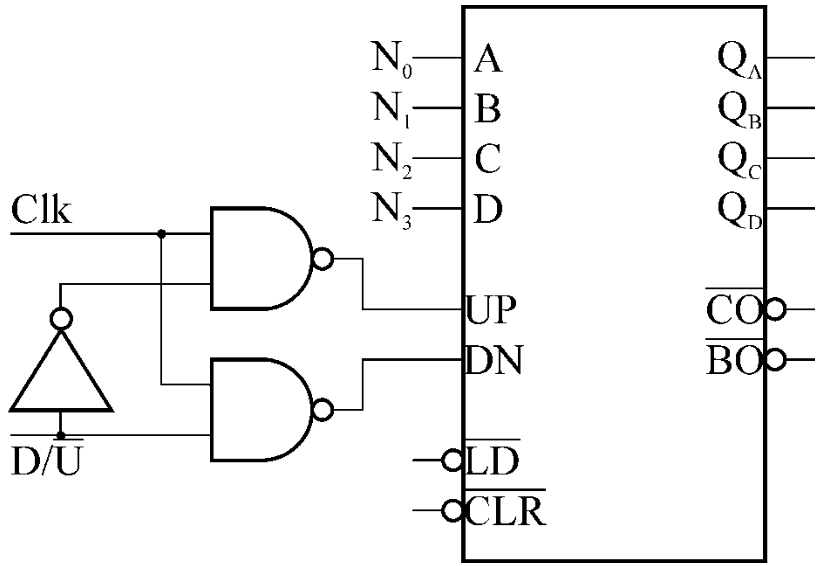
N→0



$$f = \frac{f_{Clk}}{N}$$

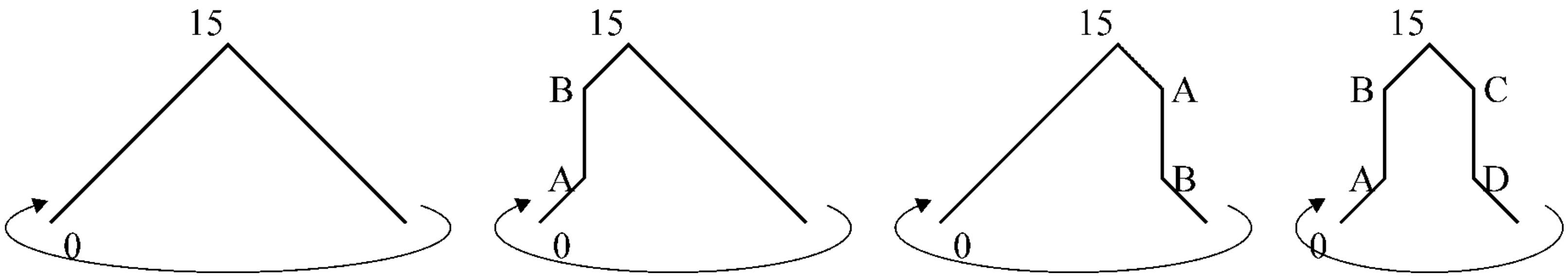
Counters

- Synchronous counters
  - Bidirectional counters – applications
    - Separate → common clock conversion



Counters

- Synchronous counters
  - Bidirectional counters – applications
    - 0, 1, …, 14, 15, 14, … 1, 0, 1, … etc. counter
    - As above, but with A→B jump
      - During count up
      - During count down
      - In both directions



    - To count how many people there are in a room/shop
      - *„COVID counter”*

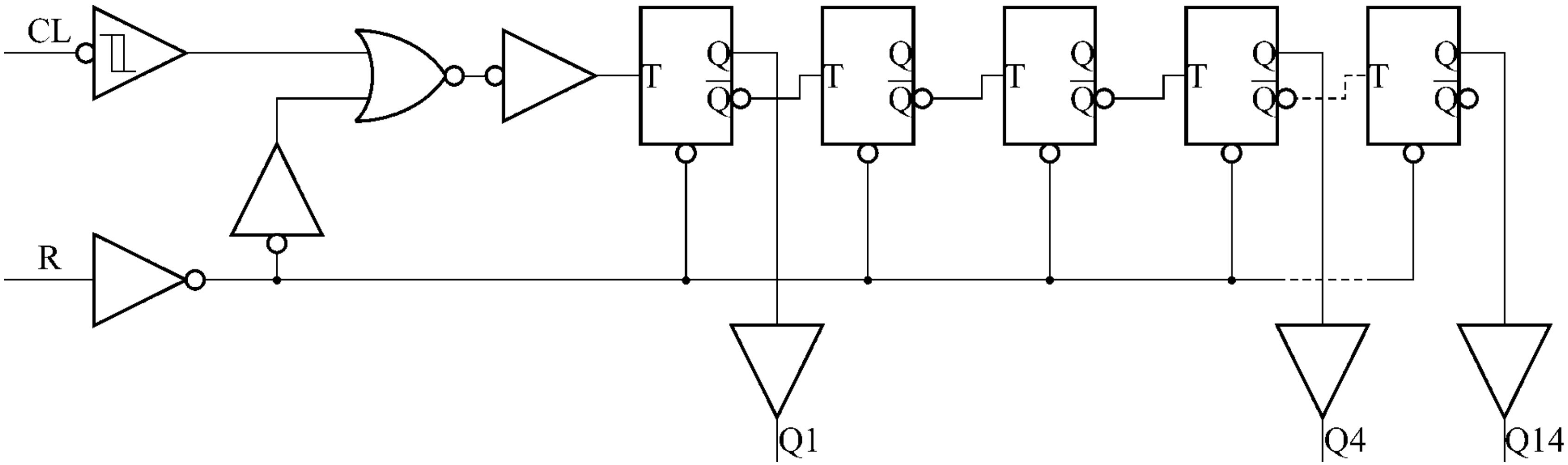
Counters

- CMOS frequency generators with dividers
  - 4024: 7-stage counter
  - 4040: 12-stage counter
  - 4020: 14-stage counter
  - 4521: 24-stage counter
  - 4060: 14-stage counter with oscillator

Part	Pins	Outputs																							
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
4020	16	+			+	+	+	+	+	+	+	+	+	+	+										
4024	14	+	+	+	+	+	+	+																	
4040	16	+	+	+	+	+	+	+	+	+	+	+	+												
4521	16																		+	+	+	+	+	+	+
4060	16				+	+	+	+	+	+	+	+	+	+	+										

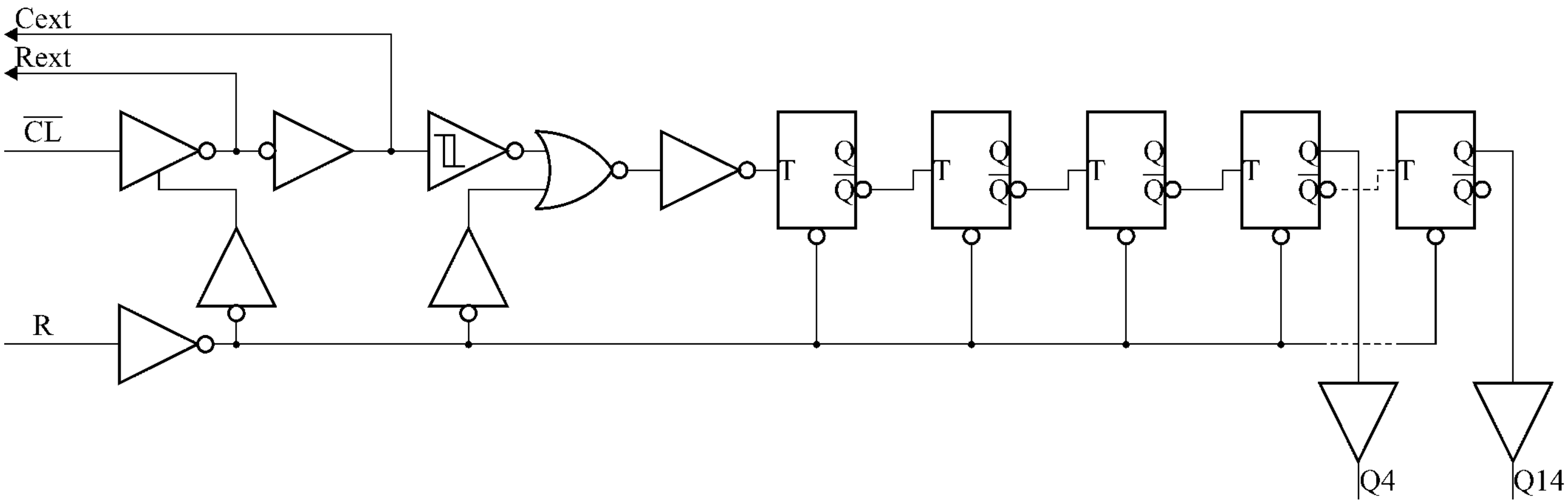
Counters

- CMOS frequency generators with dividers
  - 4020



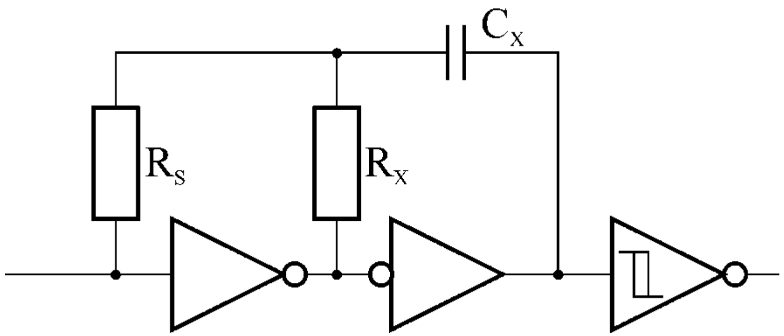
Counters

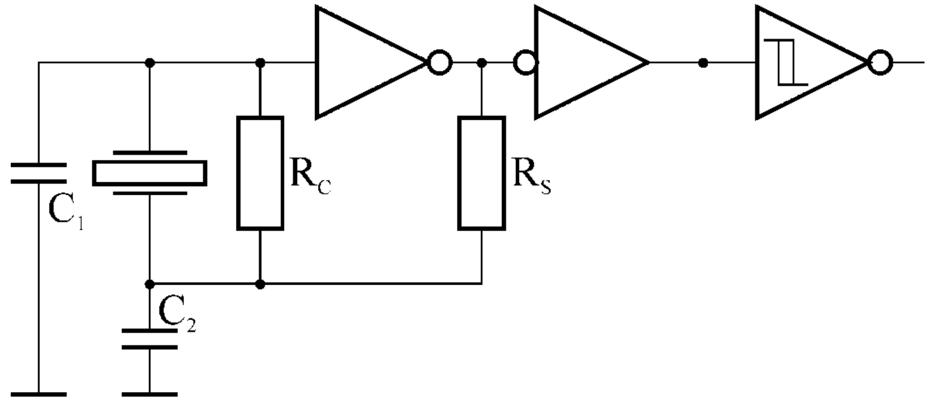
- CMOS frequency generators with dividers
  - 4060
    - Built-in oscillator
    - Falling-edge active
    - Available outputs: Q4÷Q10, Q12÷Q14



Counters

- CMOS frequency generators with dividers
  - 4060
    - RC or crystal circuits





$$T = 2.2 R_X C_X$$
$$R_S = (2 \div 10) \cdot R_X$$