



Fundusze Europejskie
Wiedza Edukacja Rozwój



**Rzeczpospolita
Polska**

Unia Europejska
Europejski Fundusz Społeczny



**Politechnika Śląska jako Centrum Nowoczesnego Kształcenia
opartego o badania i innowacje**

POWR.03.05.00-IP.08-00-PZ1/17

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Digital Circuits Design

**Faculty of Automatic Control, Electronics and Computer Science,
Informatics, Bachelor Degree**

Lecture 5

Registers

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Registers

Program:

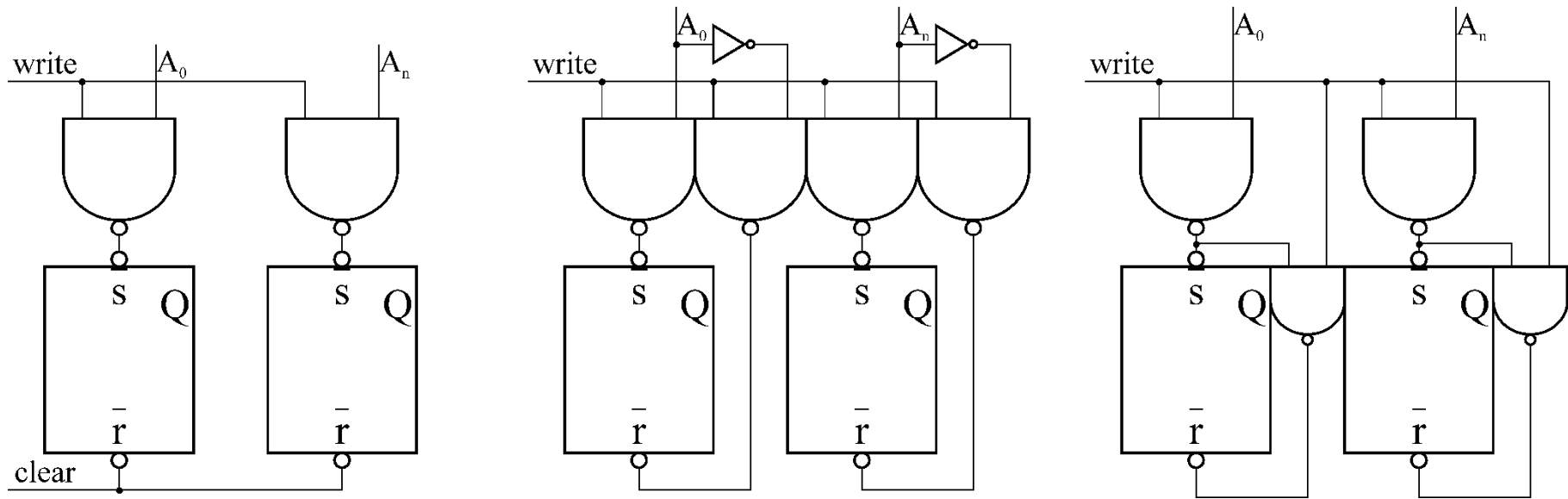
- Register types
- Input circuits
- Output circuits
- Shift registers
- Applications
- Serial \leftrightarrow parallel conversion

Registers

- Register types (classification)
 - According to data input/output
 - PIPO, PISO, SIPO, SISO
 - Serial (incl. PIPO)
 - In/out bit by bit
 - Bidirectional/unidirectional (left/right/any)
 - Parallel (PIPO)
 - In/out all bits at the same time
 - Edge-triggered/level-triggered (latch)
 - Syn/asyn load

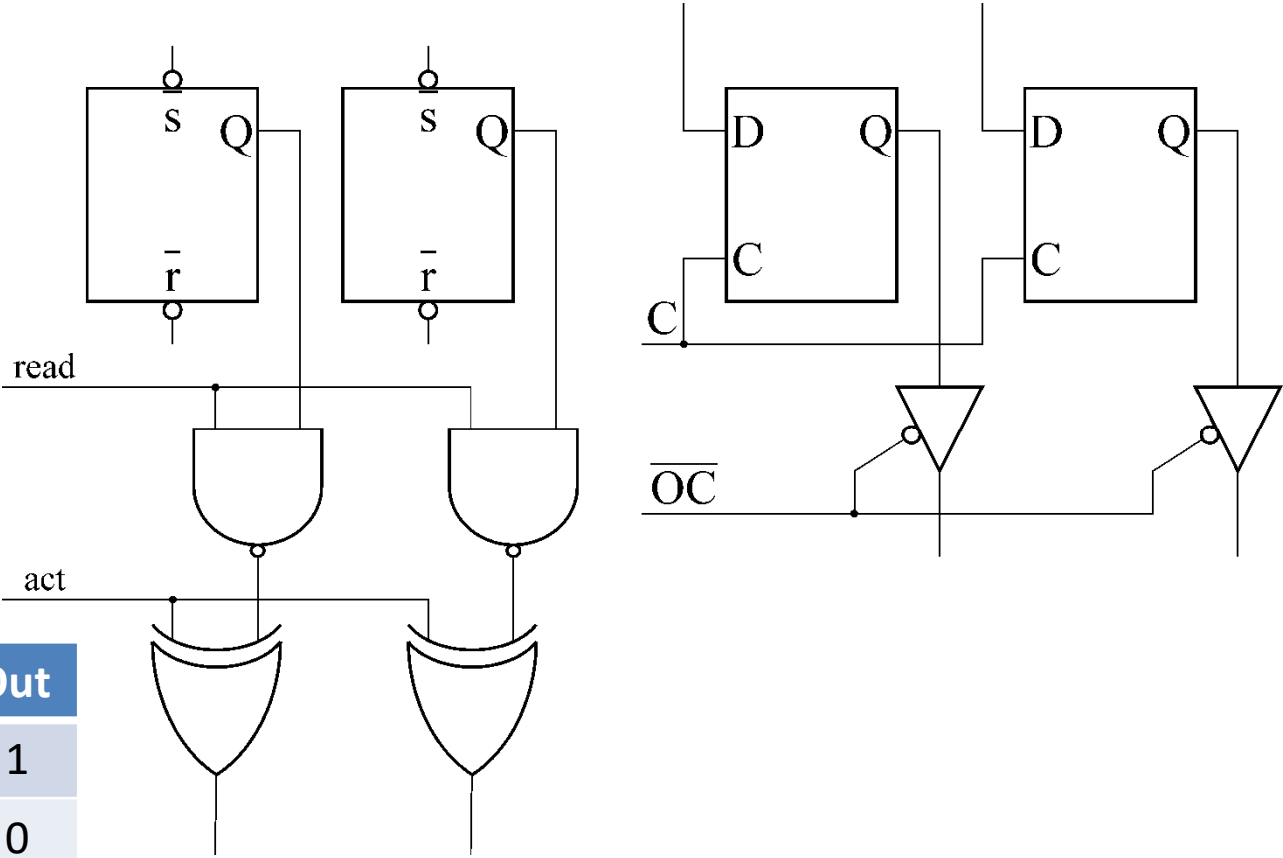
Registers

- Parallel data input circuits



Registers

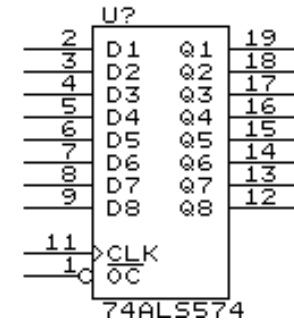
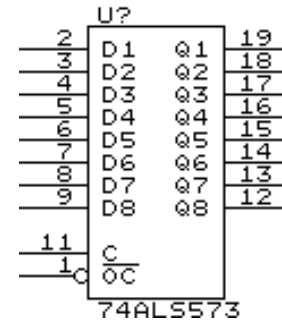
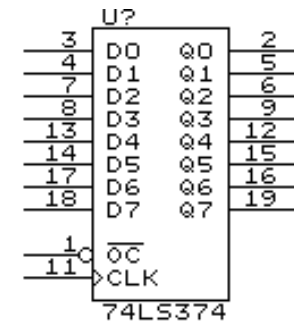
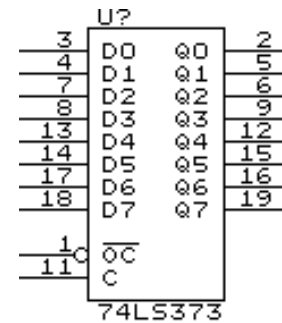
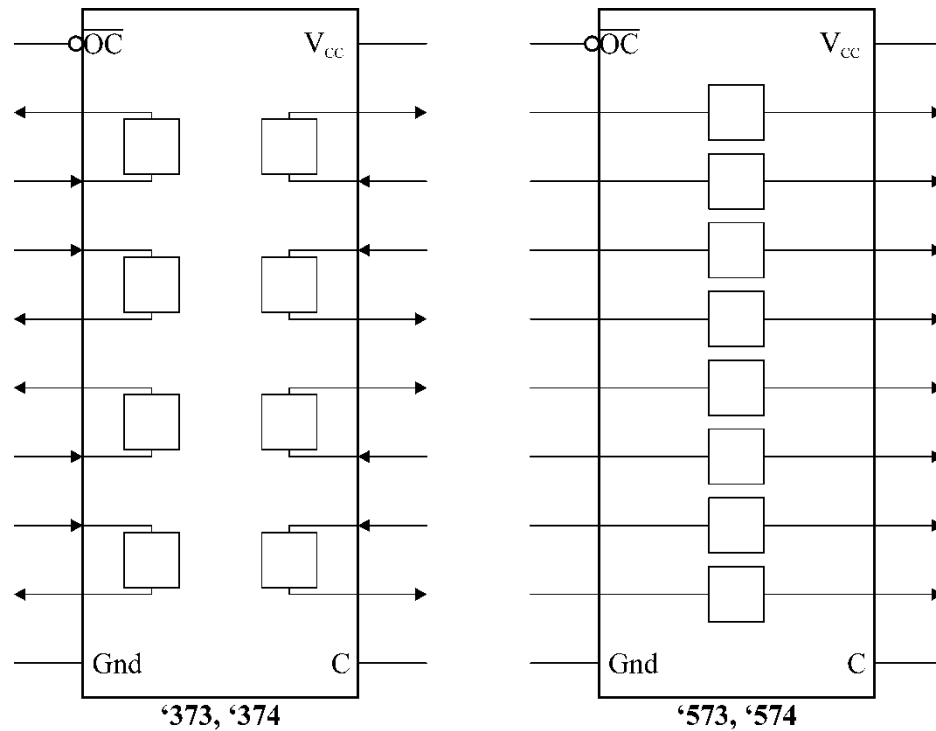
- Parallel data output circuits



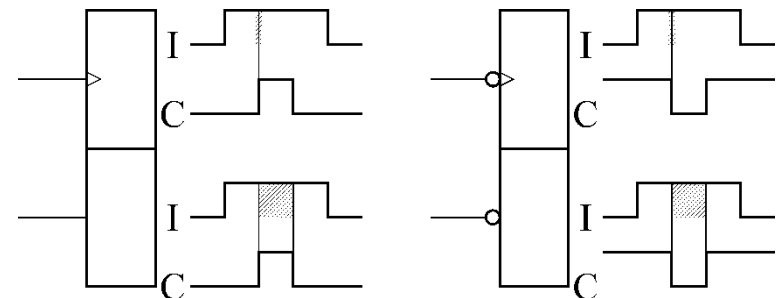
Rd	Act	Out
0	0	1
0	1	0
1	0	\bar{Q}
1	1	Q

Registers

- Example PIPO registers

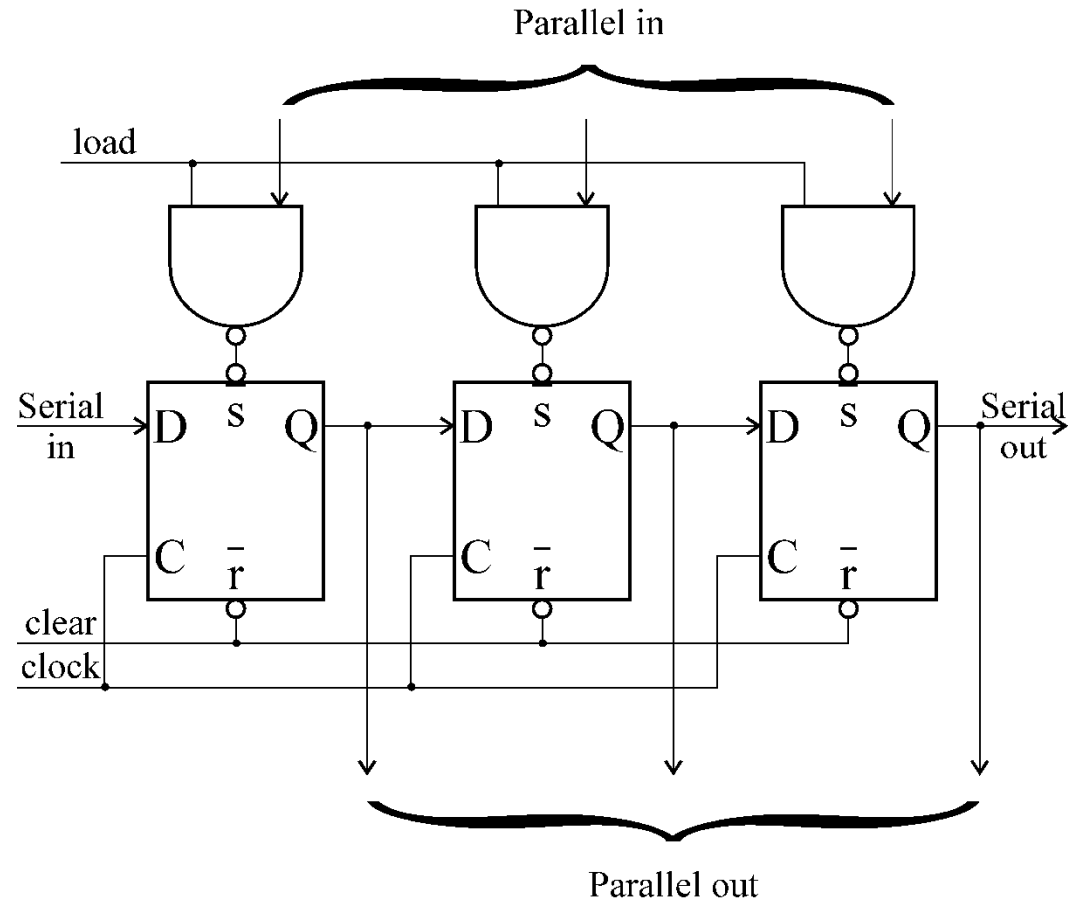


Write	I/O together	I/O opposite
Level-triggered	'373	'573
Edge-triggered	'374	'574



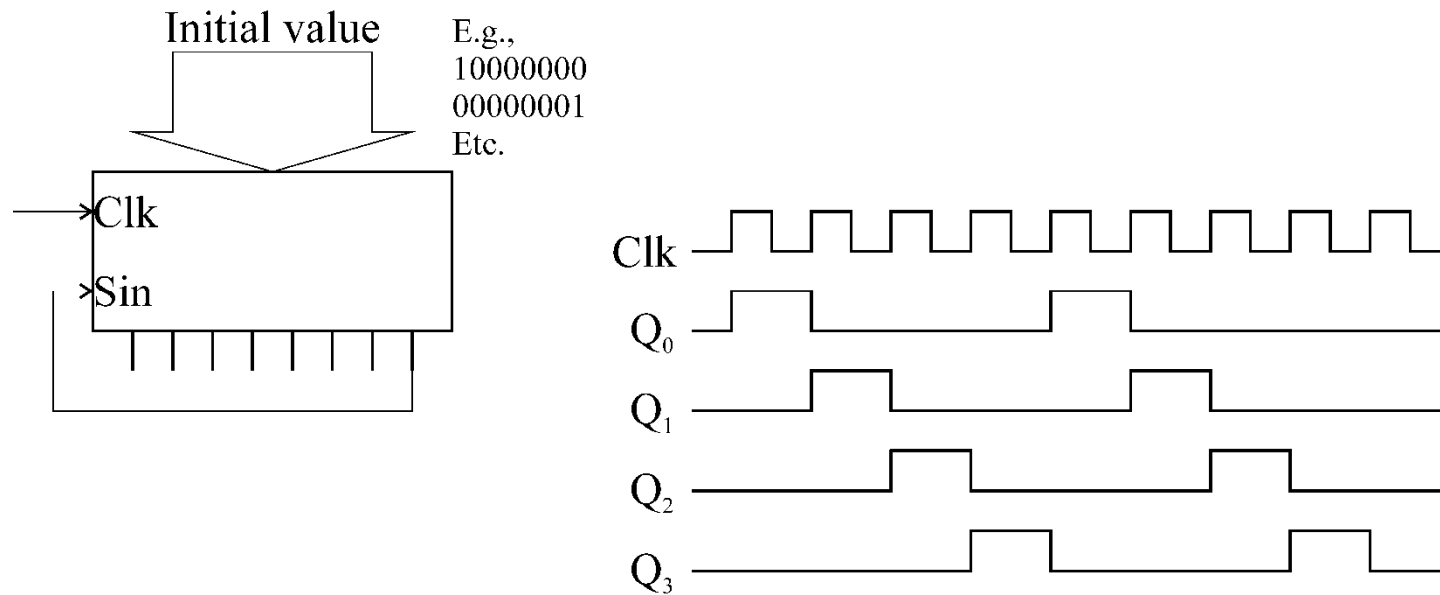
Registers

- Parallel/serial register



Registers

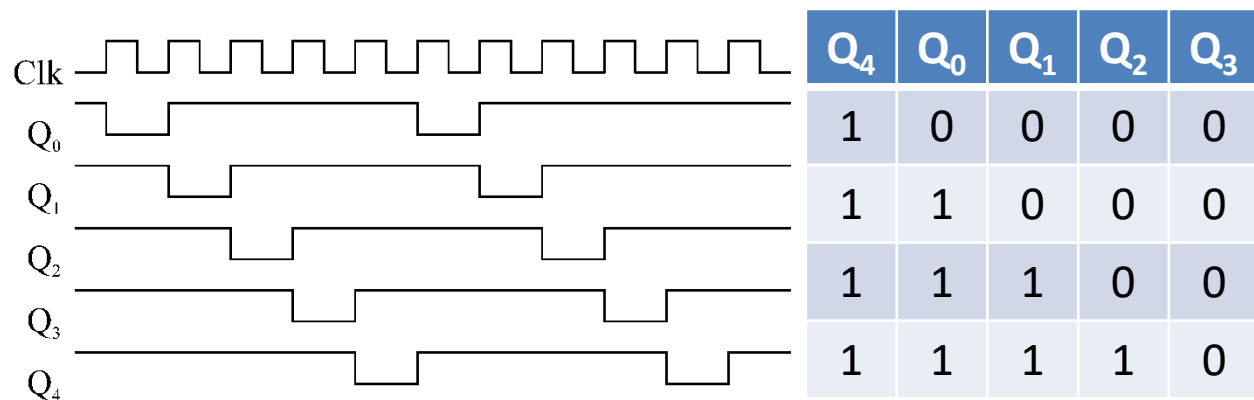
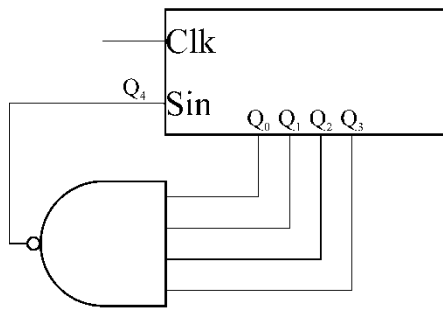
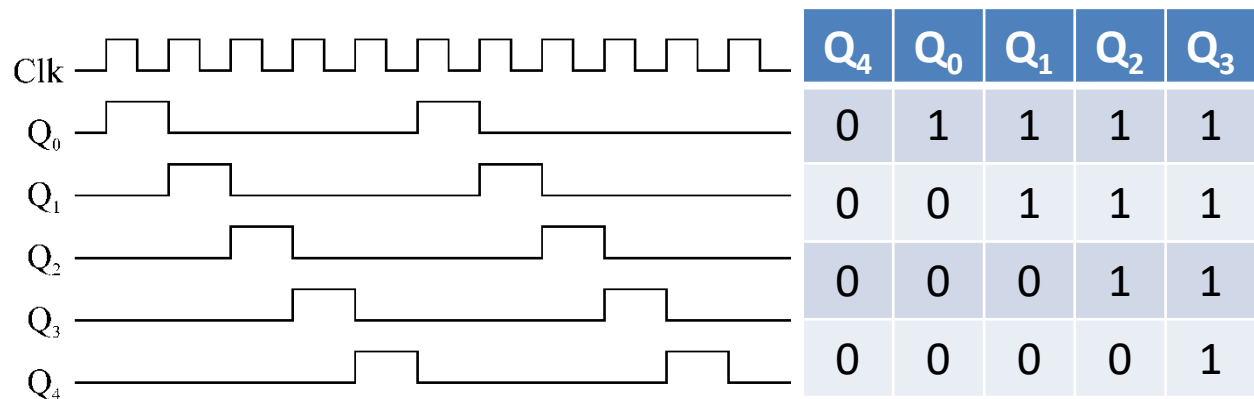
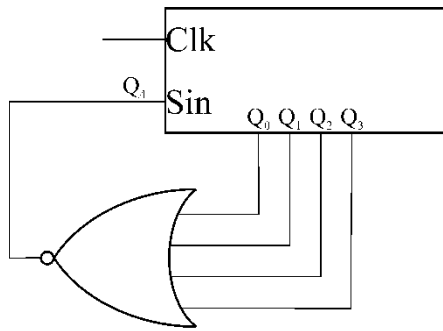
- Register applications
 - Ring register – shift register with feedback
 - single outlined state → no decoding necessary („rotating 1”, „rotating 0”)
 - Frequency dividers, signal distributors etc.



Registers

– Ring registers with error state autocorrection

- No initial value needed
- N bits \rightarrow N+1 states



Rejstry

– Pseudoring Johnson counters with autocorrection

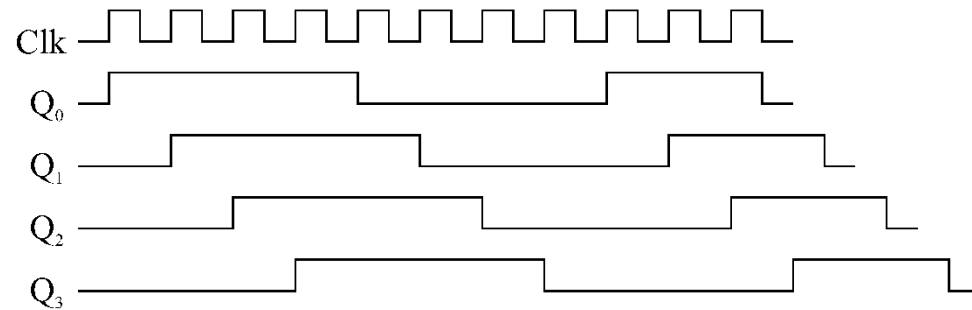
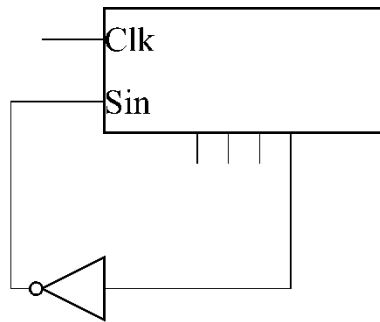
- Johnson code

Value	Johnson code
0	00000
1	00001
2	00011
3	00111
4	01111
5	11111
6	11110
7	11100
8	11000
9	10000

Registers

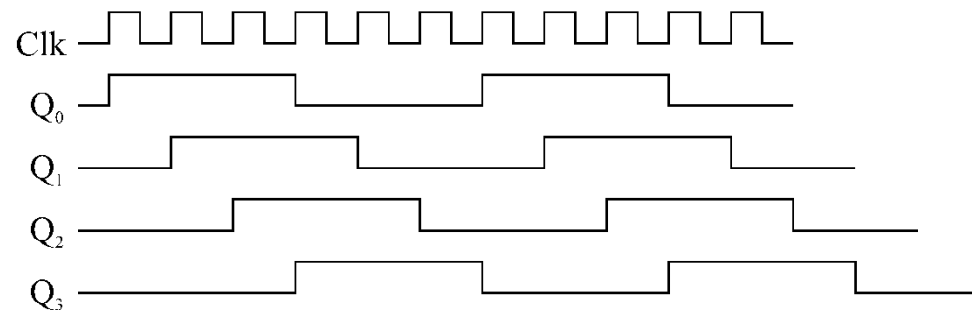
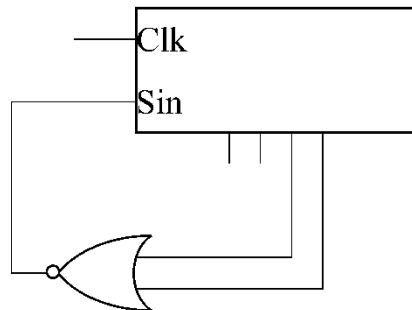
– Pseudoring Johnson counters with autocorrection

- N bits \rightarrow 2N states



- Johnson counter with shortened cycle

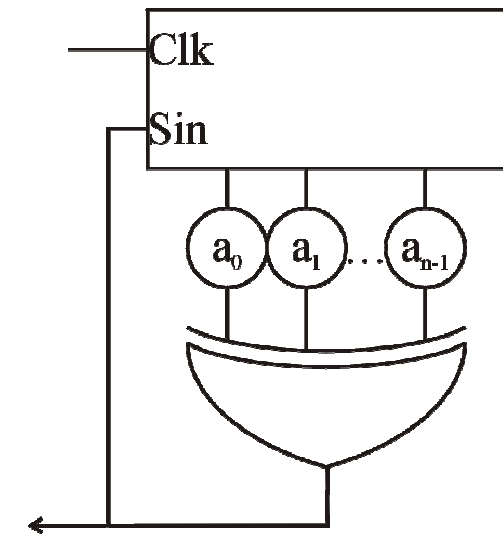
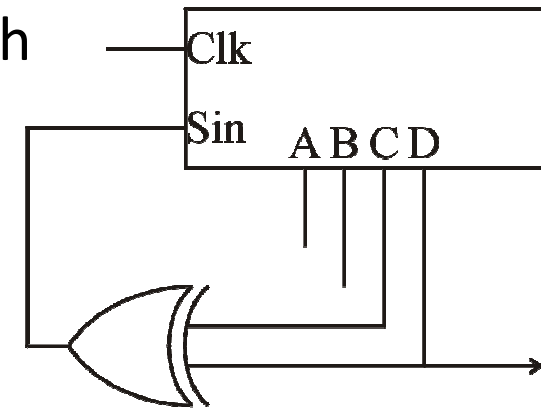
– (less than 2N states)



Registers

– Linear registers

- Shift registers with feedback through the XOR gate
- N bits $\rightarrow 2^N - 1$ states
- E.g.,
 - $N=3 \rightarrow B, C$
 - $N=4 \rightarrow C, D$
 - $N=5 \rightarrow C, E$
 - $N=6 \rightarrow E, F$
 - $N=7 \rightarrow F, G$
 - $N=8 \rightarrow D, E, F, H$
 - $N=9 \rightarrow E, I$
 - $N=10 \rightarrow G, J$
 - $N=11 \rightarrow I, K$
 - $N=12 \rightarrow F, H, K, L$



Registers

– Linear registers

- Cycle: $2^N - 1$ states
- Each state occurs exactly once, except the forbidden state
- Number of 1's: 2^{N-1} , 0's: $2^{N-2} - 1$
- Sequence of 1's and 0's – pseudorandom with distribution close to the binomial distribution

– *How to avoid the forbidden state?*

- Decode and force any other state
- Modify the feedback function

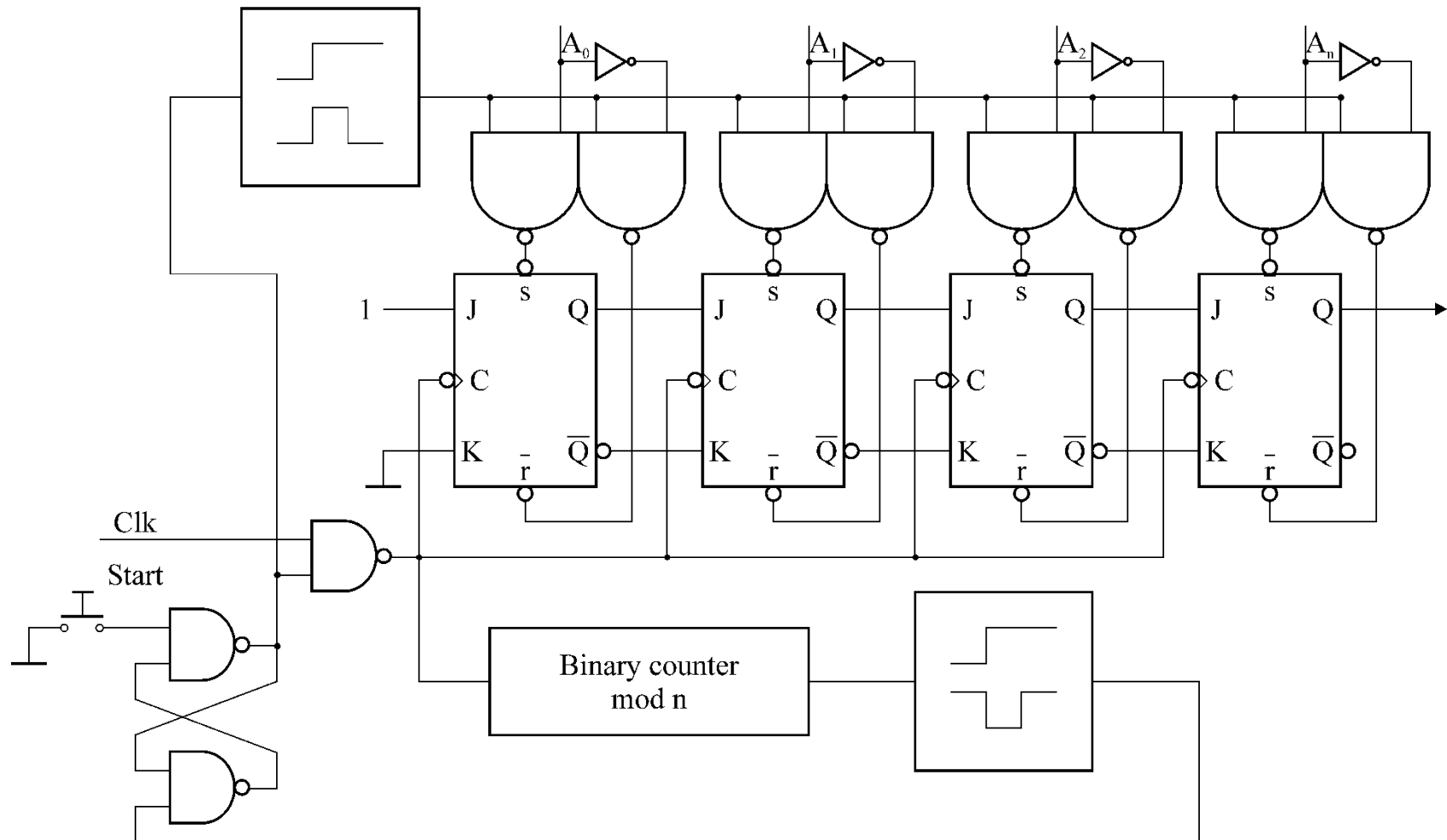
Registers

– Linear registers – applications

- Frequency dividers
- DAC converters
- ADC converters
- Testing circuits
- Data storage circuits
 - CRC (*Cyclic Redundancy Check*)
- Data transmission circuits
 - CRC
 - Spread Spectrum – wireless networks
 - » WLANs – 802.11, 802.11b (Wi-Fi)
 - » WPANs – 802.15.1 (Bluetooth), 802.15.4

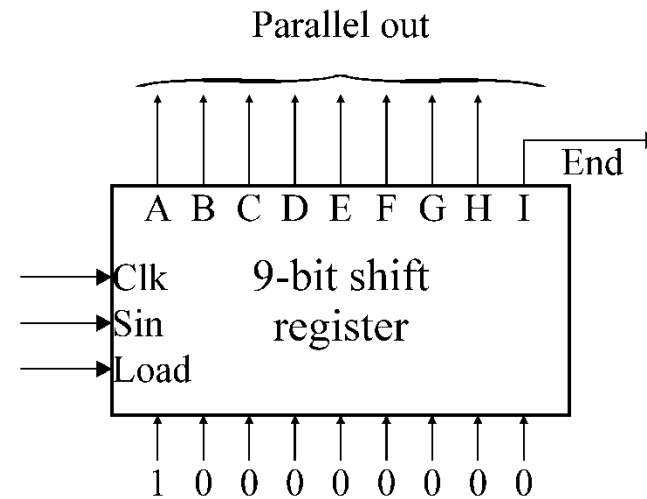
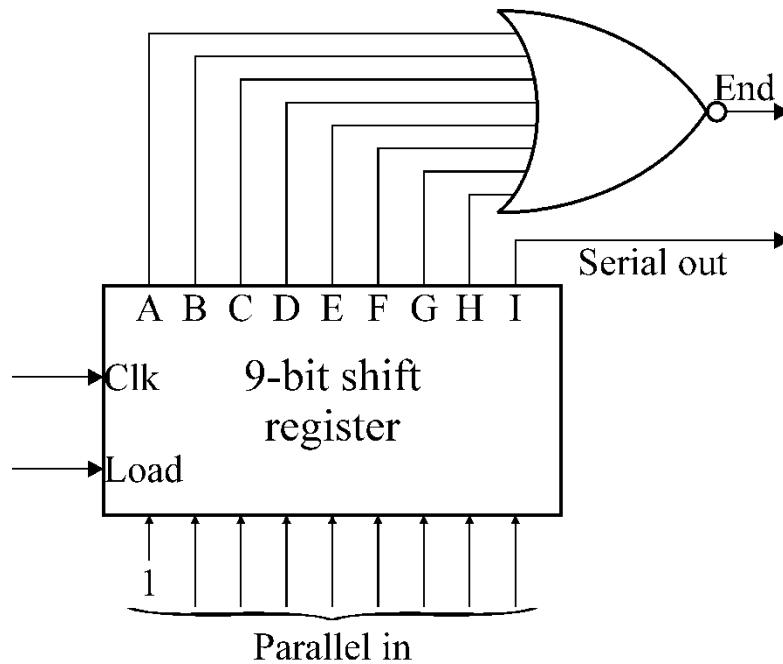
Registers

- Register applications
 - Parallel \rightarrow serial conversion



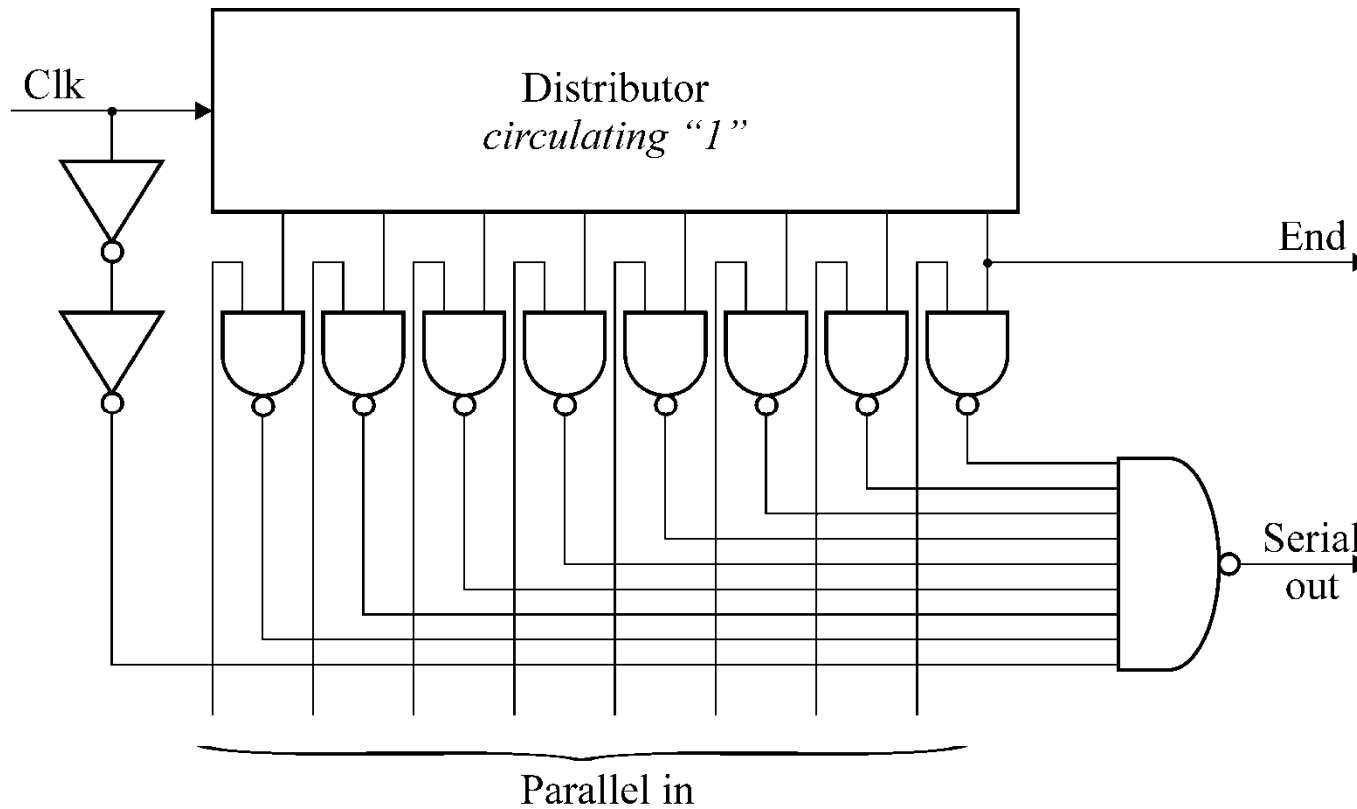
Registers

- Register applications
 - Parallel → serial conversion



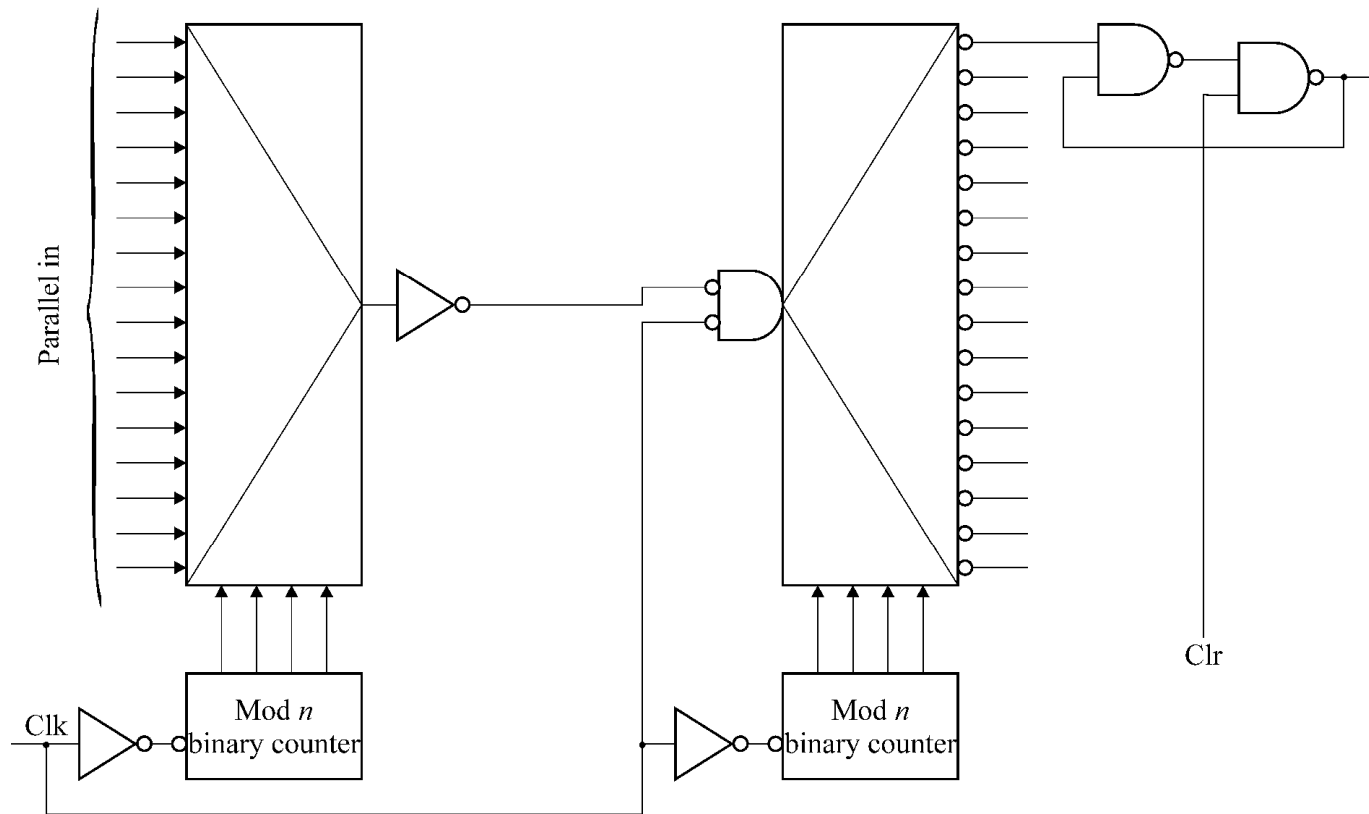
Registers

- Register applications
 - Parallel → serial conversion



Registers

- Parallel → serial conversion using mux/dmux
 - Distance \leq few tens of cm



Registers

- Parallel → serial conversion using mux/dmux
 - With parity control bit

