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Wiedza Edukacja Rozwój

Rzeczpospolita Polska

Unia Europejska
Europejski Fundusz Społeczny

Politechnika Śląska jako Centrum Nowoczesnego Kształcenia
opartego o badania i innowacje

POWR.03.05.00-IP.08-00-PZ1/17

Projekt współfinansowany przez Unię Europejską ze środków Europejskiego Funduszu Społecznego

Digital Circuits Design

Faculty of Automatic Control, Electronics and Computer Science, Informatics, Bachelor Degree

Lecture 3

Time dependencies circuits – part 1

Bartłomiej Zieliński, PhD, DSc

Time circuits – part 1

Program:

(today)

- 7412x circuit family
- Properties, applications

(next week)

- 555 circuit
- …..

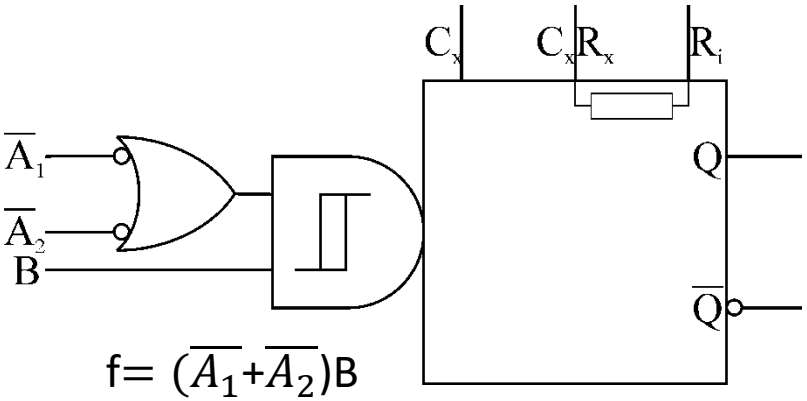
Time circuits – part 1

- Pulse generators
  - Univibrator, monostable flip-flop, monostable multivibrator
  - Upon trigger, generate output pulse of a given duration time

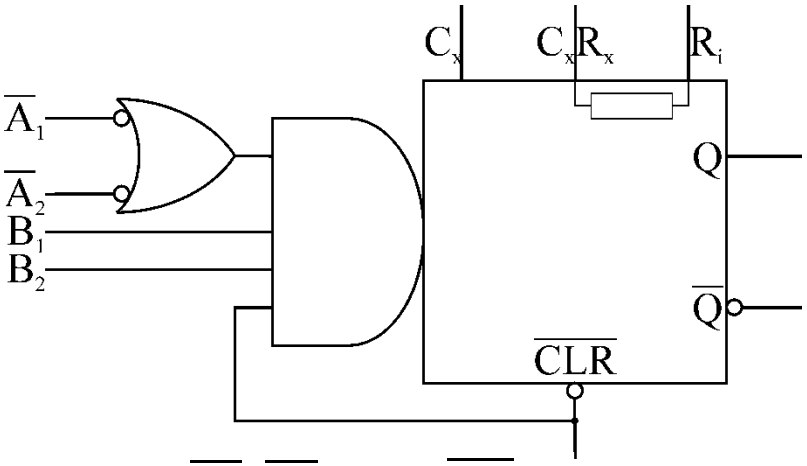
- Time duration
  - Few tens ns … few tens s
  - There are also trigger (differential) circuits – up to 10 ns pulse length
  - Very long pulses (minutes, hours long) – counters, frequency dividers, etc.

Time circuits – part 1

- 74121, 74122, 74123

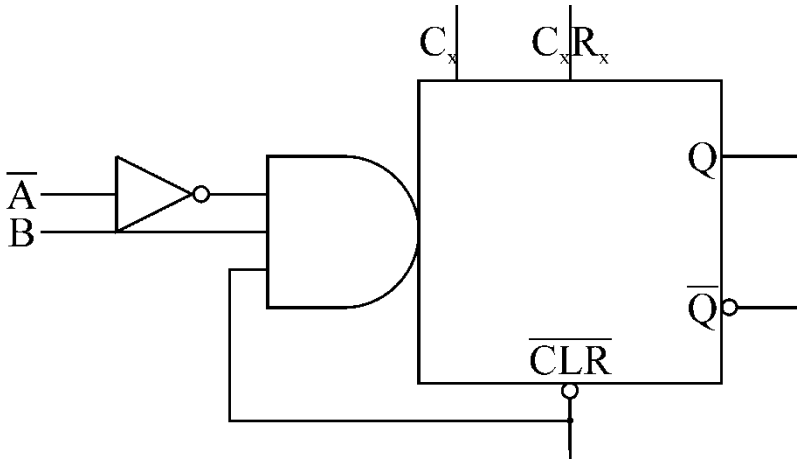


f= $(\overline{A_1}+\overline{A_2})$B



f= $(\overline{A_1}+\overline{A_2})\ B_1B_2\overline{Clr}$

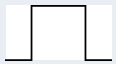
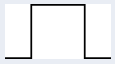
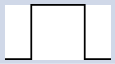
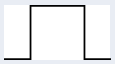
- 74121 – B = Schmitt input



f= $\bar{A}B\overline{Clr}$

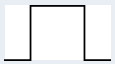
Time circuits – part 1

- 74121 – truth table

Inputs			Outputs	
$\overline{A_1}$	$\overline{A_2}$	B	Q	$\bar{Q}$
0	-	1	0	1
-	0	1	0	1
-	-	0	0	1
1	1	-	0	1
1	1→0	1		
1→0	1	1		
1→0	1→0	1		
0	-	0→1		
-	0	0→1		

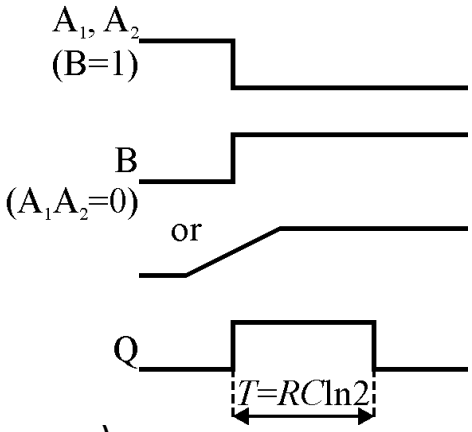
Time circuits – part 1

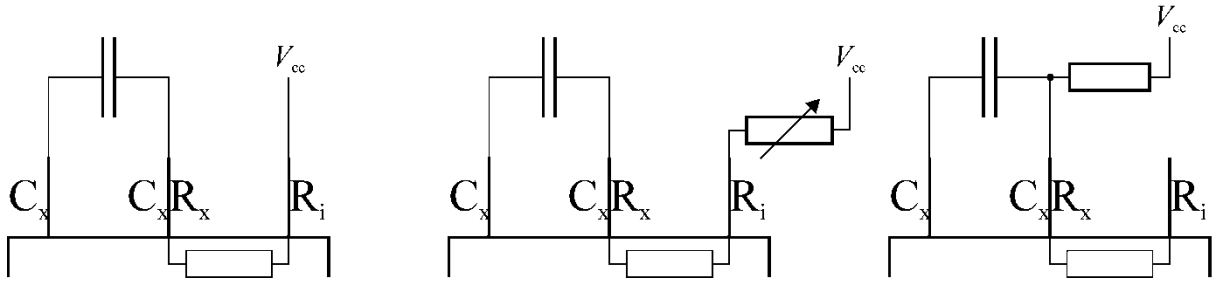
- 74123 – truth table

Inputs			Outputs	
$\overline{Clr}$	$\bar{A}$	B	Q	$\bar{Q}$
0	-	-	0	1
-	1	-	0	1
-	-	0	0	1
1	0	0→1		
1	1→0	1		
0→1	0	1		

Time circuits – part 1

- 74121 – non retrigerrable
  - A_1, A_2 – 1V/µs
  - B – 1V/s
  - T_p = abt. 40 ns
  - T = RCln2, C_i≈20 pF, R_i ≈2kΩ
  - C=10 pF…10 µF, R=2..30 kΩ
  - C up to 1000 µF, R down to 1.4 kΩ (less accuracy)

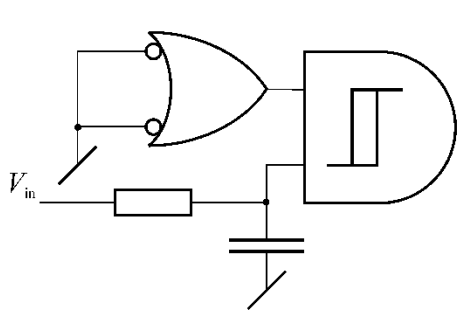


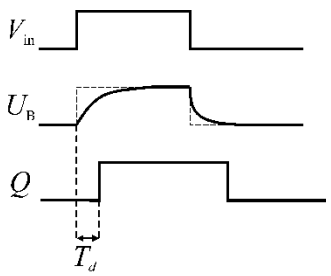


$T = CR_i \ln 2$

$T = C(R + R_i) \ln 2$

$T = CR \ln 2$



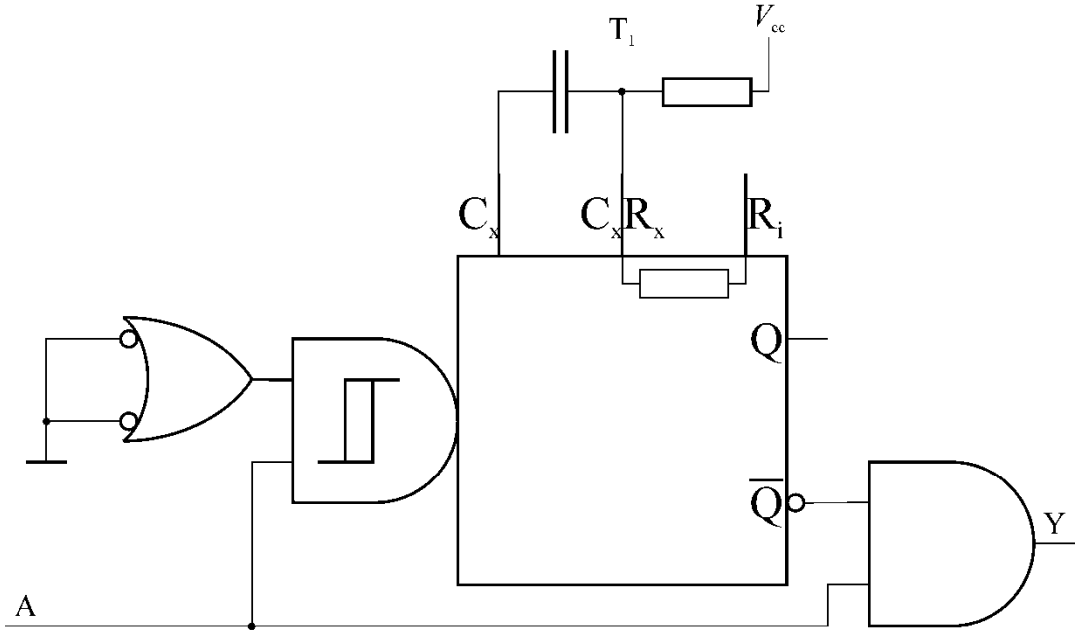


Rmax=400 Ω, for R=100 Ω:

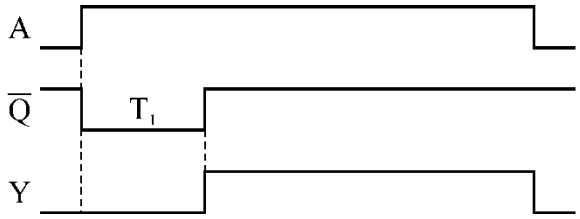
C=10 nF	T=1.36 µs
C=40 nF	T=4.9 µs
C=112 nF	T=12.4 µs

Time circuits – part 1

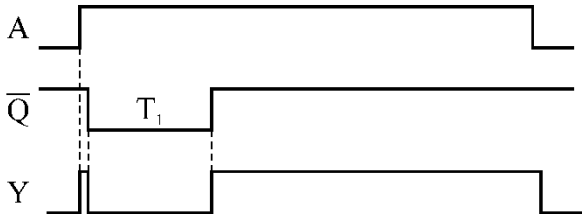
- 74121 – signal shortening circuit



idea

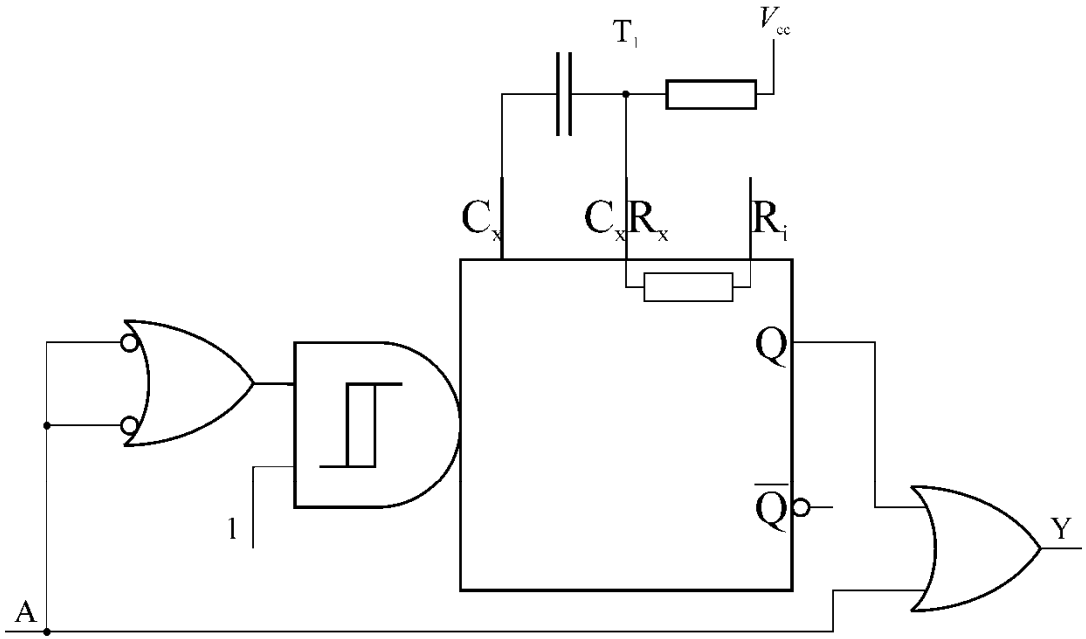


reality

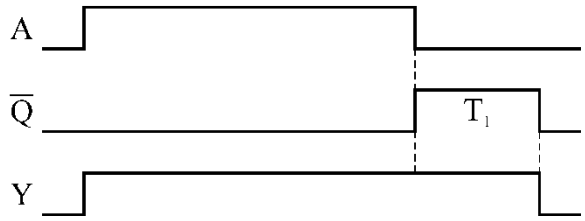


Time circuits – part 1

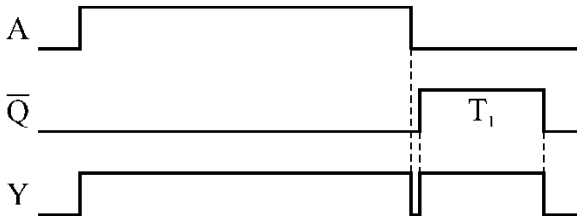
- 74121 – signal lenghtening circuit



idea

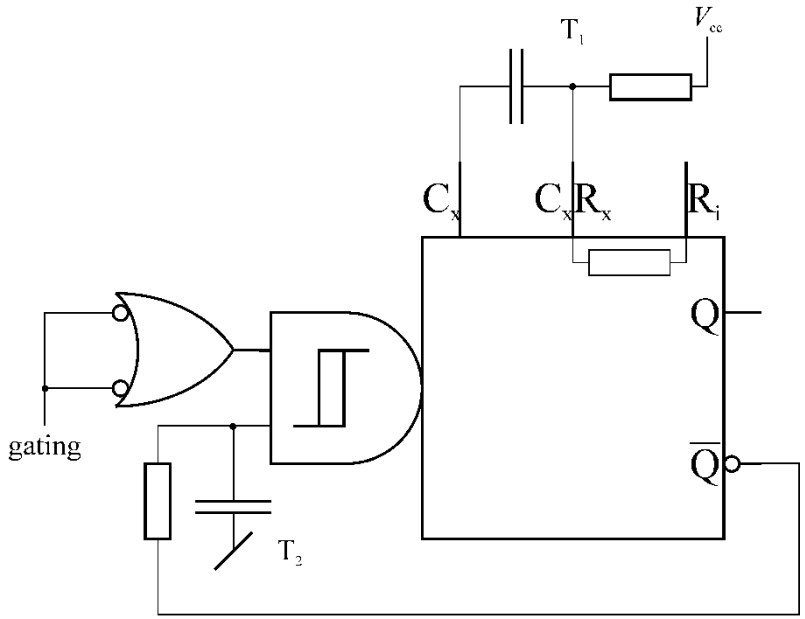


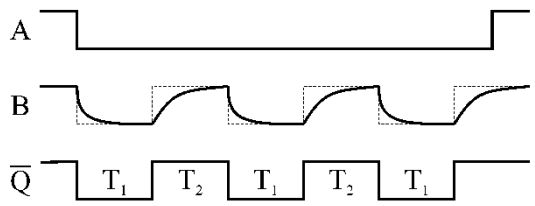
reality



Time circuits – part 1

- Single 74121 as a frequency generator



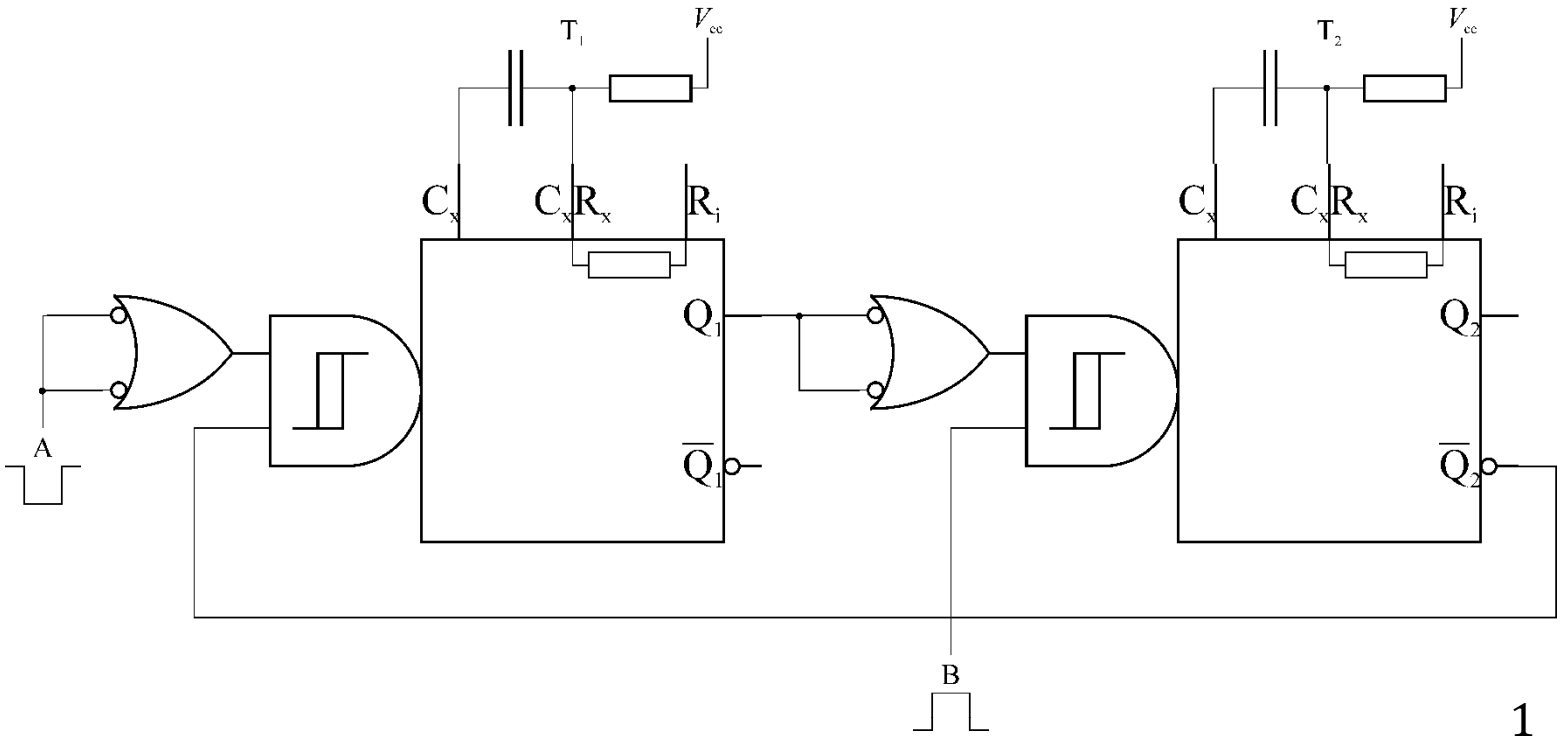


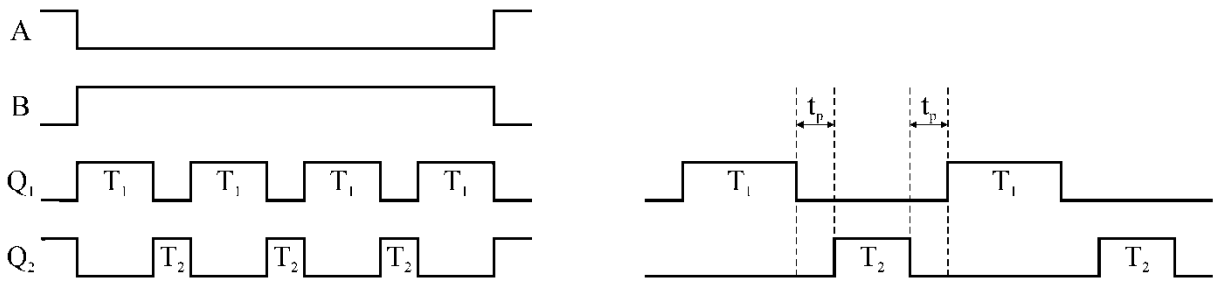
$$f = \frac{1}{T_1 + T_2 + t_p}$$

$$\eta = \frac{T_1}{T_1 + T_2 + t_p}$$

Time circuits – part 1

- Multiple 74121's as a frequency generator



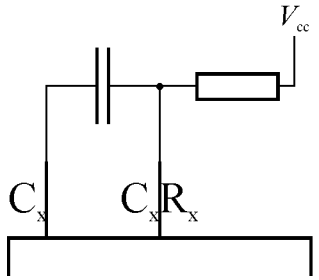


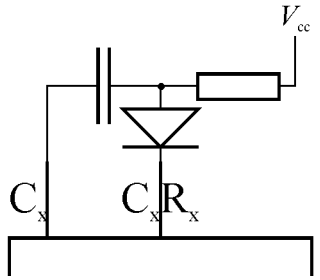
$$f = \frac{1}{T_1 + T_2 + 2t_p}$$

$$\eta = \frac{T_1}{T_1 + T_2 + 2t_p}$$

Time circuits – part 1

- 74122, 74123 – retrigerrable
  - C<1000 pF → diagrams



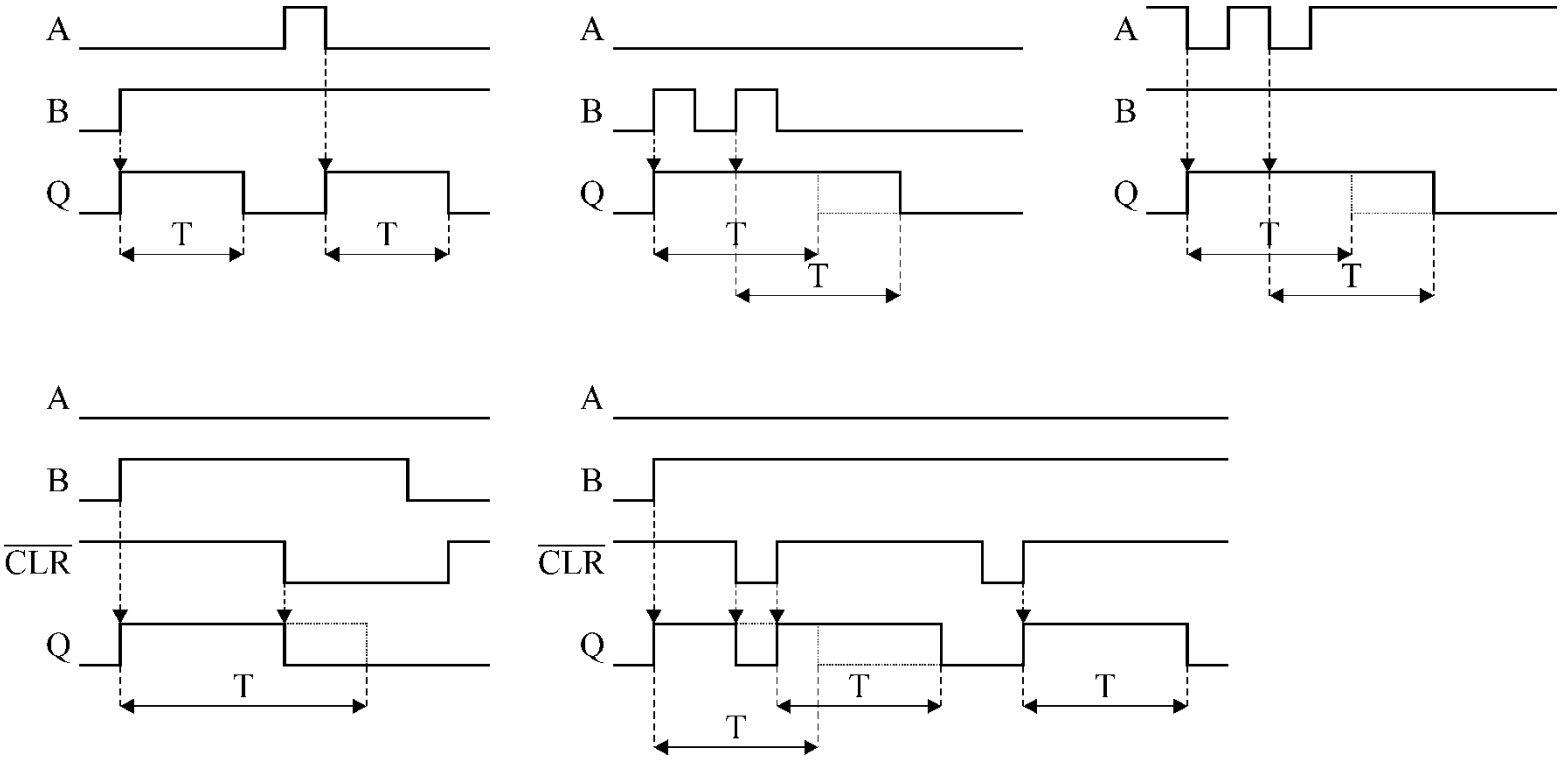


$$T = 0.32RC\left(1 + \frac{0.7}{R}\right) \approx 0.3RC \qquad T = 0.28RC\left(1 + \frac{0.7}{R}\right) \approx 0.27RC$$

- R [kΩ], C [pF], t [ns]!
- Min time between triggers: t[ns] = 0.22 C [pF]

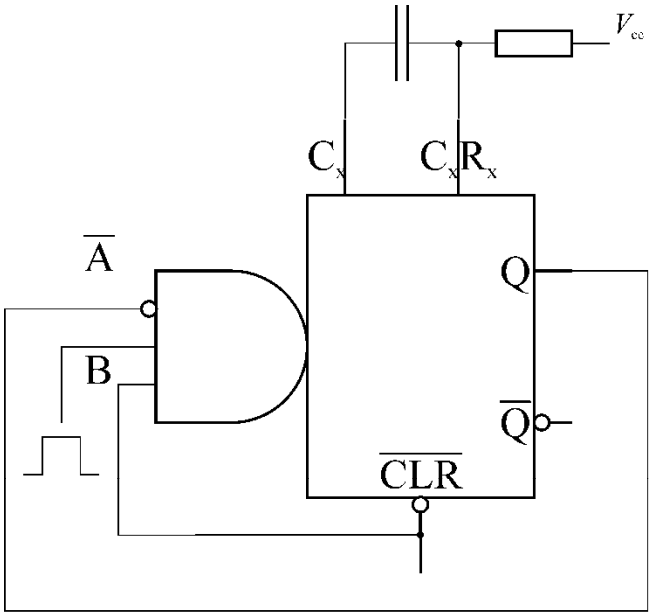
Time circuits – part 1

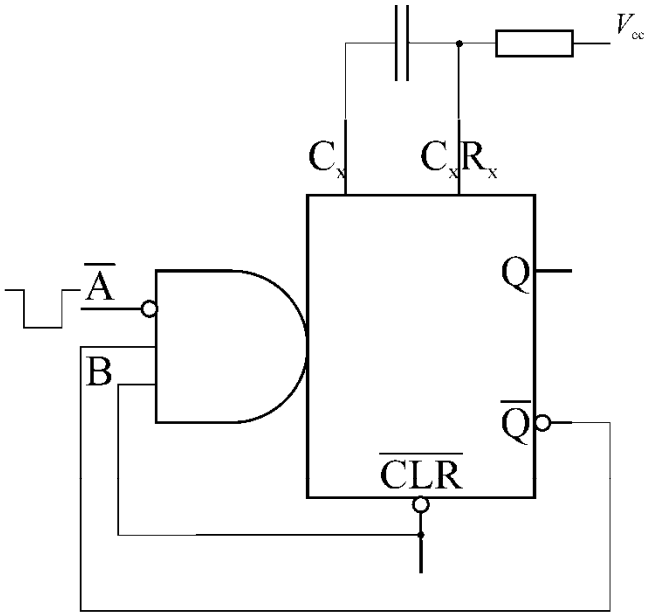
- How to trigger
  - What does „retriggerrable” mean?

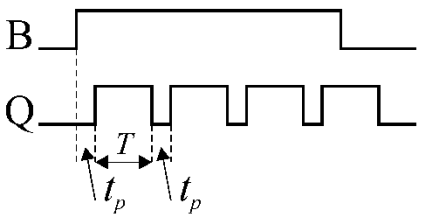


Time circuits – part 1

- 74123 as short pulse series generator

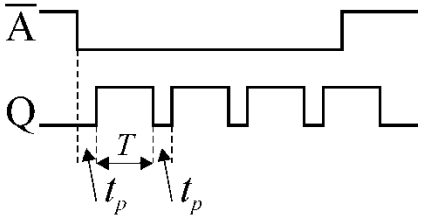






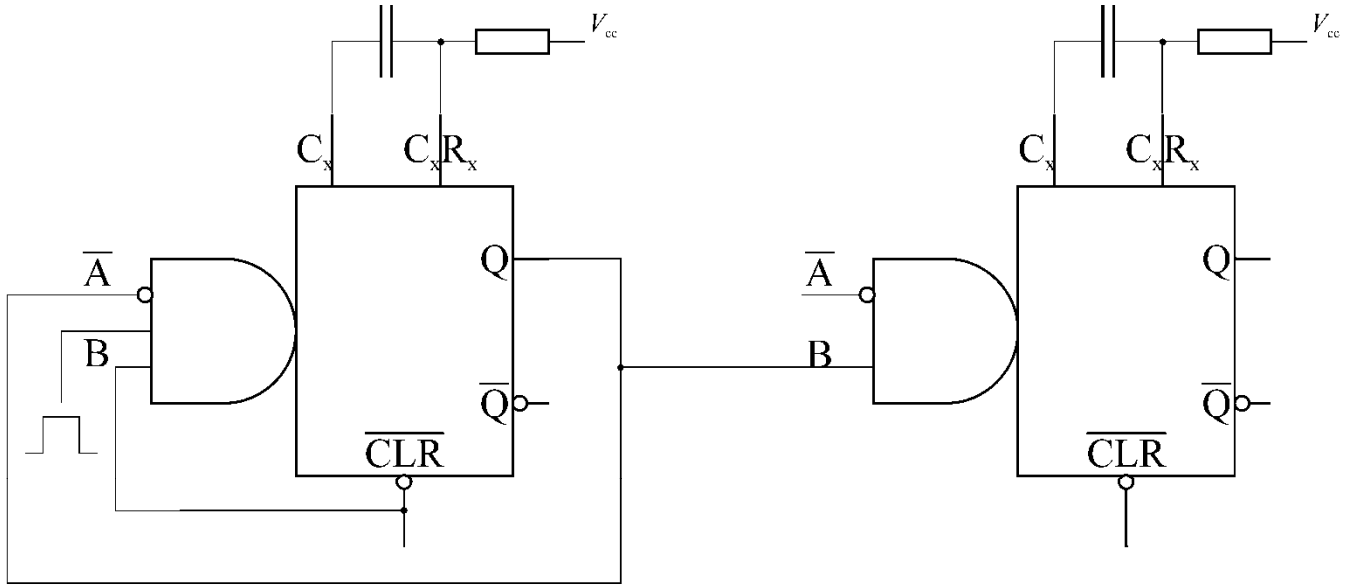
$$f = \frac{1}{T + t_p}$$

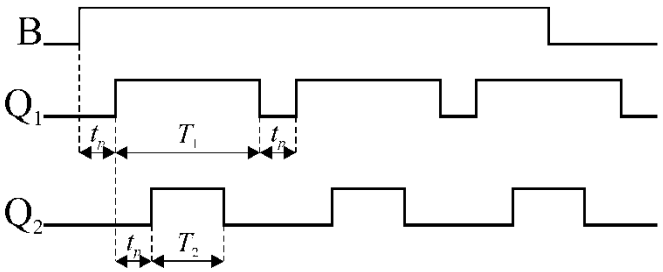
$$\eta = \frac{T}{T + t_p}$$



Time circuits – part 1

- 74123 as a frequency generator
  - Using a short pulse generator



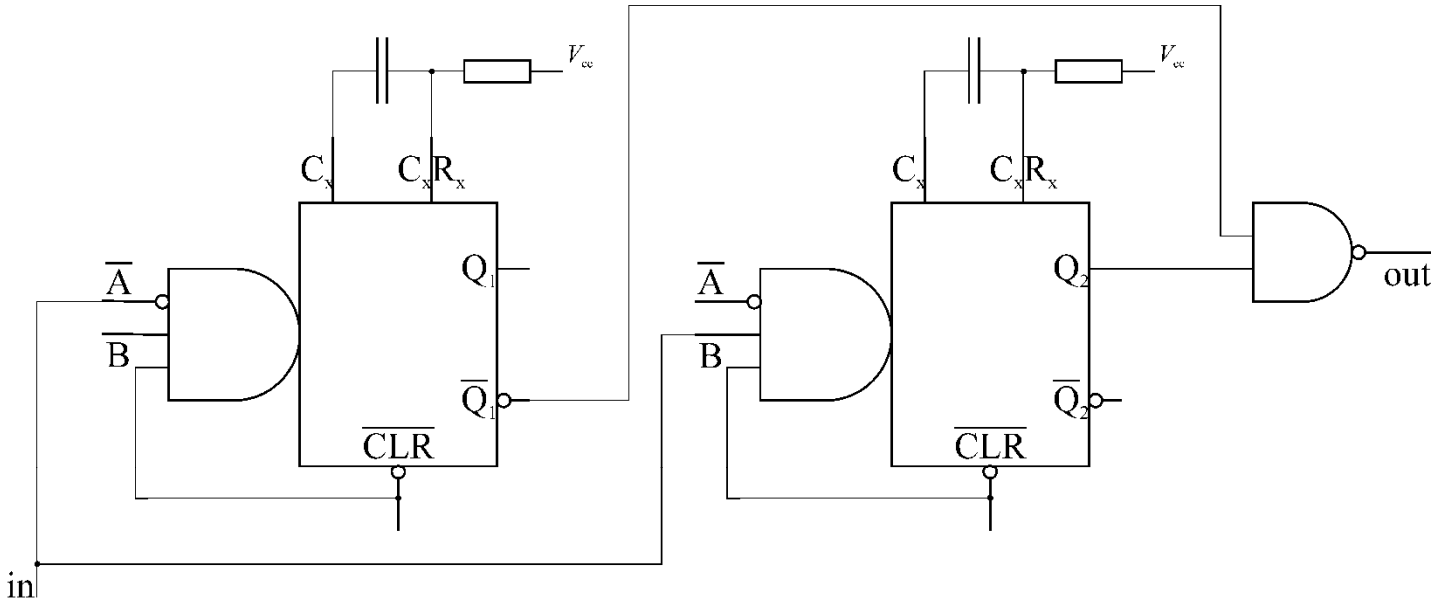


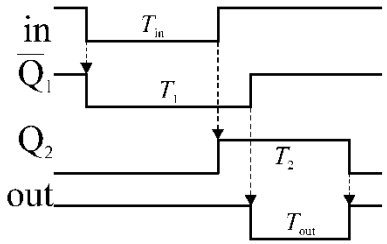
$$f = \frac{1}{T_1 + t_p}$$

$$\eta = \frac{T_2}{T_1 + t_p}$$

Time circuits – part 1

- 74123 as edge delay circuit





Time circuits – part 1

- 74123 as frequency comparator