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Digital Circuits Design

Faculty of Automatic Control, Electronics and Computer Science, Informatics, Bachelor Degree

Lecture 2

Digital IC Parameters – part 2

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Parameters – part 2

Program:

(last week)

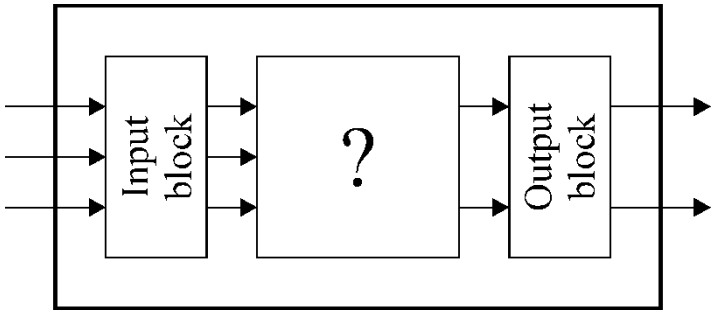
- Parameter groups
- Functional parameters
- Dynamic parameters

(today)

- Static parameters
- Operational conditions parameters
- Clock asynchronism, example values

Parameters – part 2

- Static parameters
  - Digital IC inputs and outputs properties
  - Cooperation conditions with other IC's
  - Depend on input and output structure and not on IC function

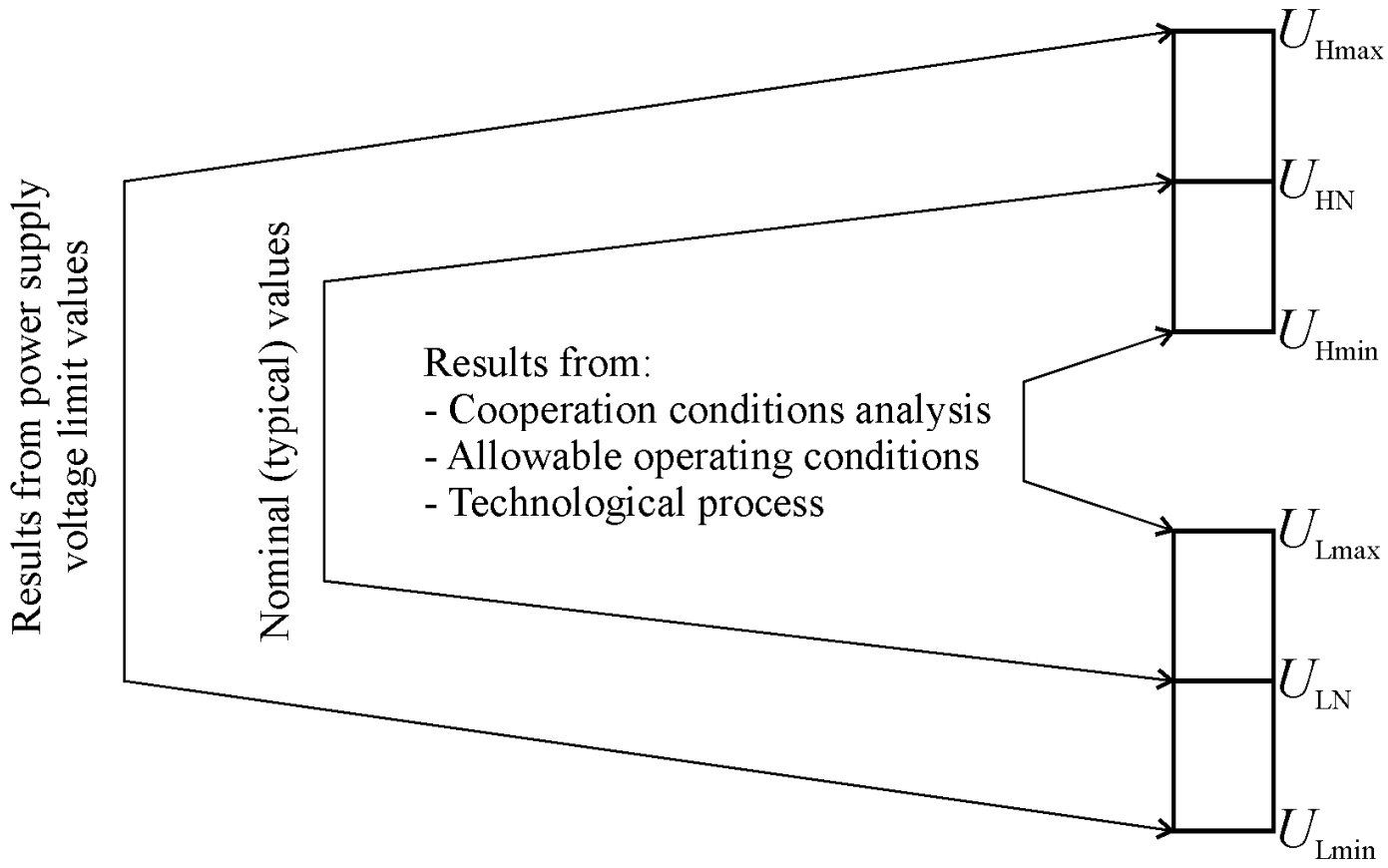


- Voltage parameters
  - Logic levels voltages
  - Operation conditions in the presence of interferences and noise

- Current parameters
  - Conditions of control of IC by another IC

Parameters – part 2

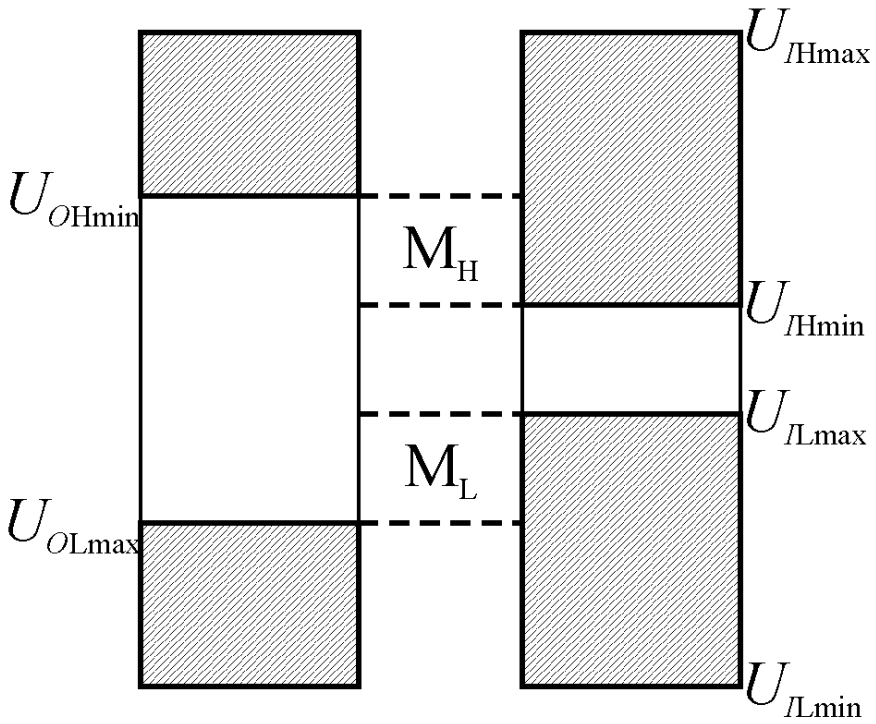
- Voltage parameters



Parameters – part 2

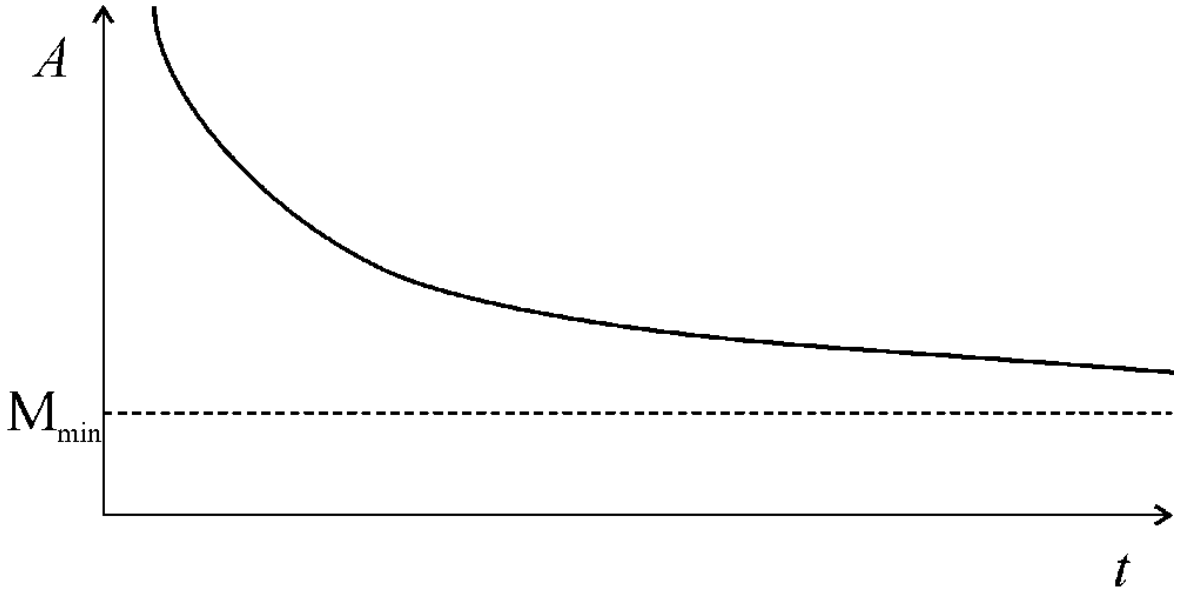
- Interference margin
  - IC immunity to direct current interference in the worst case
  - Minimum interfence margin:

$$M_L = |U_{I\mathrm{Lmax}} - U_{O\mathrm{Lmax}}|$$
$$M_H = |U_{I\mathrm{Hmin}} - U_{O\mathrm{Hmin}}|$$



Parameters – part 2

- Immunity to alternating current interference
  - Max amplitude *A* of interference duration time *t* which does not cause any errors in a digital system
  - For t→∞, alternating current immunity → direct current immunity



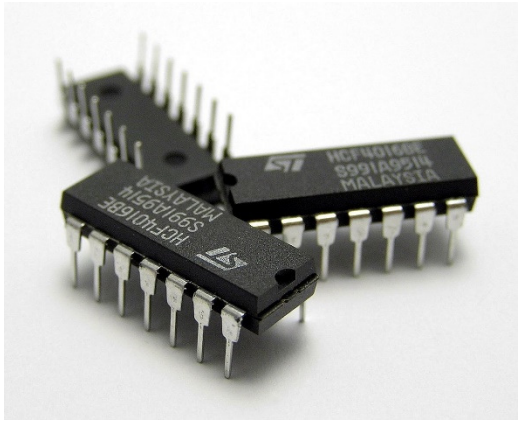
  - Current static parameters – max values of input and output currents

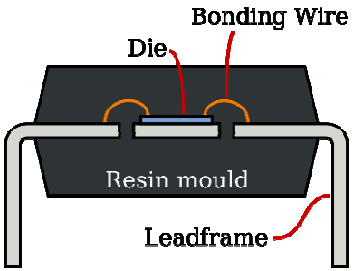
Parameters – part 2

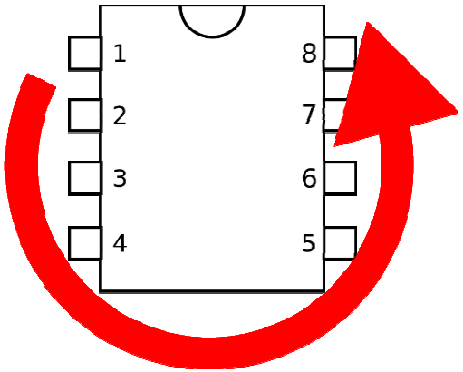
- Operation conditions parameters
  - Power supply
    - Number of supply voltages, power consumptions, etc.
    - Quality factor (?)
      - Average power × average propagation time
  - Allowable conditions, limit parameters
    - Temperature, humidity, pressure
    - Load value
    - Power voltage jitter
  - IC housing
    - DIP
      - Through-hole mount
      - Surface mount

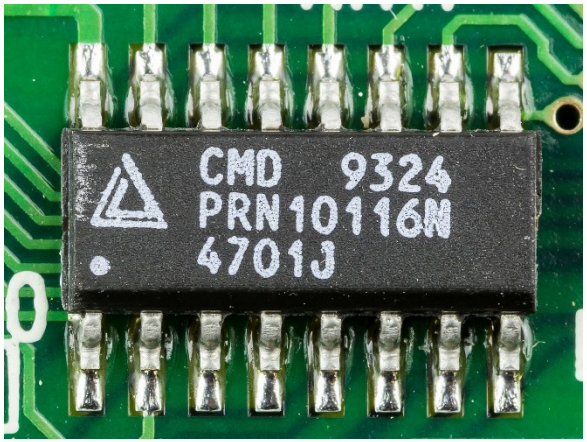
Parameters – part 2

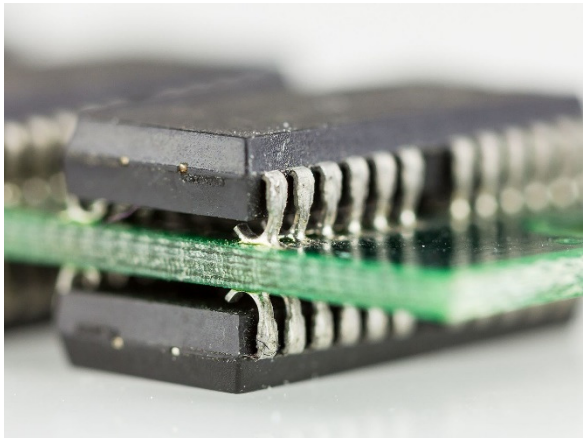
- Operation conditions parameters
  - IC housing examples





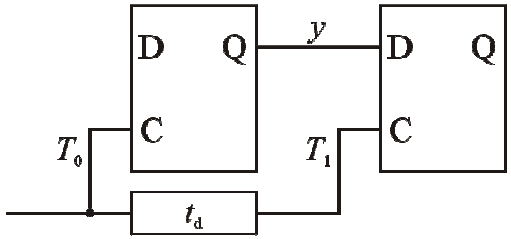


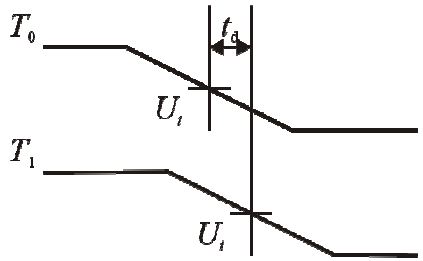


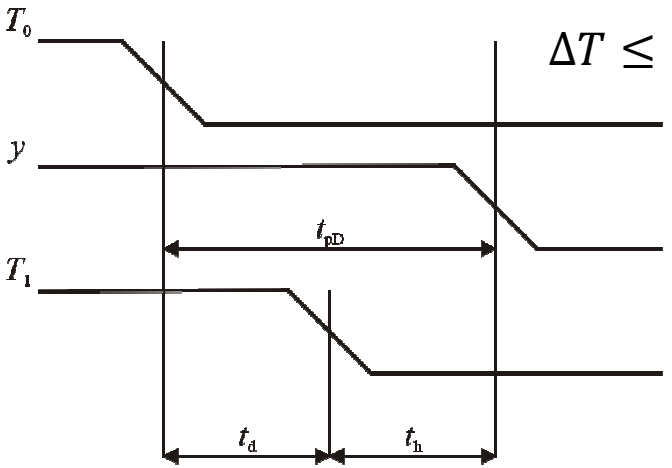


Parameters – part 2

- Clock asynchronism
  - Results from static and dynamic parameters
  - Occurs in synchronous circuits
    - When clock signal must drive many inputs
    - Clock signal at different inputs can be shifted in time







$$\Delta T \leq t_{pD} - t_{hmax}$$

Parameters – part 2

- Clock asynchronism
  - For TTL devices, t_{pD}=10 ns, t_h=5 ns → ΔT ≤ 5 ns
    - Very low value, which may result from production dispersion
  - Can also occur when clock rise and fall times are long
    - Switching threshold dispersion reaches 0.1V
    - To ensure ΔT ≤ 5 ns, $p \geq \frac{0.1V}{5ns} = 20V/\mu s$
    - Thus, t_f or t_r ≤ 125 ns
    - For flip-flops, t_f or t_r ≤ 60 ns
  - When single gate output load is not enough

Parameters – part 2

- TTL IC's
  - Transistor-Transistor Logic
  - Low power consumption (not all series)
  - High logic gain (high load)
  - Low output impedance for 0 and 1
  - Single power supply
  - High immunity to interference
  - Wide temperature range
  - Few series
    - TTL L
    - TTL H
    - TTL LS
    - TTL S
    - TTL AS
    - TTL ALS
    - Voltages similar to TTL std.
    - Input/output currents can significanty differ → classes

Parameters – part 2

- TTL IC's
  - U_{IL}: -0.5 to 0.8 V
  - U_{OL}: 0 to 0.4 V
  - U_{IH}: 2 to 5.5 V
  - U_{OH}: 2.5 to 5 V
  - U_{CC}: 4.75 to 5.25 V
  - Avg t_p: 10 ns
  - Flip-flop f_{max}: 20 MHz
  - Gate P: 10 mW
  - Flip-flop P: 40 mW
  - Temperature 0 to 70 C
  - Logic gain: 10
  - Typical interference immunity: 1V
  - Minimal interference immunity: 0.4V

Parameters – part 2

- CMOS IC's
  - Complementary Metal-Oxide Semiconductor
  - Nowadays fast enough (formerly very slow)
  - Very low power consumption
  - Wide power supply range
    - Higher V_{CC} → higher f_{max}, wider interference margin

	4000B			74C			74HC			74HCT	74AC
V_{CC}	2÷18			3÷15			2÷6			4.5÷5.5	2÷6
V_{CC}	5	10	15	5	10	15	2	4.5	6	4.5÷5.5	4.5
U_{ILmax}	1.5	3	4	1.5	3	4	0.3	0.9	1.2	0.8	0.9
U_{OLmax}	0.05	0.05	0.05	0.05	0.05	0.05	0.1	0.1	0.1	0.1	0.1
U_{IHmin}	3.5	7	11	3.5	7	11	1.5	3.15	4.2	2.0	3.15
U_{OHmin}	4.95	9.95	14.95	4.95	9.95	14.95	1.9	4.4	5.9	4.4	4.4
I_I	100pA÷10mA										
I_{OL}	0.36			0.36			4			4	24
I_{OH}	0.36			0.36			4			4	24

Parameters – part 2

- CMOS vs. TTL

Technology		CMOS	HCMOS	FACT	TTL	TTL LS	TTLS	ALS	AS
V_{CC}	[V]	3-18	HCT: 5 HC: 2-6	ACT: 5 AC: 2-6	5	5	5	5	5
I_{in}	mA	0.001	0.001	0.001	1.6	0.4	2.0	0.1	0.5
P_{stat}	mW	2.5 nW	2.5 nW	2.5 nW	10	2	19	1	8.5
Q	pJ	0.2	0.02	0.01	100	20	57	8	16
t_p	ns	90	9	5	10	10	3	4	1.5
TTLLS Load	Std	2	10		40	20	50	20	50
	Buf	16	16		120	60	160	120	160
Interf. margin $\%V_{CC}$	0	29	HC: 28 HCT: 14	AC: 28	8	8	8	8	8
	1	29	HC: 28 HCT: 58	AC: 28	14	14	14	14	14

Parameters – part 2

- P=f(*f*)
  - V_{CC}=5V
  - C_L=50pF