Fundusze Europejskie
Wiedza Edukacja Rozwój

Rzeczpospolita Polska

Unia Europejska
Europejski Fundusz Społeczny

Politechnika Śląska jako Centrum Nowoczesnego Kształcenia
opartego o badania i innowacje

POWR.03.05.00-IP.08-00-PZ1/17

Projekt współfinansowany przez Unię Europejską ze środków Europejskiego Funduszu Społecznego

Digital Circuits Design

Faculty of Automatic Control, Electronics and Computer Science, Informatics, Bachelor Degree

Lecture 8.

SEMICONDUCTOR MEMORY

Ph.D. Eng. **Adam Opara**

Memory

Agenda:

- Introduction
- Parameters and signals
- Semiconductor memory classification
  - Read Only (ROM, PROM)
  - Non volatile (EPROM, EEPROM, NVRAM, FLASH EEPROM, FRAM, MRAM)
  - Volatile
    - RAM (SRAM, DRAM – EDO, SDRAM , DDR, VSRAM)
    - Special (FIFO, LIFO, associative CAM, dual port)
- Organizing memory blocks

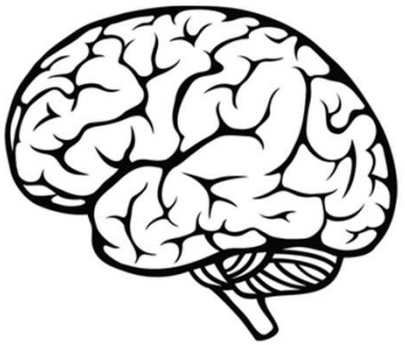
Memory

- Devices used to store a digital information

  (analog devices also exist!)

  – Operational (data and prog. used by µP - semiconductor)

  – External (eg. HDD)



Memory

- Parameters
  - Capacity - # of cells
  - Word length (organization #words x #word length)
  - Access time
  - Memory cycle (+ regeneration)
  - Power per bit (technology: bipolar, CMOS)

Memory

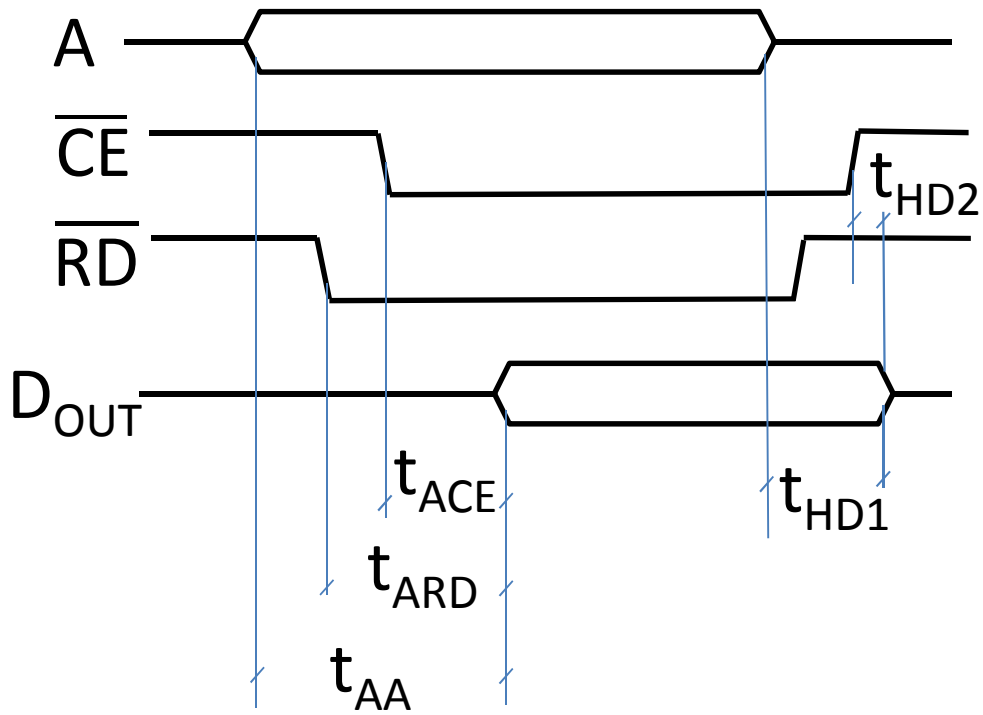
- Signals
  - Address (input)
  - Data (input)
  - Data (output)

  } or in/out

  - Control
    - Chip enable or chip select $\overline{\mathrm{CE}}$, $\overline{\mathrm{CS}}$
    - Access type $\overline{\mathrm{OE}}$, $\overline{\mathrm{WE}}$, $\mathrm{R}/\overline{\mathrm{W}}$
    - Enable programming (non-volatile mem.)

Memory parameters

- Read timing. The access time measured from change of
  - address t_{AA}
  - chip enable t_{ACE}
  - read signal t_{ARD}

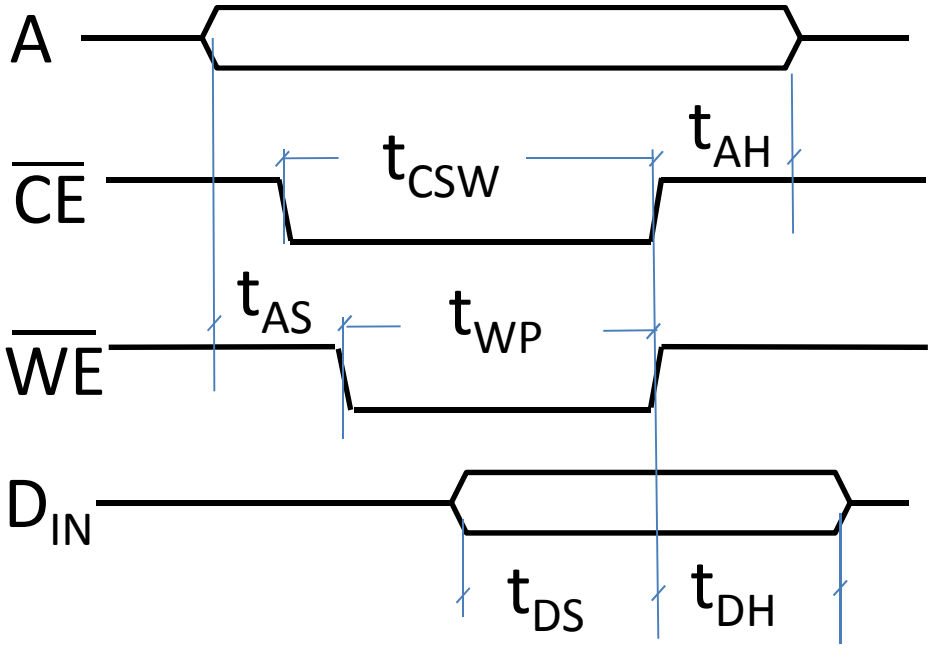


t_{HD1} - hold data time after decaying A

t_{HD2} - hold data time after decaying CE

Memory parameters

- Write timing.



t_{AS} – address setup

t_{AH} – address hold

t_{CSW} – chip select before write

t_{WP} – write pulse minimum width

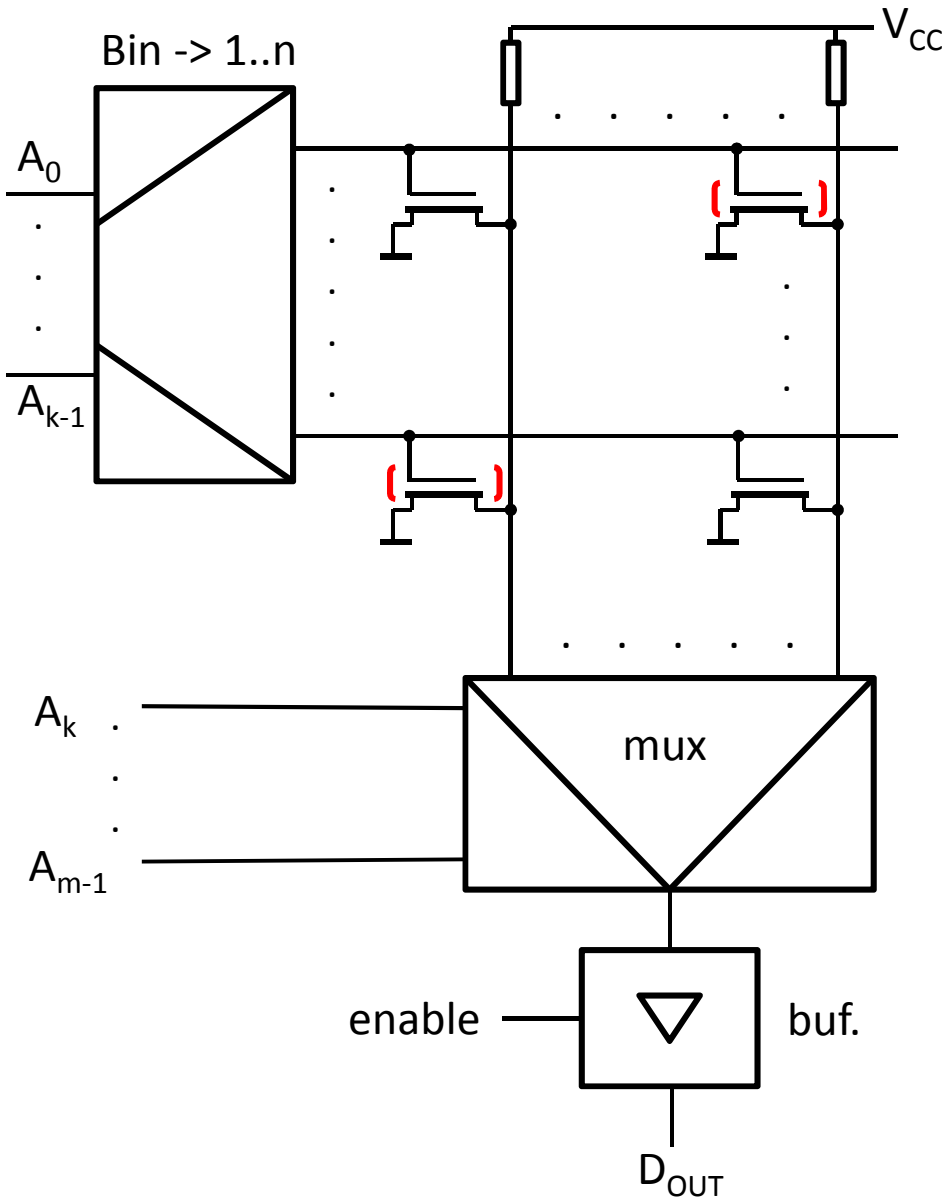
t_{DS} – data setup

t_{DH} – data hold

ROM

- Read Only Memory

Programmed during manufacturing



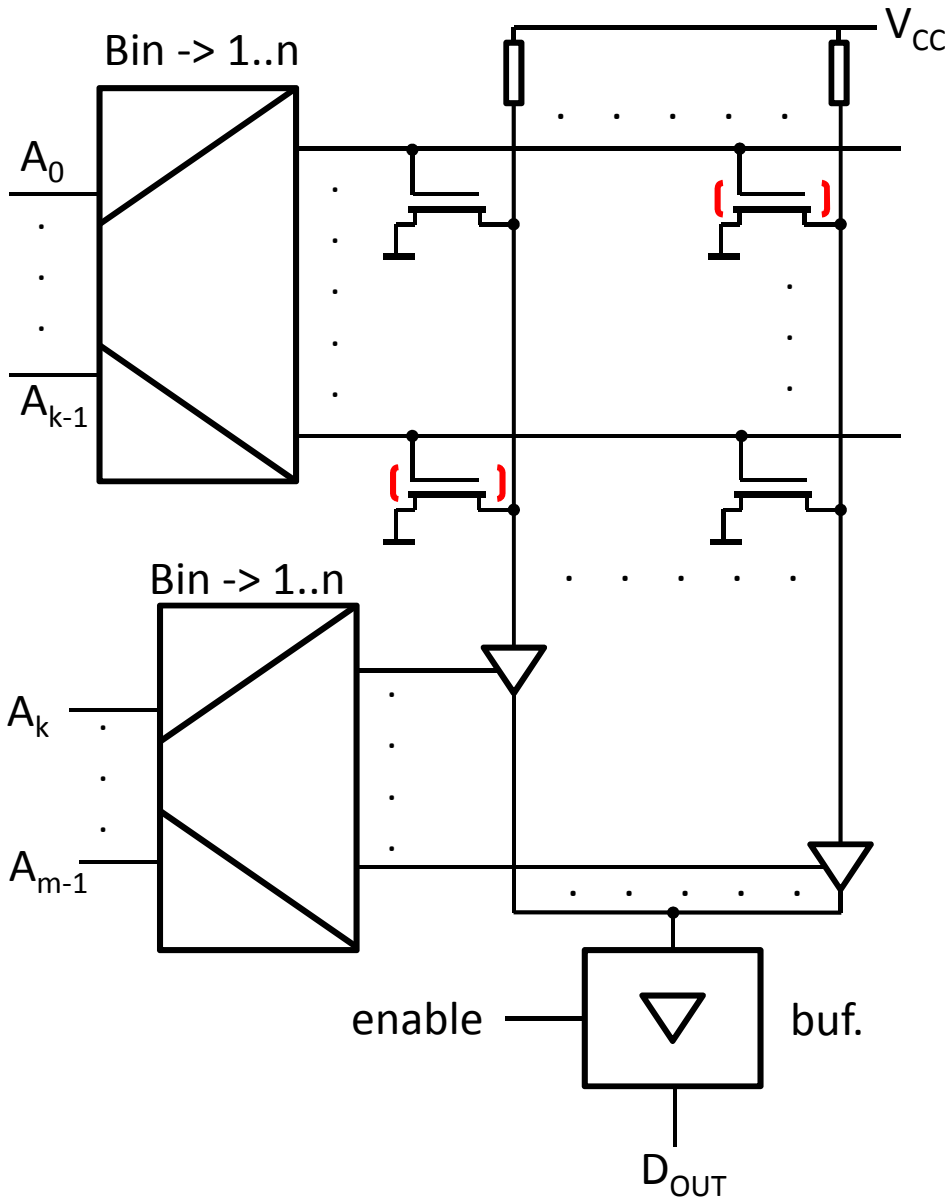
ROM

- Read Only Memory

Programmed during manufacturing

Application:

- character generator,
- code converter,
- multiplier,
- µP program
- A/D, D/A nonlinearity correction
- combinatorial circuits



PROM

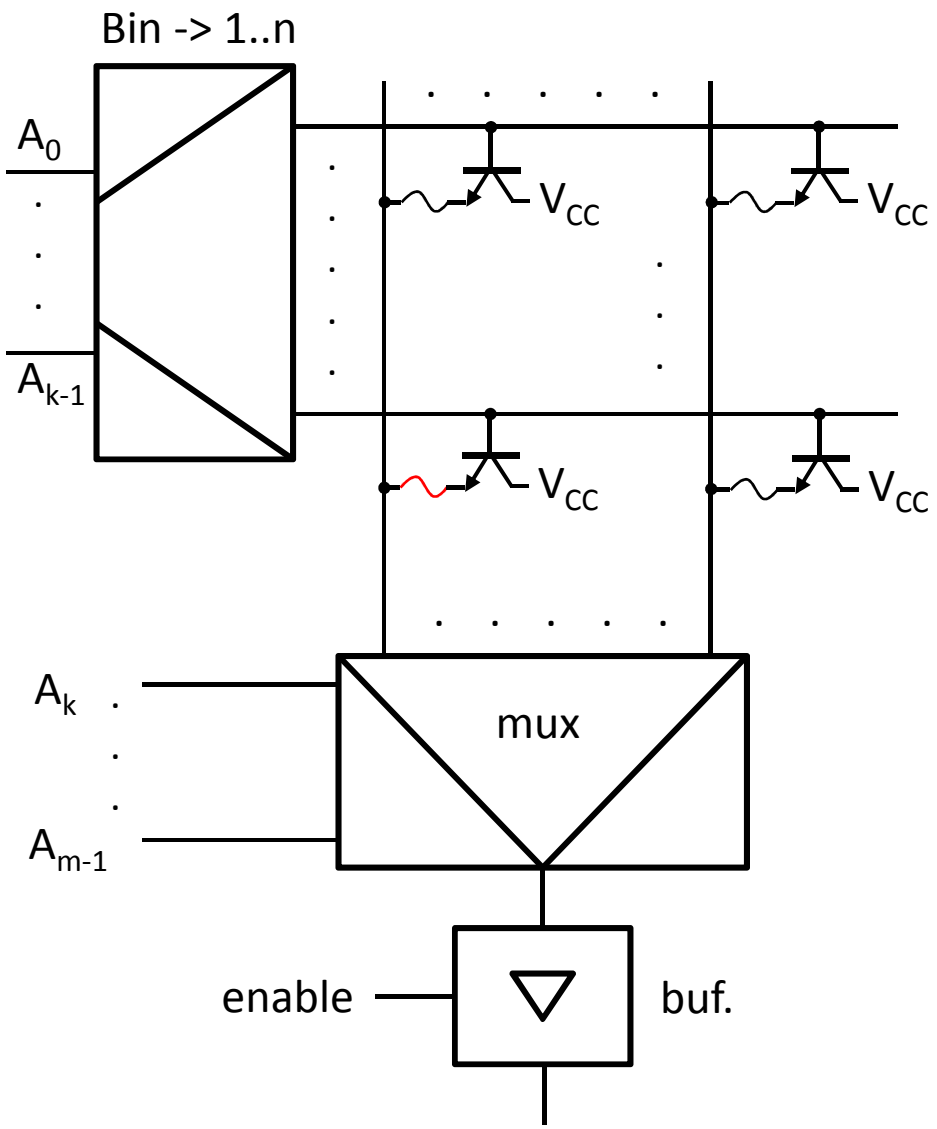
- Programmable ROM

mostly bipolar

10ns-50ns

<128Kb

One time user programmable

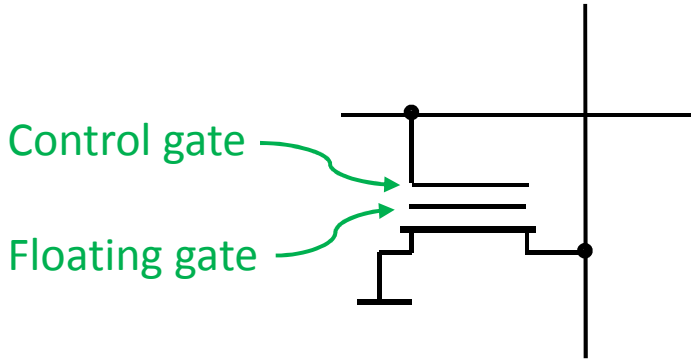


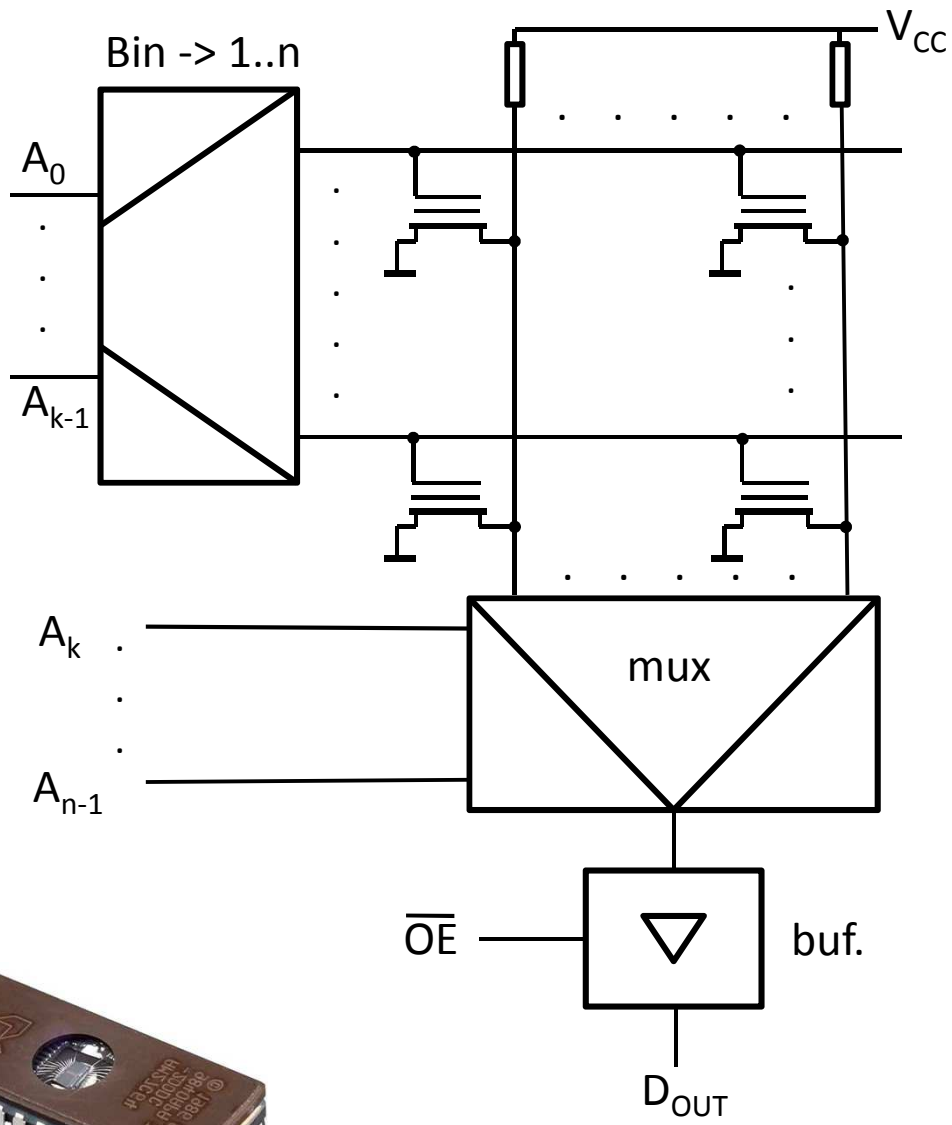
EPROM

- Erasable PROM

Programming:

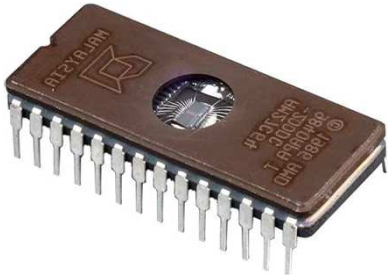
- high U -> c. gate
- electrons -> f. gate





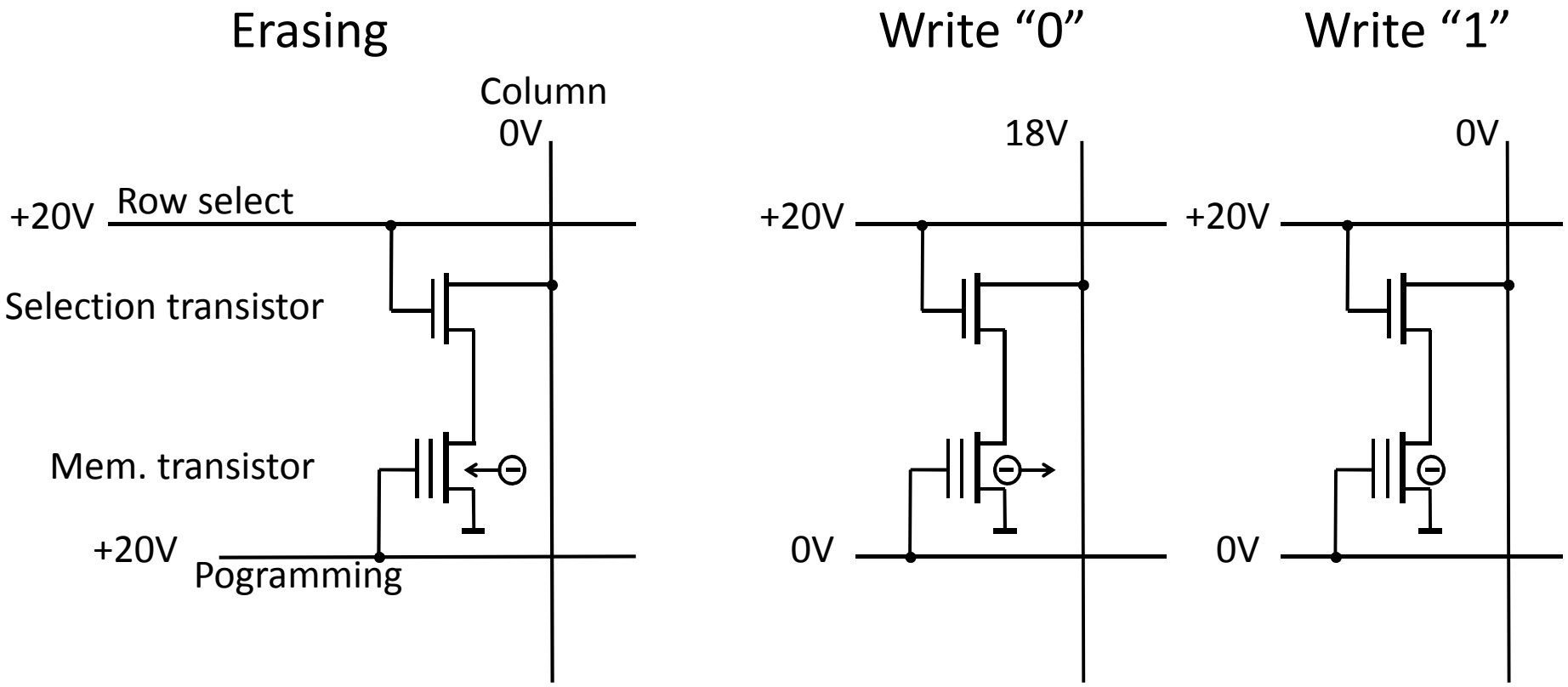
Erasing:

- quartz glass window
- UV 2537 A, 15Ws/cm^2, 15…30 min.

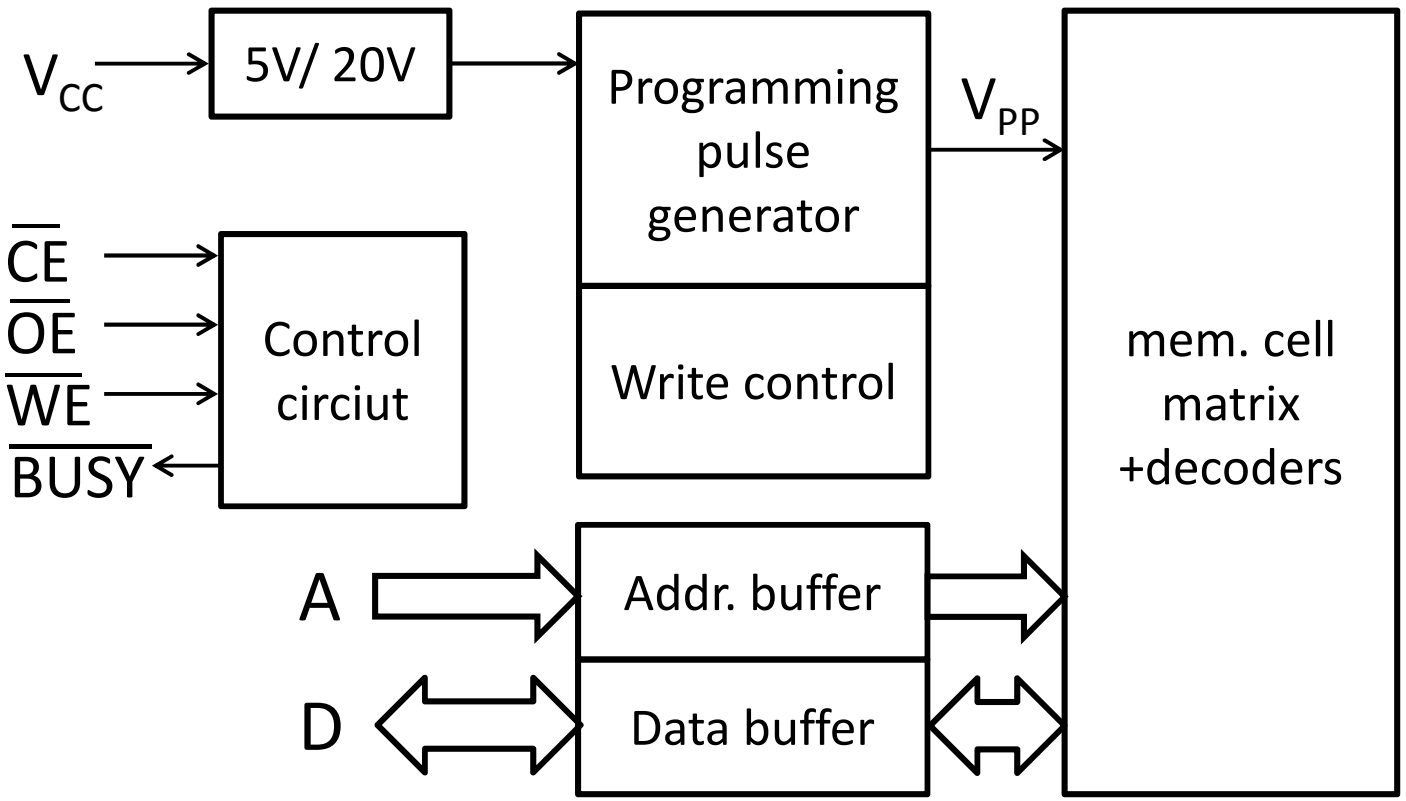


EEPROM

- Electrically Erasable PROM



EEPROM programming

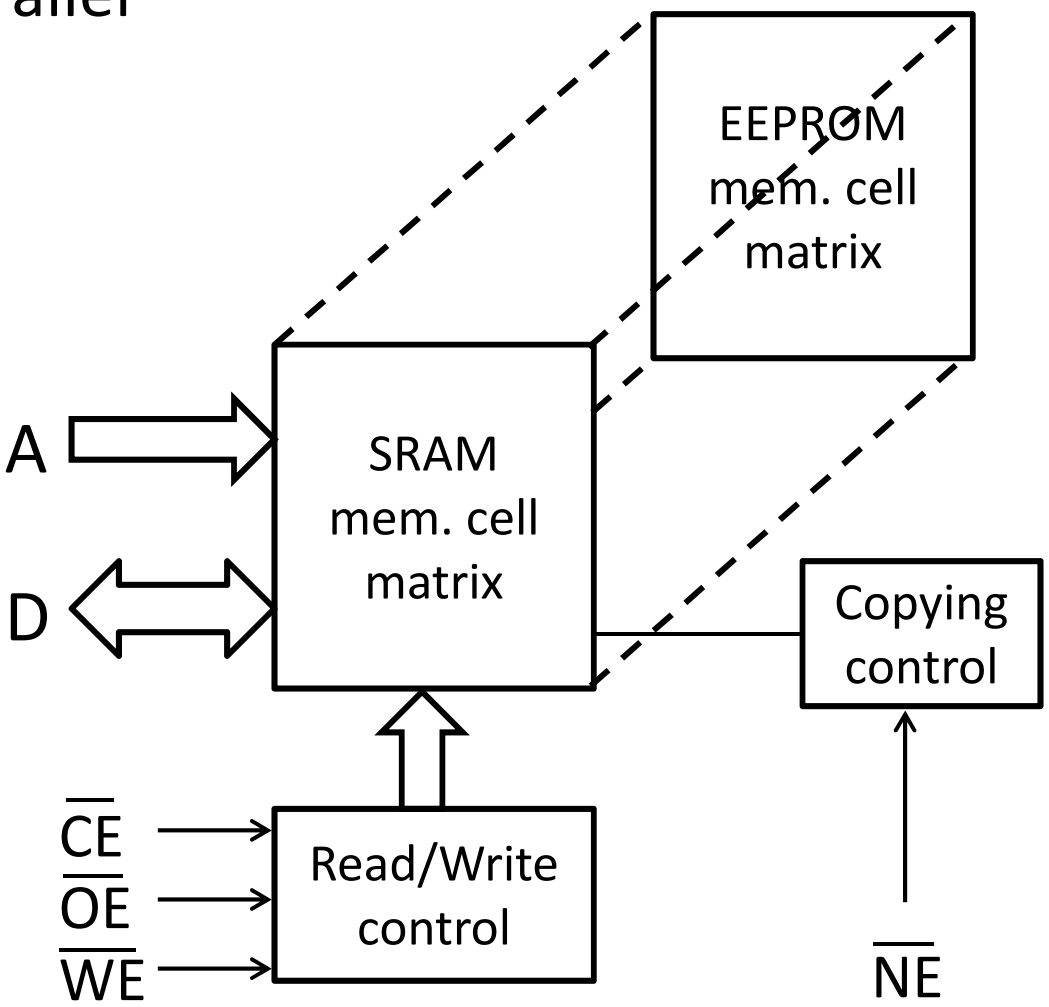


Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	D	$\overline{BUSY}$
Read	0	0	1	D_{OUT}	HiZ
Idle	1	-	-	HiZ	HiZ
Write	0	1	0	D_{IN}	0

NVRAM

- Battery-backed SRAM
- EEPROM+SRAM in parallel
  - Fast
  - Non Volatile

	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{NE}$	
read	**0**	**0**	1	**0**	
write	**0**	1	**0**	**0**	
recall	**0**	**0**	1	1	< 10µs
store	**0**	1	**0**	1	10ms



FLASH

- Fast erase (sector/block)
- Programming wr 0 like in EPROM

- NAND FLASH – high density
- NOR – high durability

New NV memories

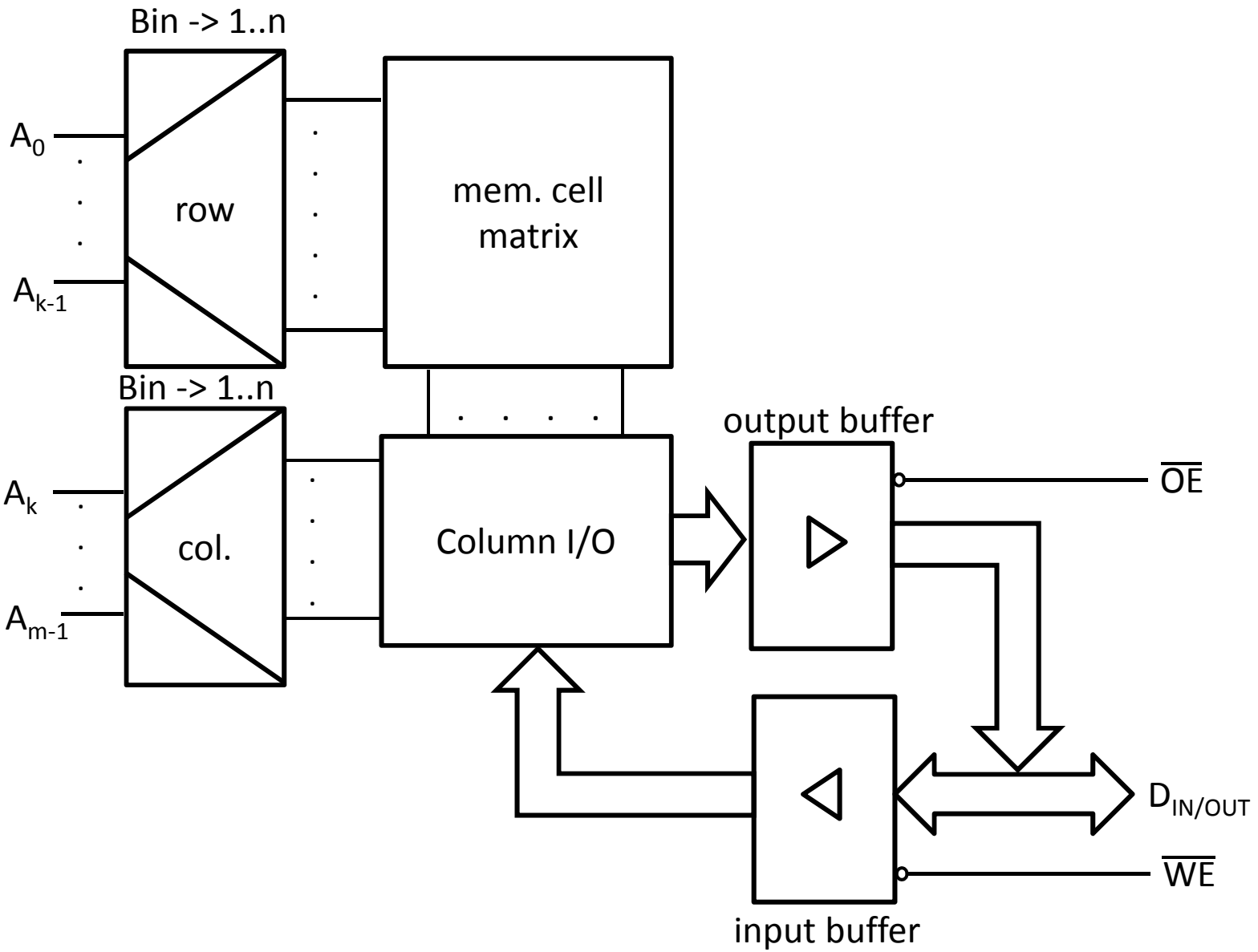
- Ferroelectric RAM (FRAM)
  - Programmable capacitors, dielectric cristals polarize under electric field
  - High density, many RD/WR
  - Low power
- Magnetoresistive RAM (MRAM)
  - Like magnetic core memory
  - Spin electron or tunneling magnetic resistance

SRAM

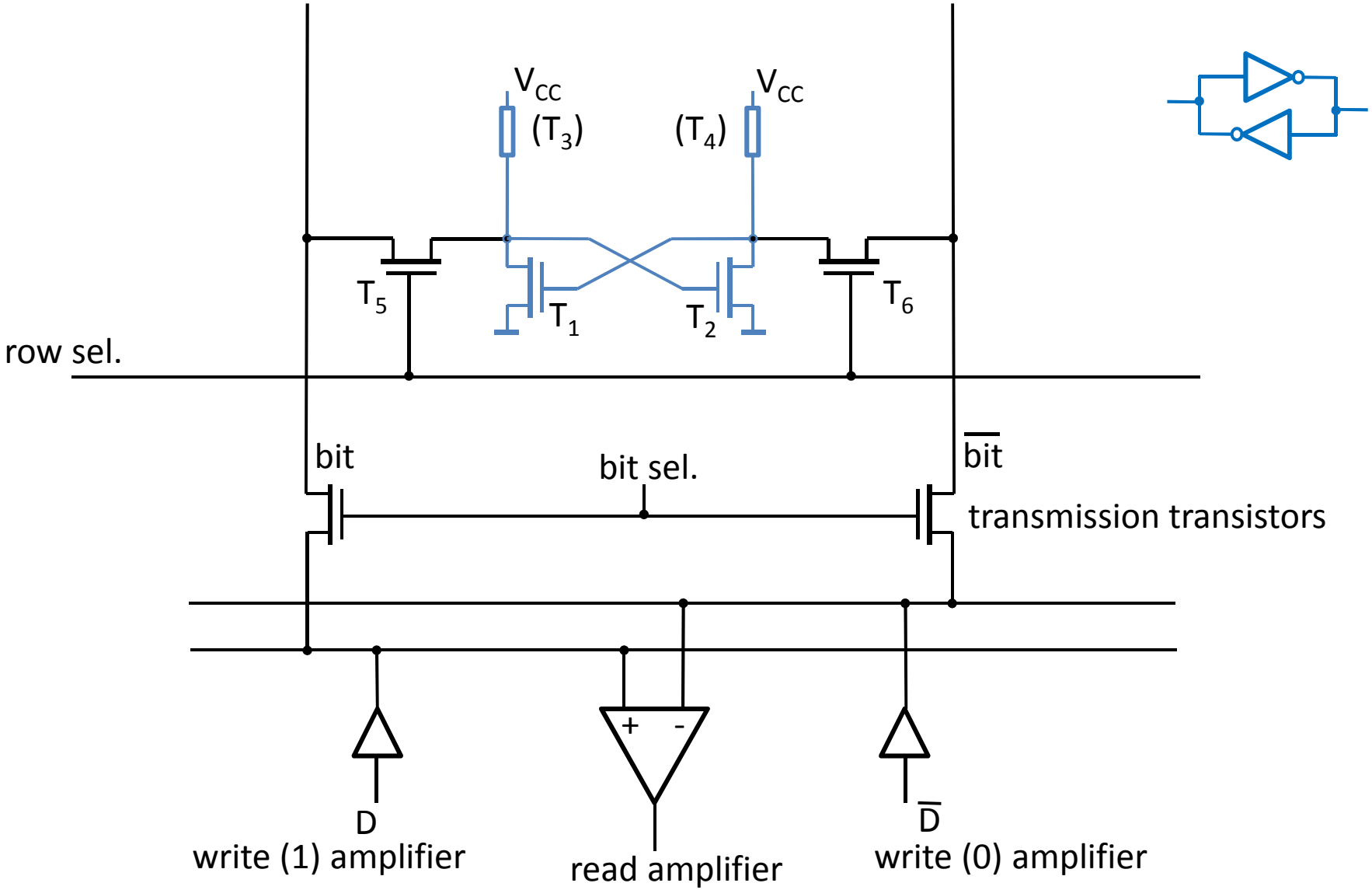
Static RAM

- Fast
- 1 cell = 1 flip flop (4-6 transistors)
- High power dissipation

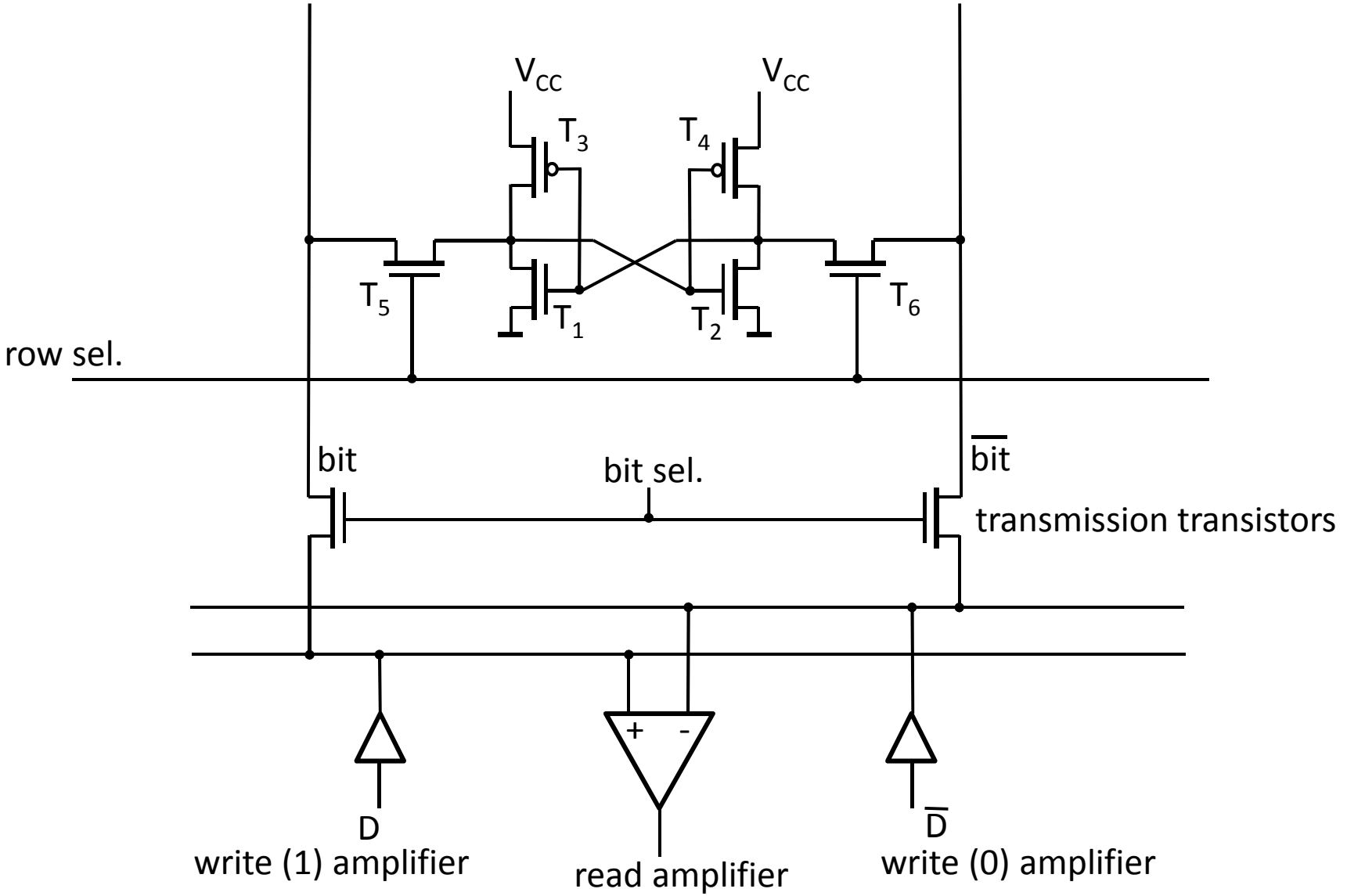
SRAM


Bin -> 1..n
A0
Ak-1
row
mem. cell
matrix
Bin -> 1..n
Ak
Am-1
col.
Column I/O
output buffer
OE
DIN/OUT
WE
input buffer

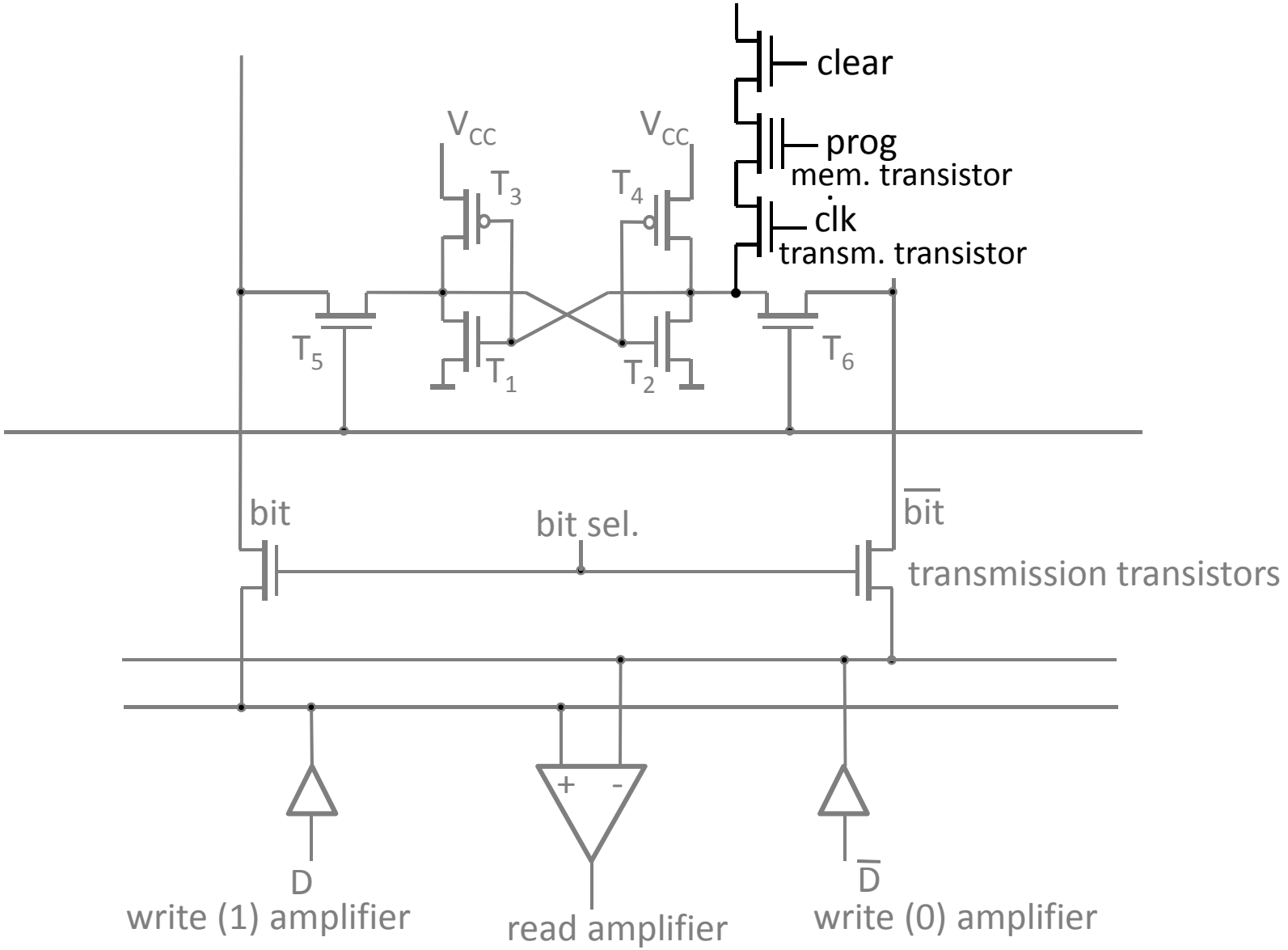
SRAM – memory cell



SRAM – memory cell



NVRAM – EEPROM+SRAM

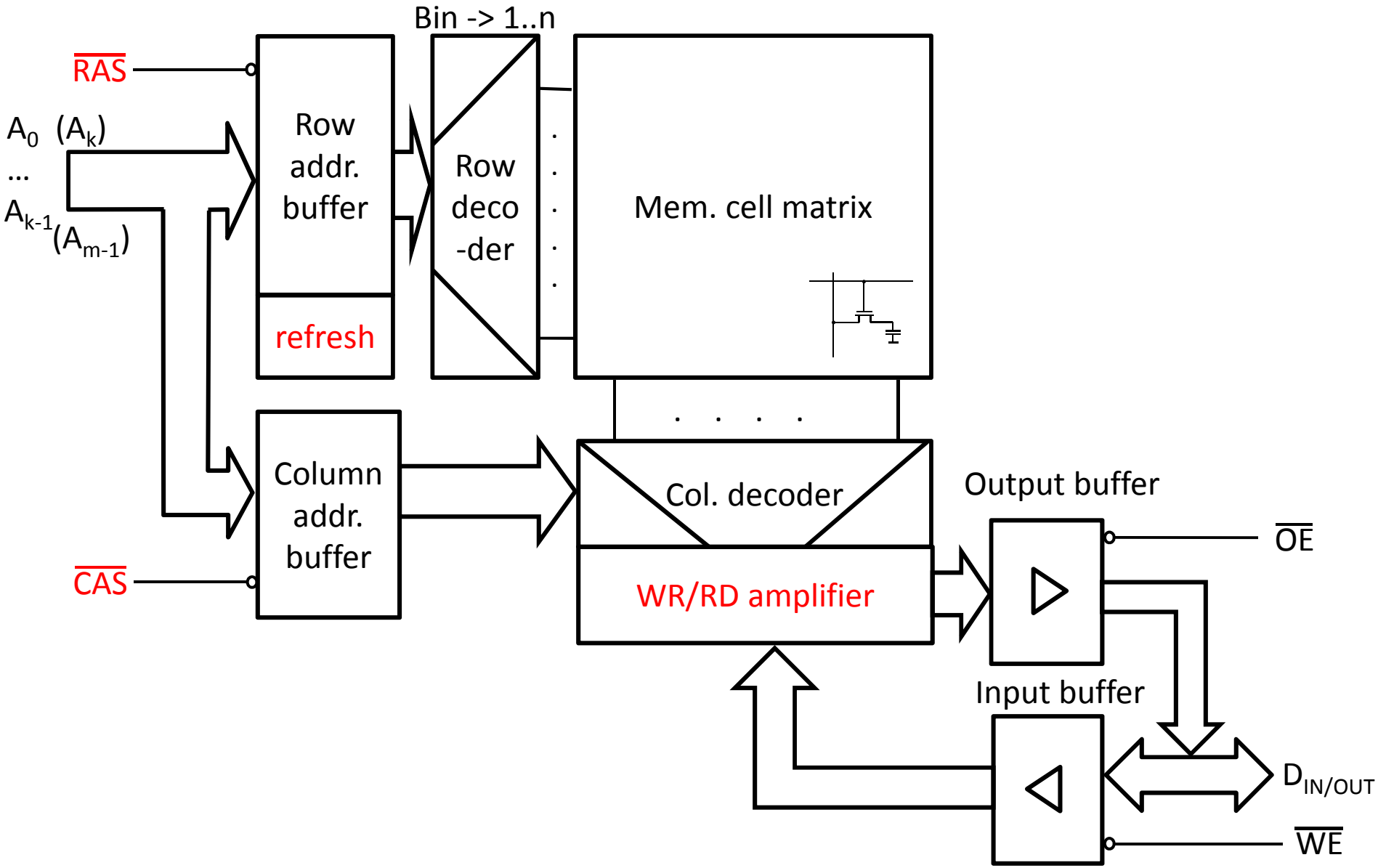


DRAM

Dynamic RAM

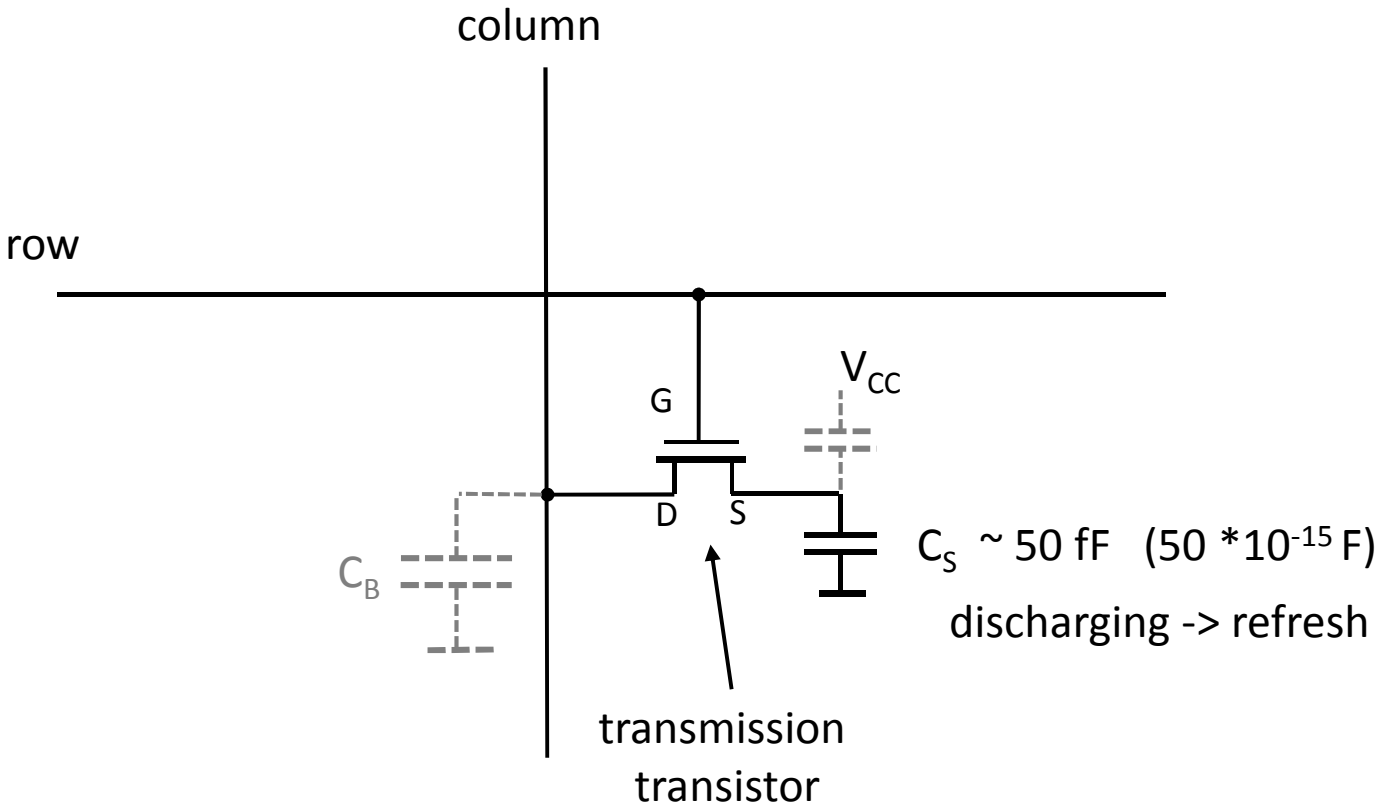
- Slower than Static RAM
- 1 cell = 1 transistor + capacitance
- Refresh

DRAM


Bin -> 1..n
RAS
A0 (Ak)
...
Ak-1 (Am-1)
Row addr. buffer
refresh
Row deco -der
Mem. cell matrix
Column addr. buffer
CAS
Col. decoder
WR/RD amplifier
Output buffer
OE
Input buffer
DIN/OUT
WE

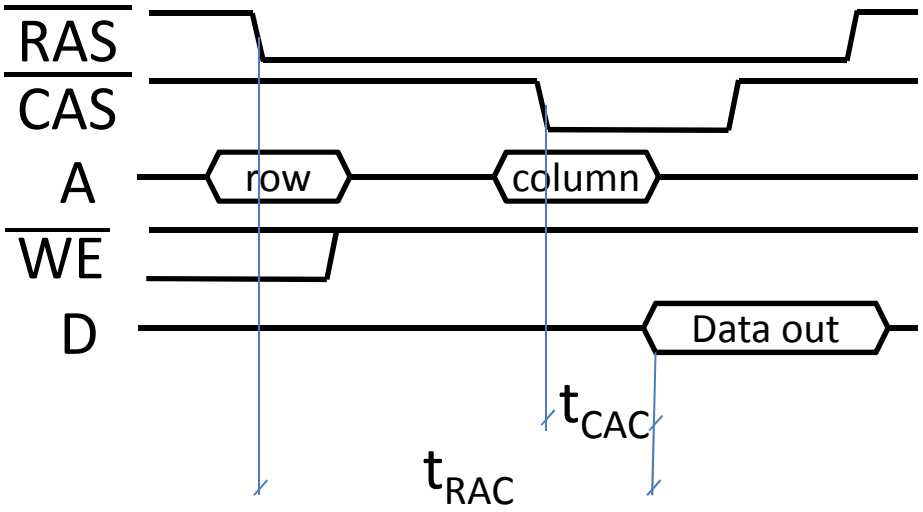
DRAM

Memory cell

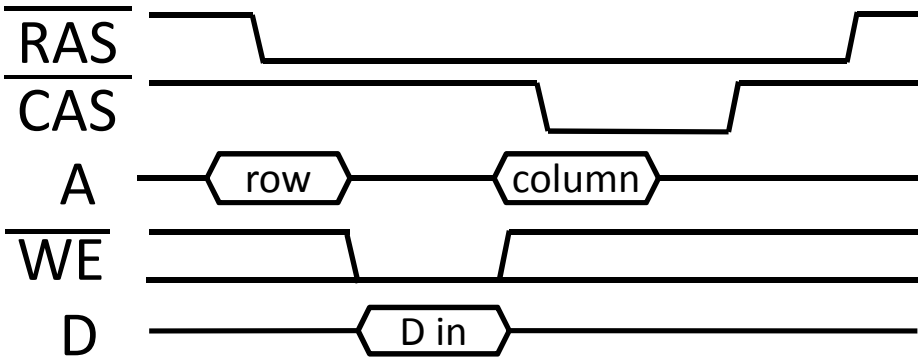


DRAM

Read

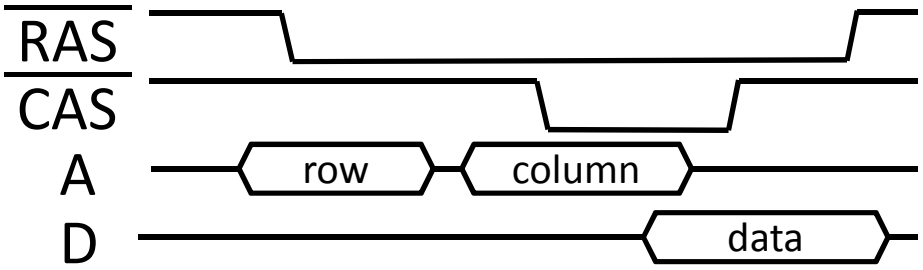


Write

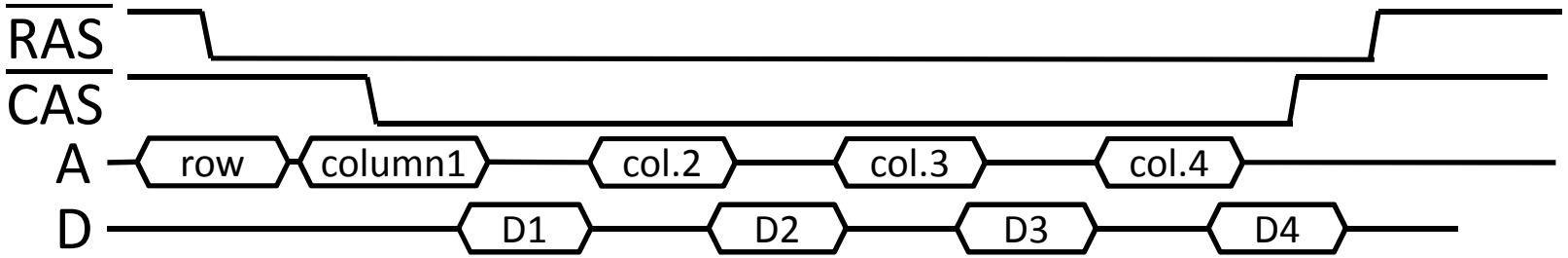


DRAM

Std. CAS writes column addr. and enables output

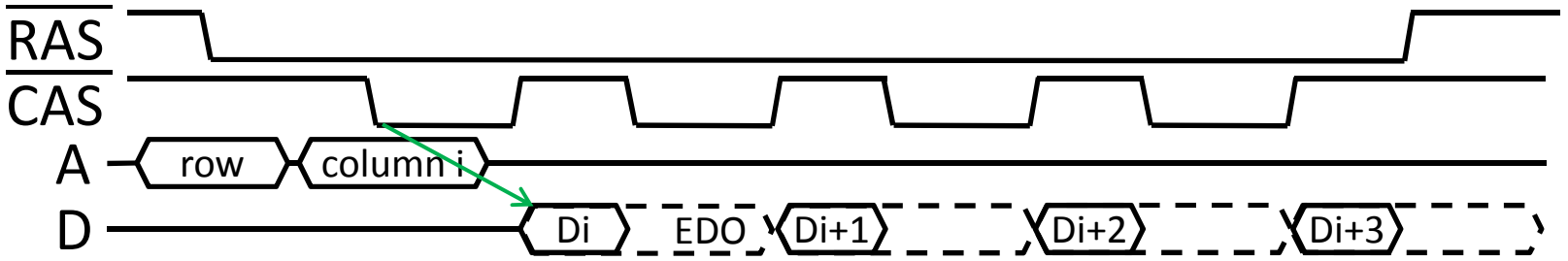


Static columns change of addr. automatically detected, no CAS sync.

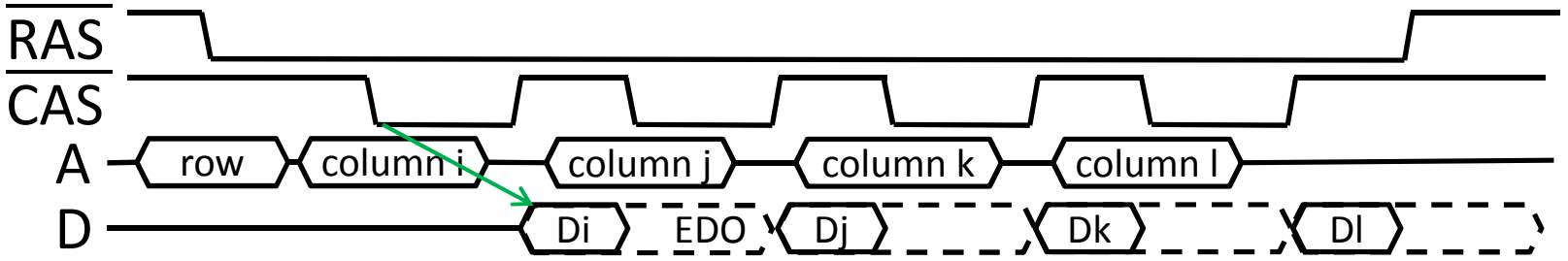


DRAM

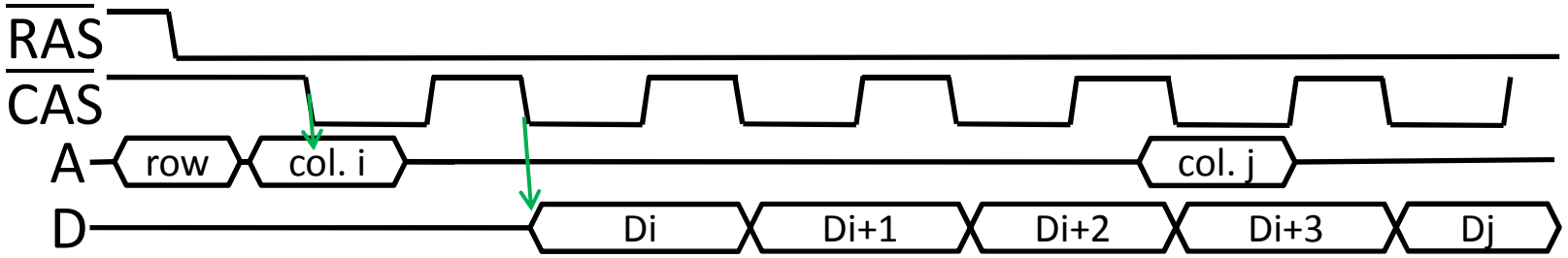
Nibble/EDO fast access to 4 data cells



FastPage/EDO fast access to a few columns

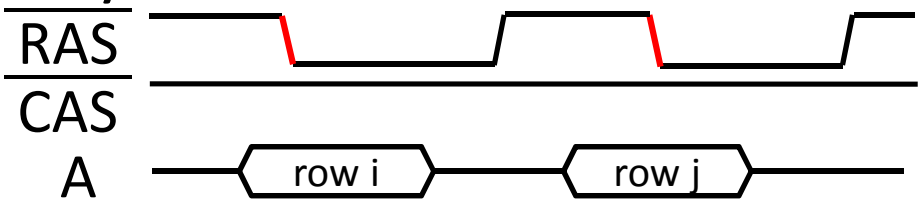


Pipelined Burst EDO Nibble+FastPage

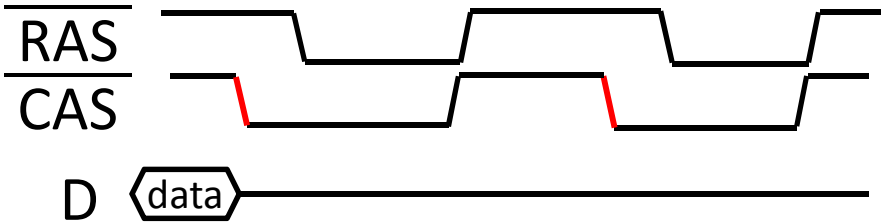


DRAM – refresh timing

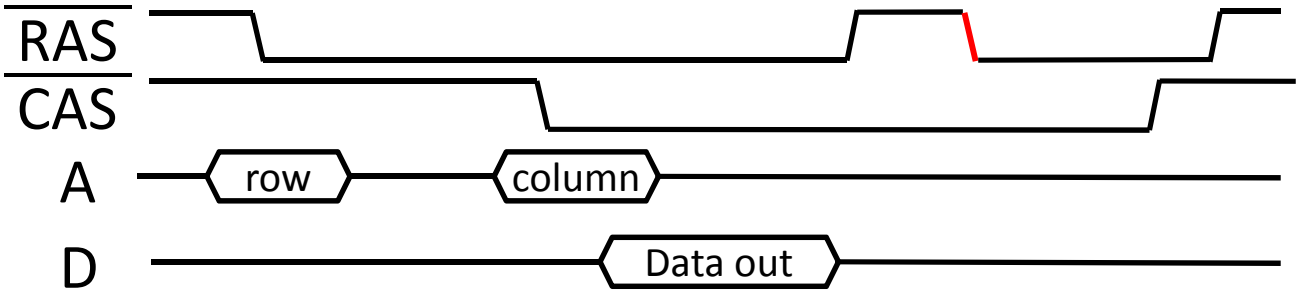
RAS only refresh



CAS before RAS (internal counter)

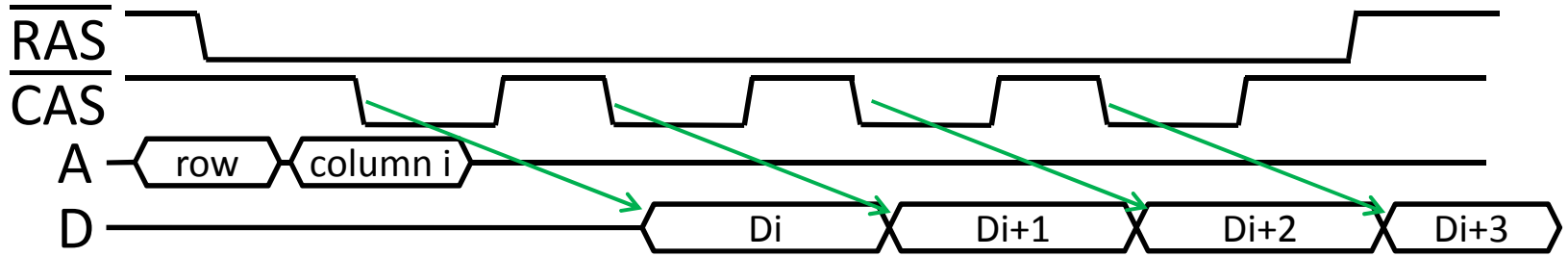


Hidden (additional RAS during read cycle)

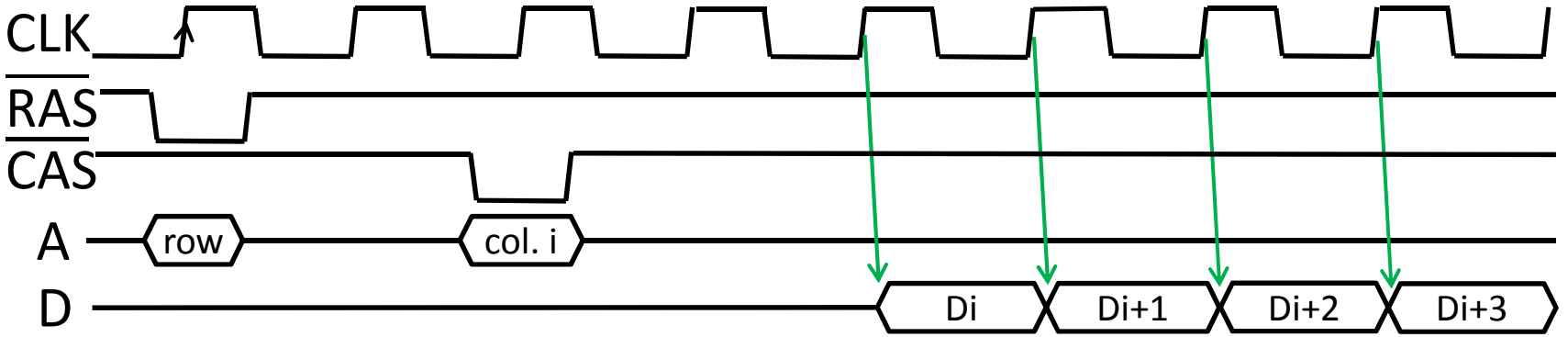


SDRAM

Asynchronous DRAM



Synchronous DRAM



Double Data Rate DDR DRAM

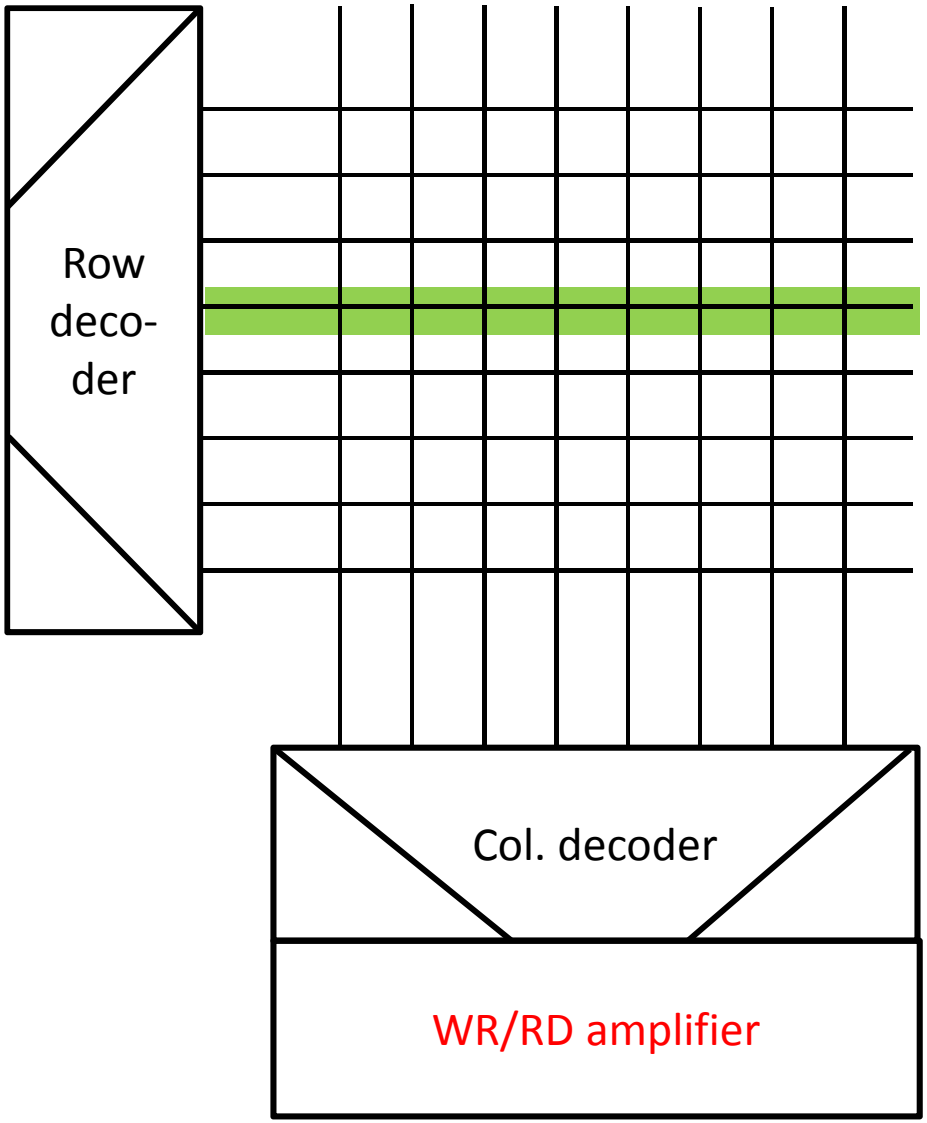
DDR - speed

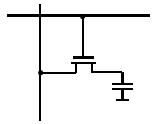
Name		Release	Chip	Bus		Voltage
Generation	Standard	year	Clock rate	Clock rate	Bandwidth	[V]
			[MHz]	[MHz]	[MB/s]	
DDR	DDR-200	2000	100 (10ns)	100	1600	2.5
	…					
	DDR-400		200	200	3200	2.6
DDR2	DDR2-1066	2003	266⅔	533⅓	8533⅓	1.8
DDR3	DDR3-2133	2007	266⅔	1066⅔	17066⅔	1.5/1.35
DDR4	DDR4-3200	2014	400 (2,5ns)	1600	25600	1.2/1.05
DDR5		2020				

DRAM - Row hammer

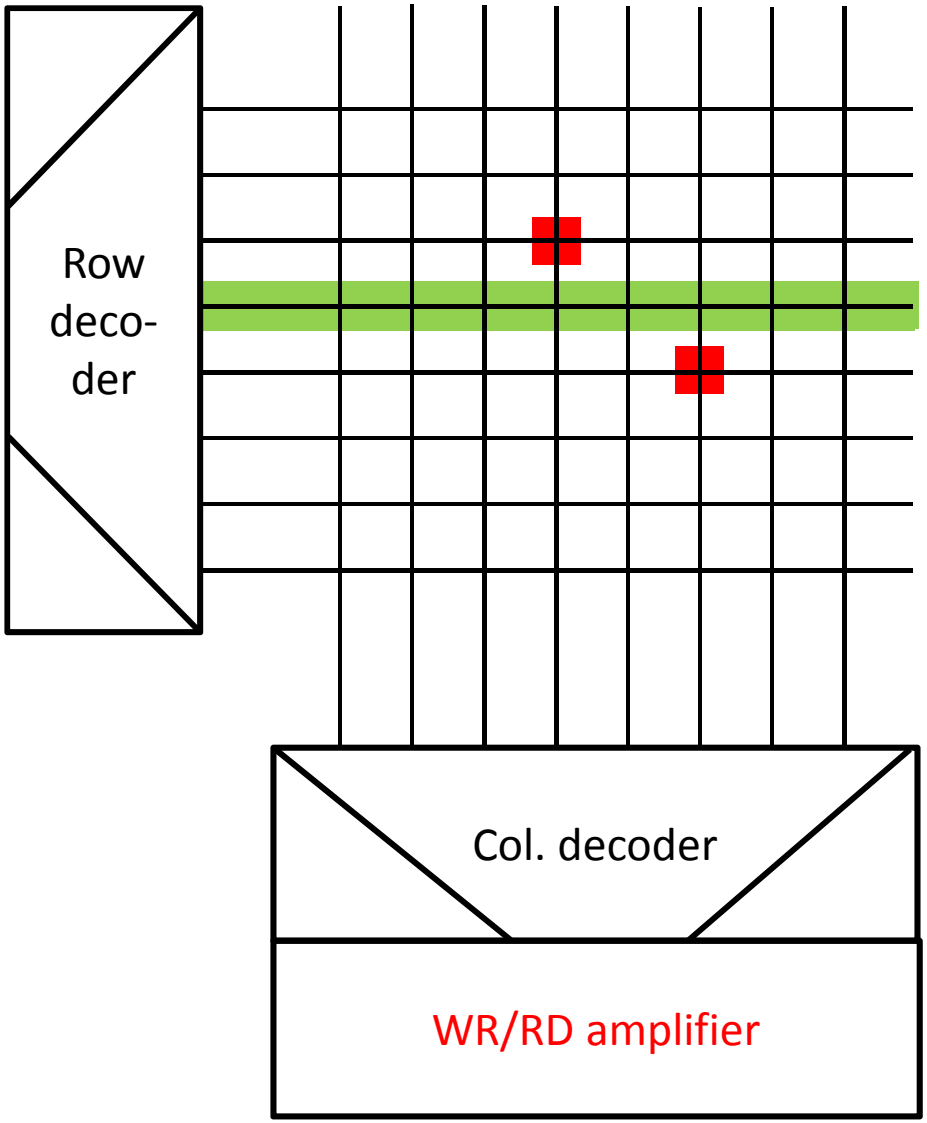
- Row hammer attack - without exploiting software bugs
  - Y. Kim; R. Daly; J. Kim; C. Fallin; J.H. Lee; D. Lee; C. Wilkerson; K. Lai; O. Mutlu (June 24, 2014). "*Flipping Bits in Memory Without Accessing Them: An Experimental Study of DRAM Disturbance Errors*". ece.cmu.edu. IEEE. Retrieved March 10, 2015.

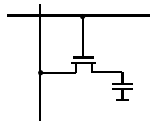
DDR - Row hammer





DDR - Row hammer





DDR - Row hammer

- How we can defend?
  - ECC error correction
  - Refreshing neighbors

Memory

- Organizing memory blocks
  - data width
  - address width