Fundusze Europejskie
Wiedza Edukacja Rozwój

Rzeczpospolita Polska

Unia Europejska
Europejski Fundusz Społeczny

Politechnika Śląska jako Centrum Nowoczesnego Kształcenia
opartego o badania i innowacje

POWR.03.05.00-IP.08-00-PZ1/17

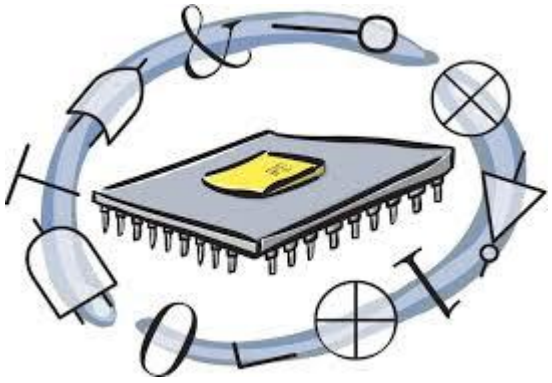
Projekt współfinansowany przez Unię Europejską ze środków Europejskiego Funduszu Społecznego

Digital Circuits Design

Faculty of Automatic Control, Electronics and Computer Science, Informatics, Bachelor Degree

Lecture 10.

Field Programmable Logic Devices (FPGA)



Ph.D. Eng. **Adam Opara**

FPGA

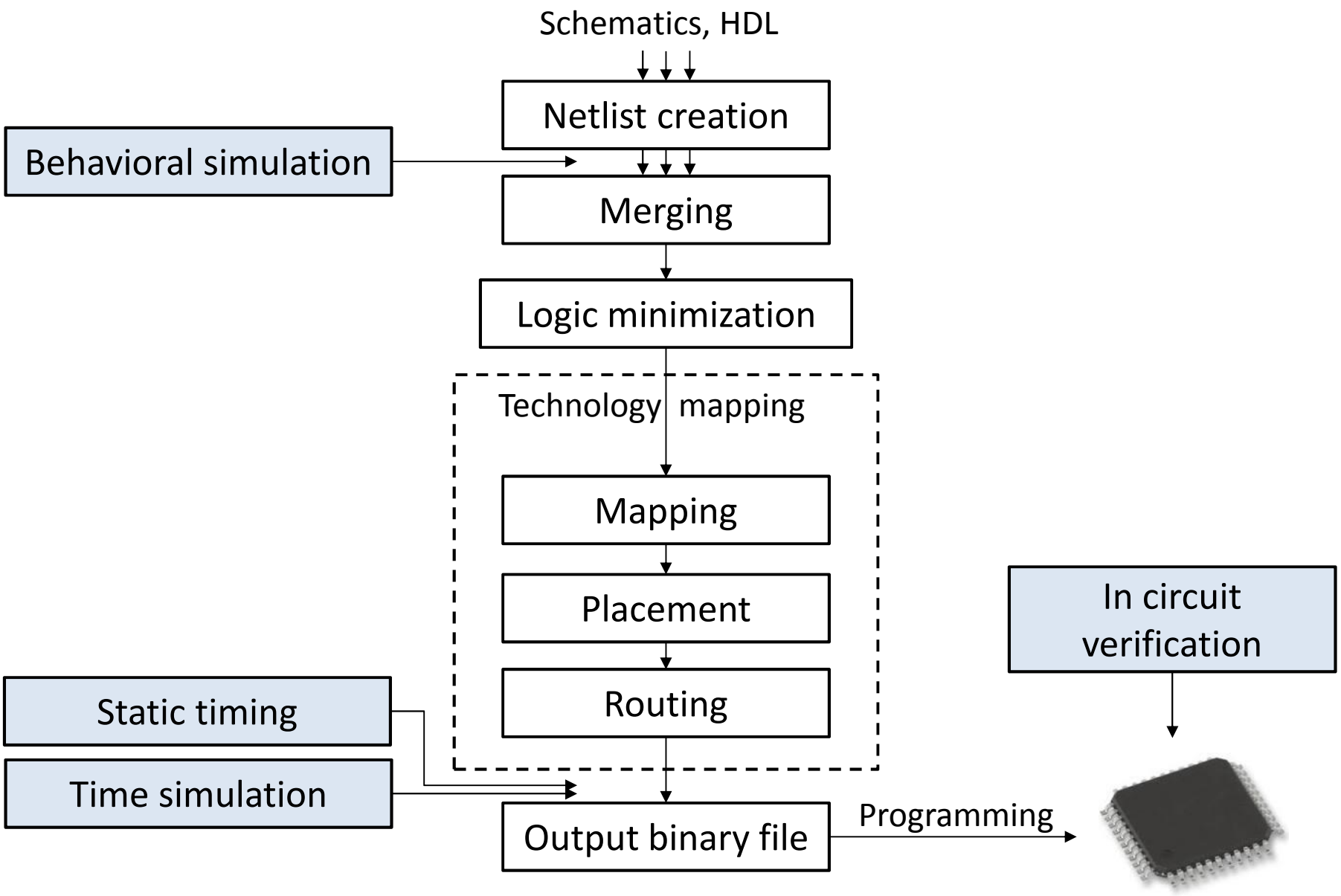
Agenda:

- Why to use FPGA?
- Design process
- Internal structure
  - CLB (LUT4/LUT5, carry logic,FF)
  - Additional elements (block RAM, Mul/Add, PLL)
  - Connection matrix
- Types
  - Simple – only Programmable Logic
  - SoC – Programmable Logic + uP hard cores

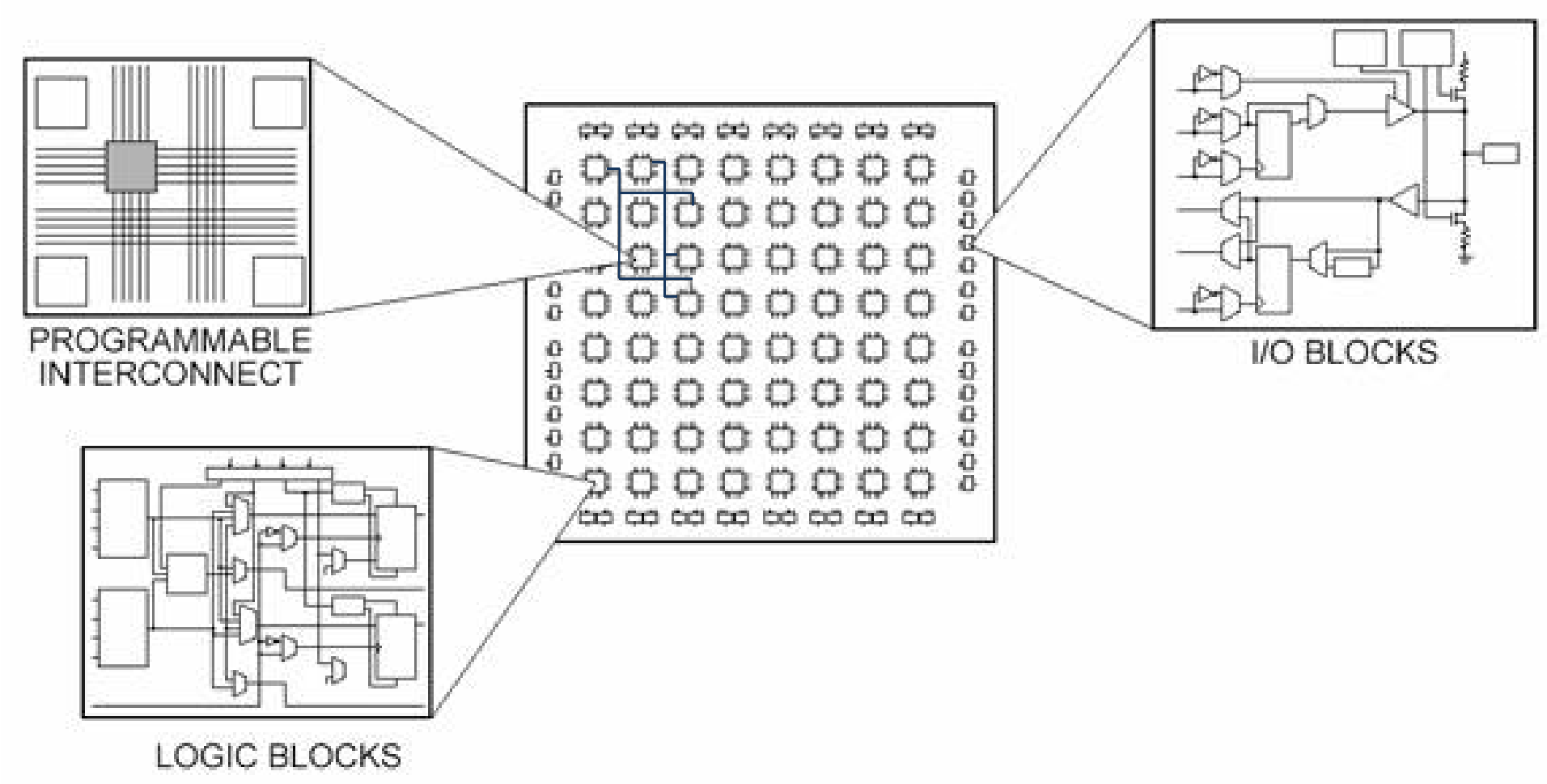
FPGA

- Why use an FPGA not CPU (GPU)?
  - Low latency
  - Connectivity
  - Energy efficiency
  - Disadvantage – engineering costs

FPGA


Schematics, HDL
Netlist creation
Behavioral simulation
Merging
Logic minimization
Technology mapping
Mapping
Placement
Routing
In circuit verification
Static timing
Time simulation
Output binary file
Programming

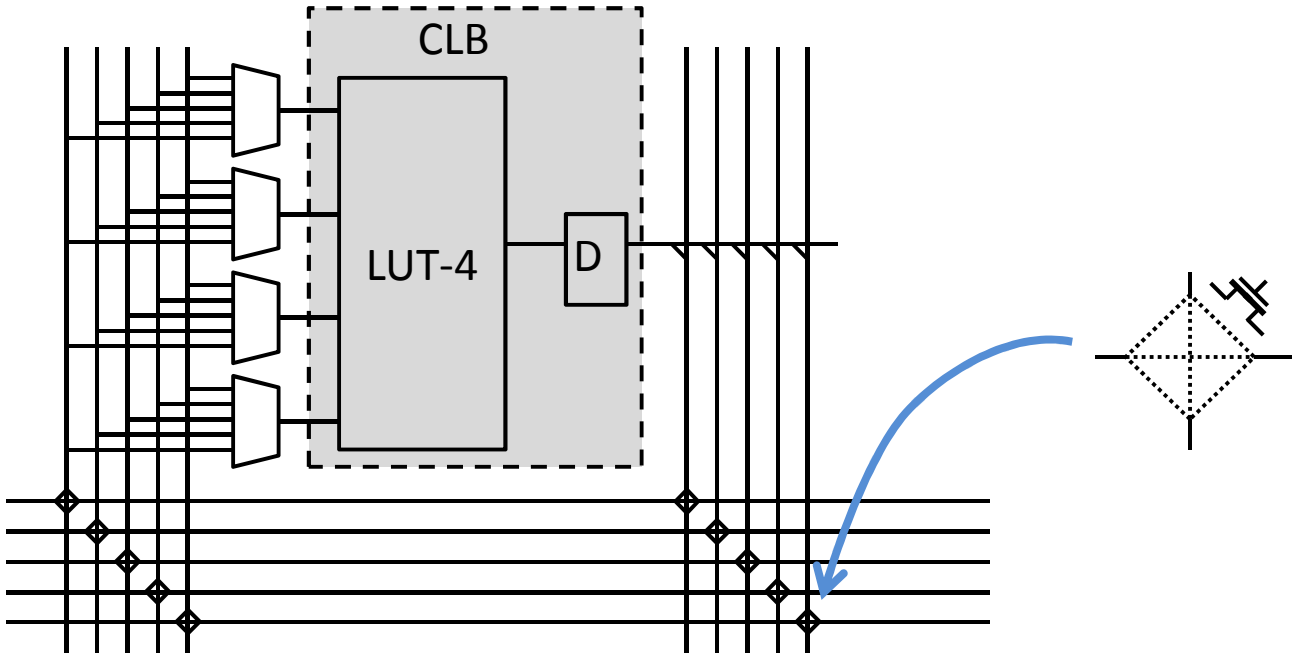
FPGA



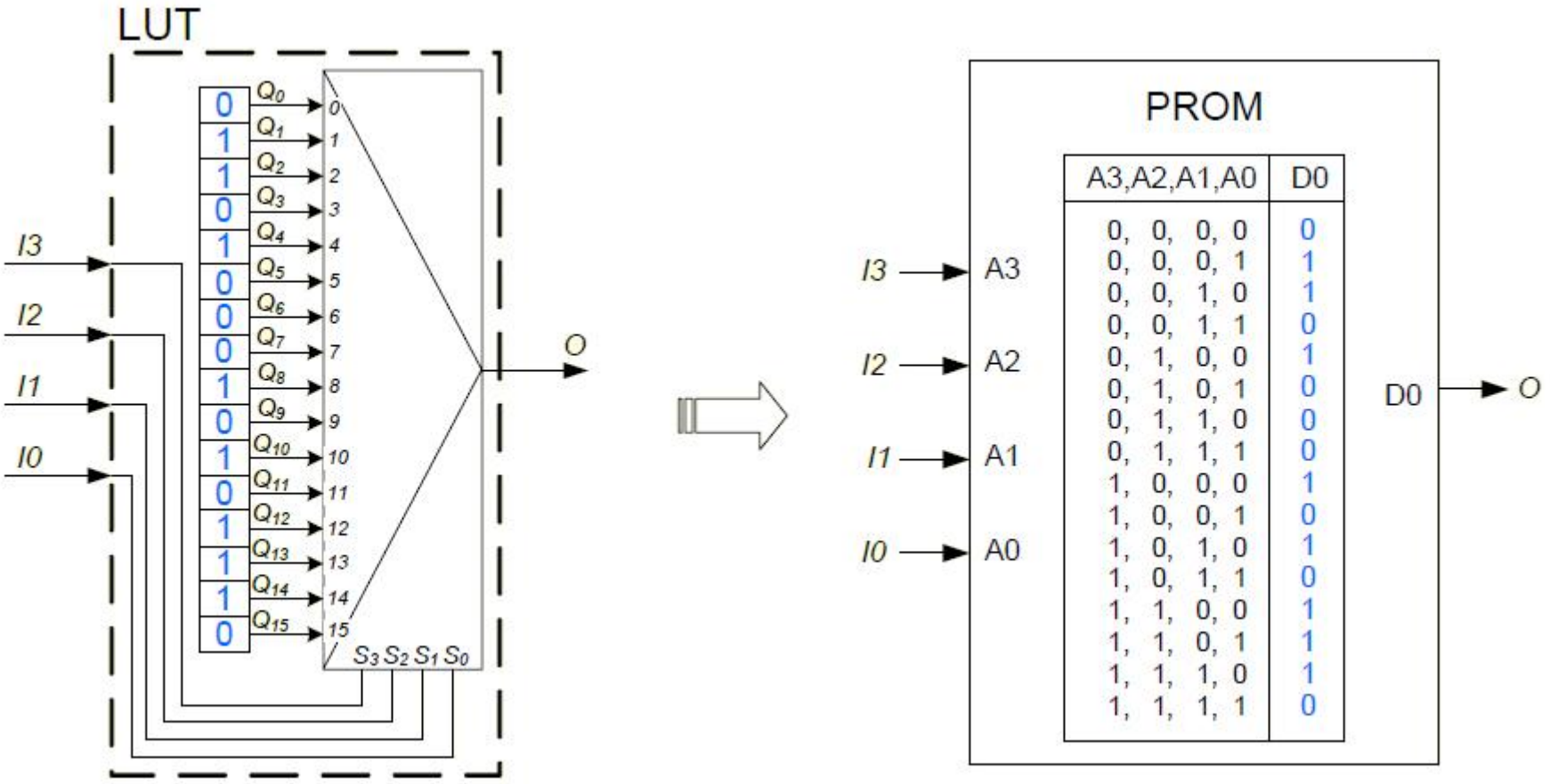
FPGA

CLB - Configurable Logic Block

- Look Up Table (LUT) small RAM implementing any 4 input logic function

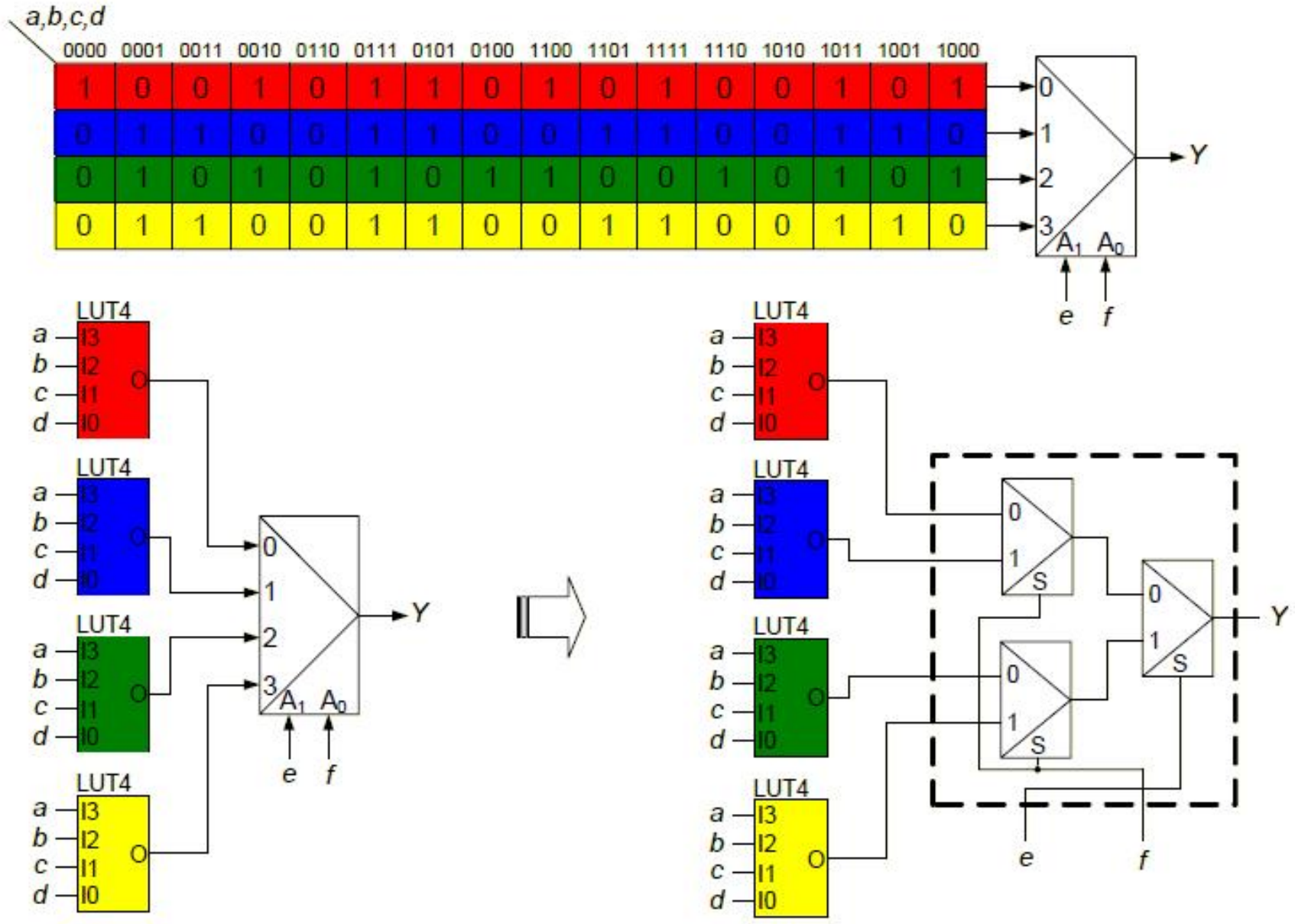


FPGA


LUT
I3
I2
I1
I0
O
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
S3 S2 S1 S0
PROM
A3,A2,A1,A0
D0
A3
A2
A1
A0
0, 0, 0, 0 0
0, 0, 0, 1 1
0, 0, 1, 0 1
0, 0, 1, 1 0
0, 1, 0, 0 1
0, 1, 0, 1 0
0, 1, 1, 0 0
0, 1, 1, 1 0
1, 0, 0, 0 1
1, 0, 0, 1 0
1, 0, 1, 0 1
1, 0, 1, 1 0
1, 1, 0, 0 1
1, 1, 0, 1 1
1, 1, 1, 0 1
1, 1, 1, 1 0

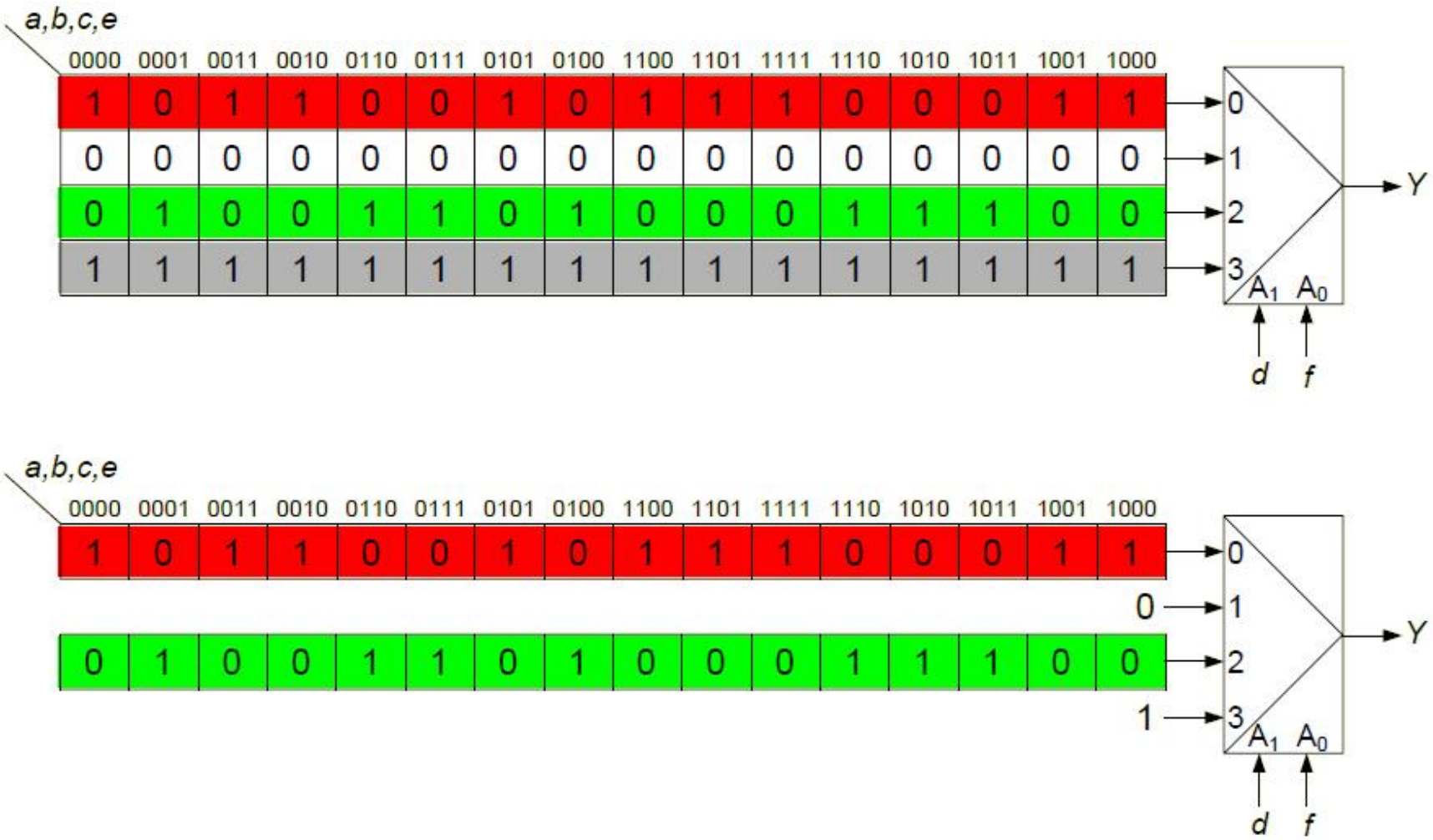
* [1]

FPGA


a,b,c,d
0000 0001 0011 0010 0110 0111 0101 0100 1100 1101 1111 1110 1010 1011 1001 1000
1 0 0 1 0 1 1 0 1 0 1 0 0 1 0 1
0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0
0 1 0 1 0 1 0 1 1 0 0 1 0 1 0 1
0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0
0 1 2 3
Y
A1 A0
e f
LUT4
a b c d
I3 I2 I1 I0
O
S

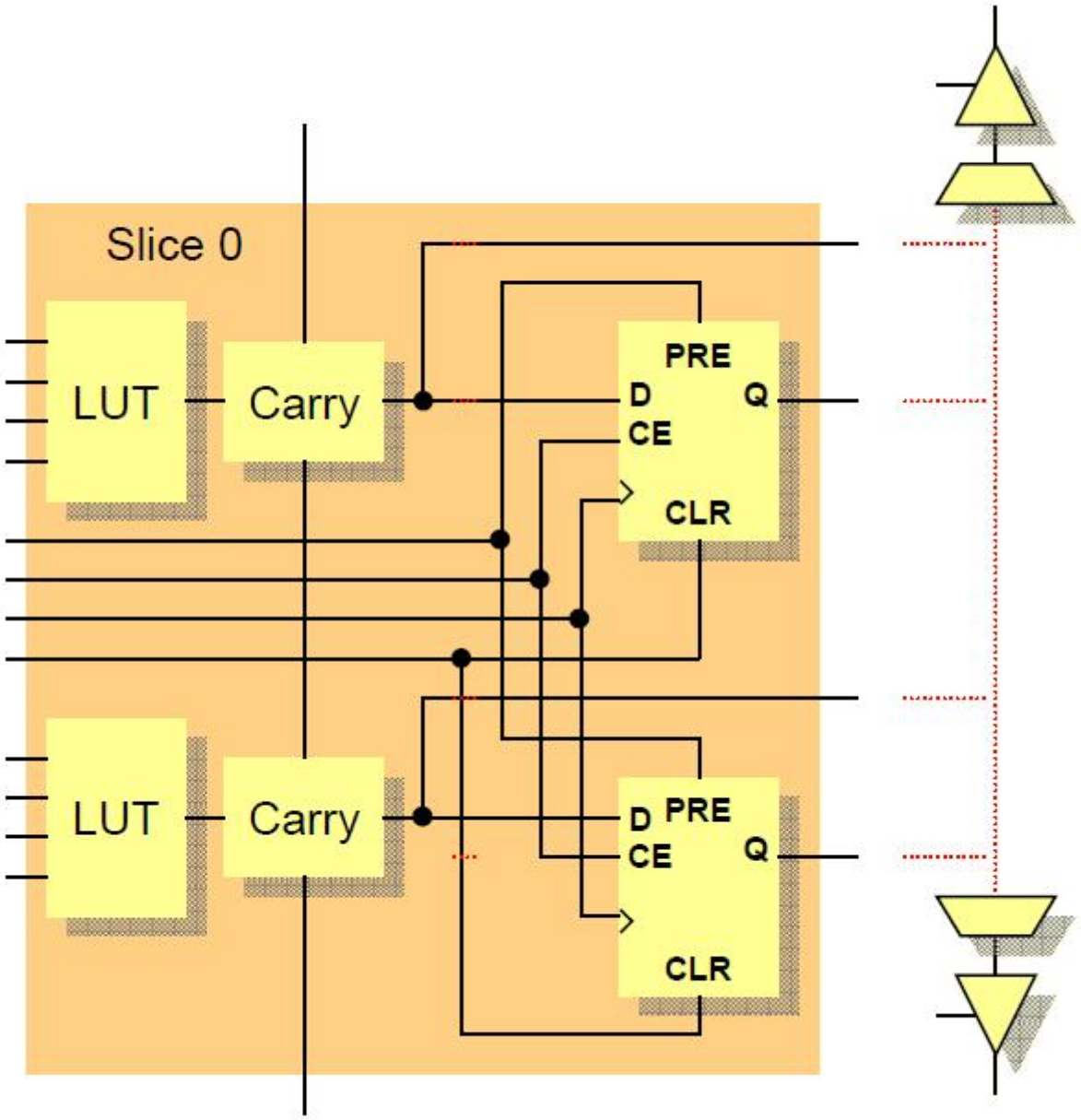
* [1]

FPGA

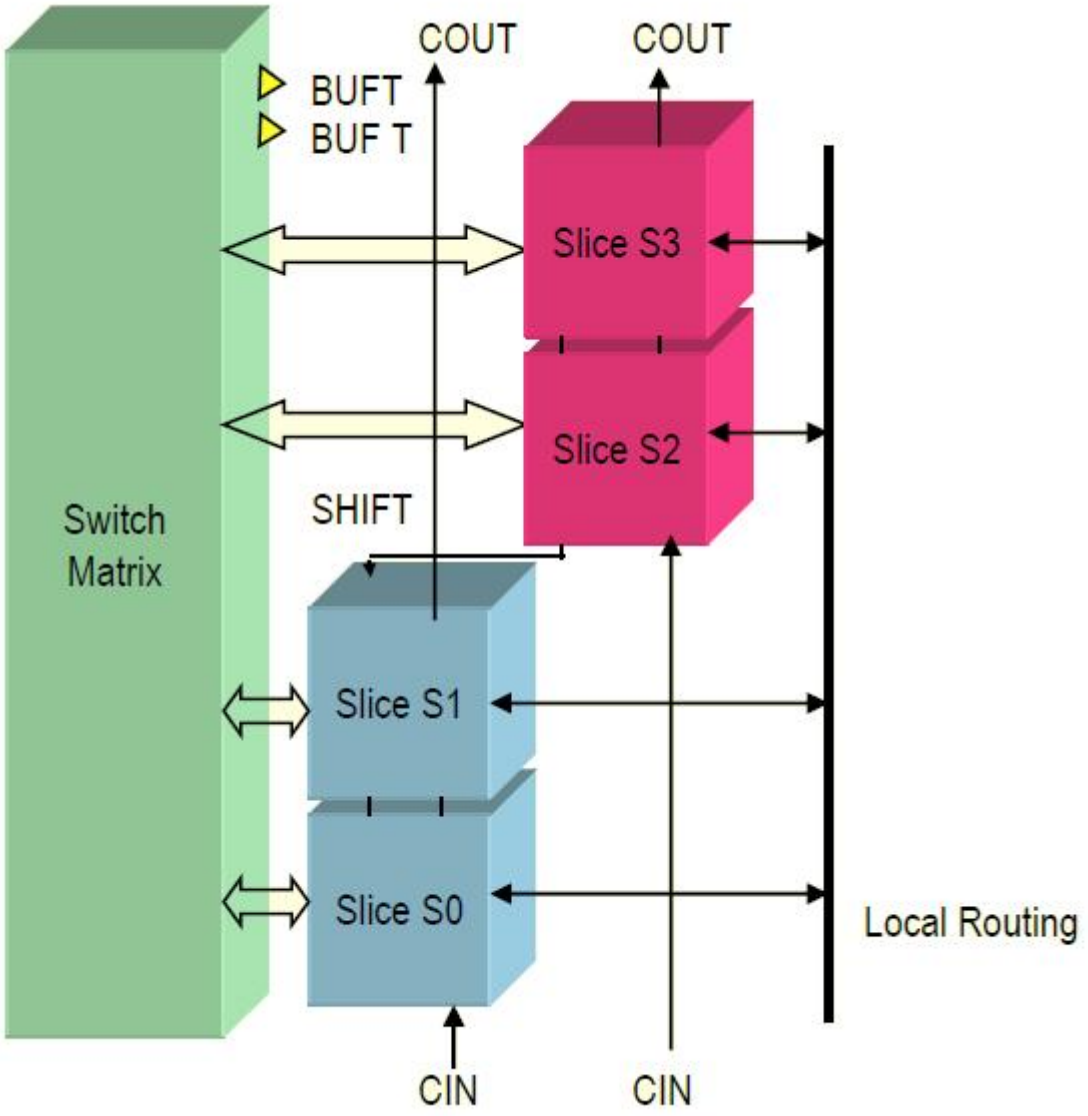

a,b,c,e
0000 0001 0011 0010 0110 0111 0101 0100 1100 1101 1111 1110 1010 1011 1001 1000
1 0 1 1 0 0 1 0 1 1 1 0 0 0 1 1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 1 0 0 1 1 0 1 0 0 0 1 1 1 0 0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
0
1
2
3
Y
A1 A0
d f
a,b,c,e
0000 0001 0011 0010 0110 0111 0101 0100 1100 1101 1111 1110 1010 1011 1001 1000
1 0 1 1 0 0 1 0 1 1 1 0 0 0 1 1
0 1 0 0 1 1 0 1 0 0 0 1 1 1 0 0
0
1
0
1
2
3
Y
A1 A0
d f

* [1]

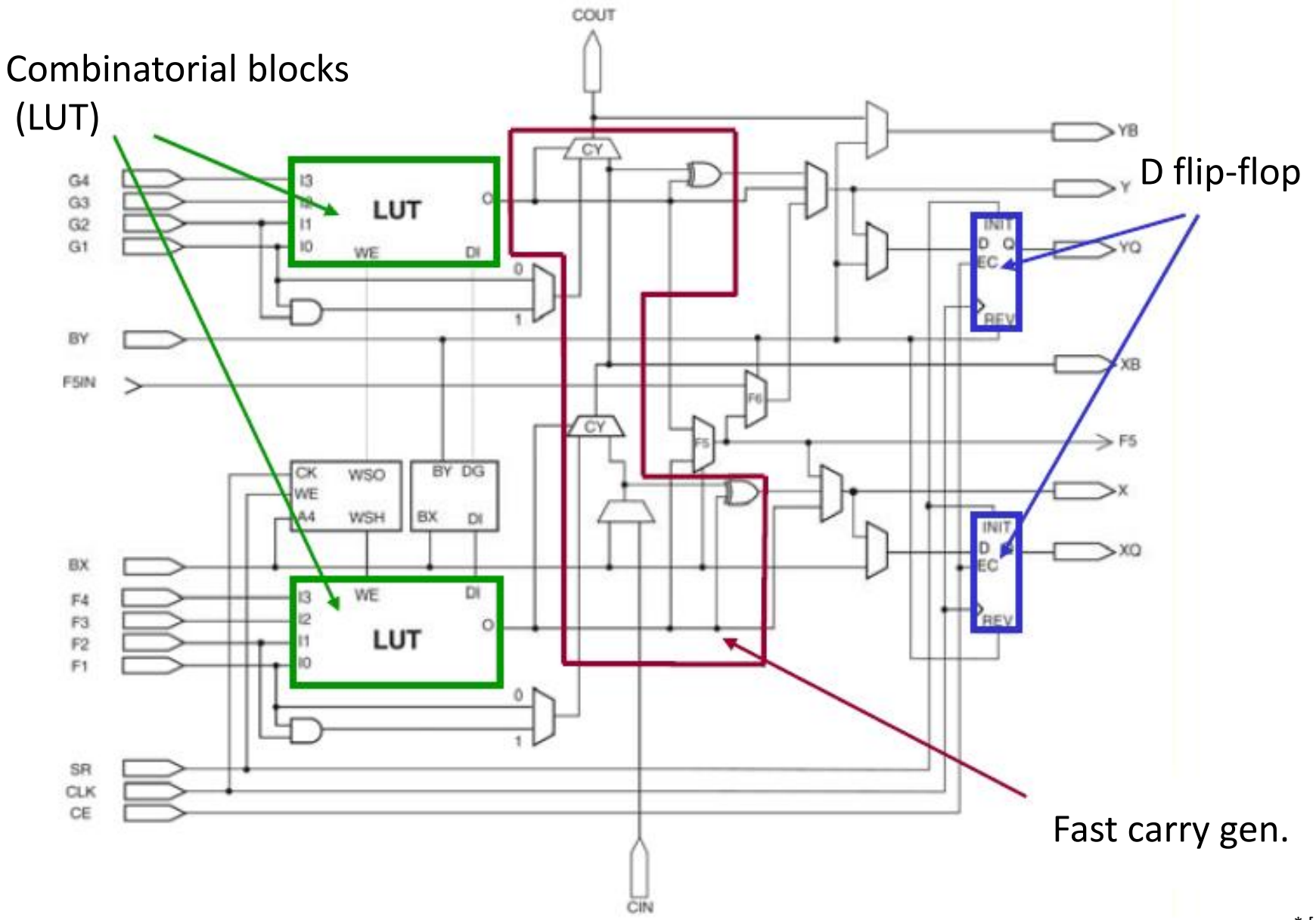
FPGA



FPGA

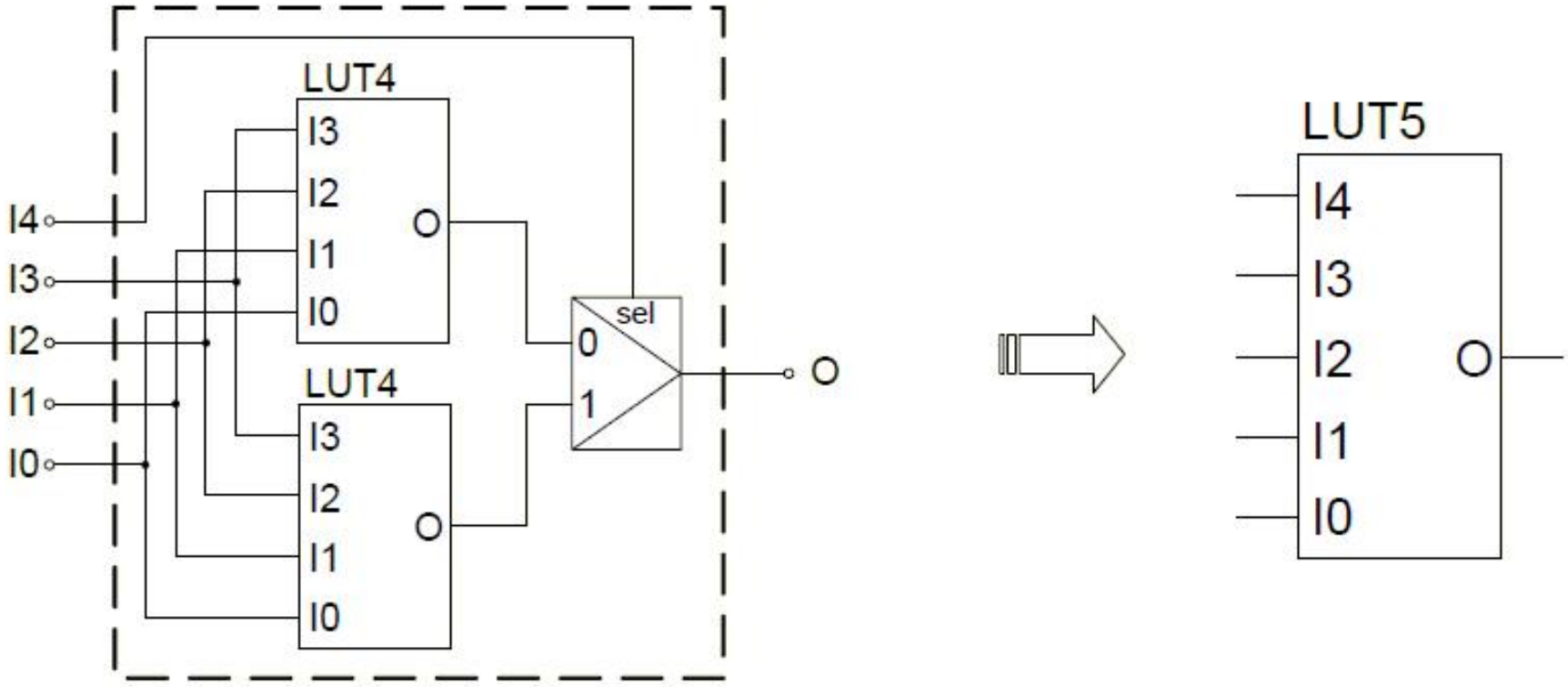

COUT
COUT
BUFT
BUF T
Slice S3
Slice S2
Switch
Matrix
SHIFT
Slice S1
Slice S0
Local Routing
CIN
CIN

FPGA

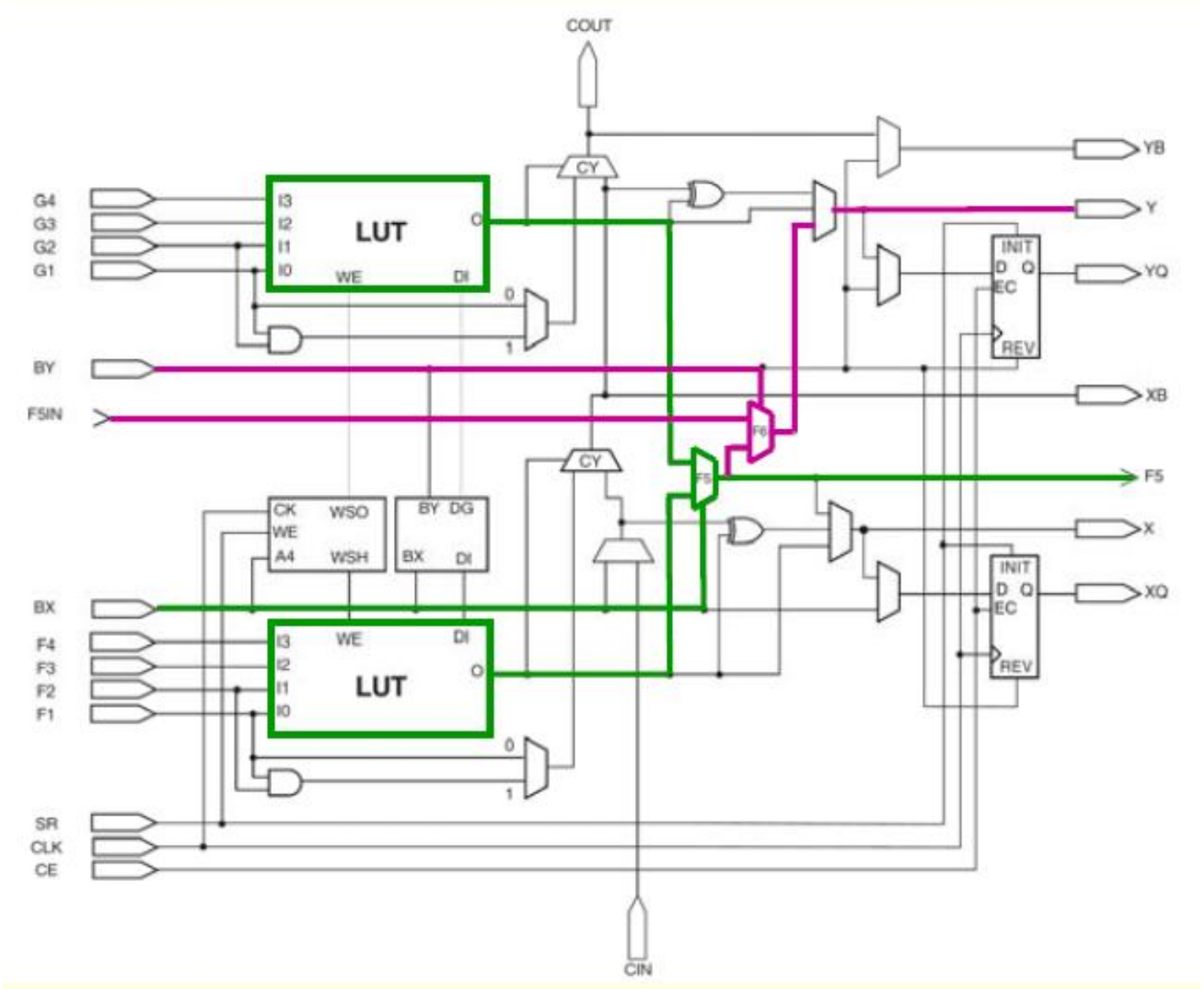

Combinatorial blocks
(LUT)
D flip-flop
Fast carry gen.
COUT
CIN
LUT
LUT
CY
CY
G4
G3
G2
G1
BY
F5IN
BX
F4
F3
F2
F1
SR
CLK
CE
YB
Y
YQ
XB
F5
X
XQ
INIT
REV
WE
DI
CK
WSO
WSH
BX
BY DG

* [1]

FPGA

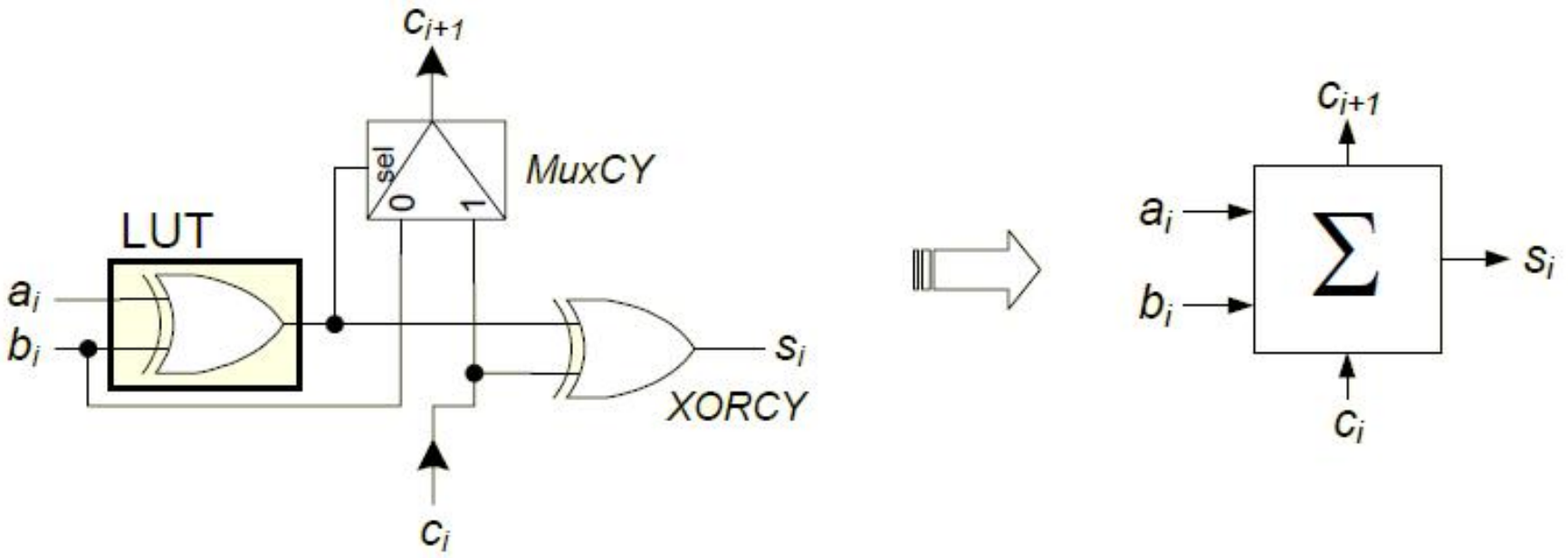

LUT4
I3
I2
I1
I0
O
LUT4
I3
I2
I1
I0
O
sel
0
1
O
I4
I3
I2
I1
I0
LUT5
I4
I3
I2
I1
I0
O

FPGA


COUT
CY
YB
Y
YQ
G4
G3
G2
G1
I3
I2
I1
I0
LUT
O
WE
DI
0
1
INIT
D Q
EC
REV
BY
FSIN
XB
F6
CY
F5
F5
CK
WE
A4
WSO
WSH
BY DG
BX
DI
X
INIT
D Q
EC
REV
XQ
BX
F4
F3
F2
F1
I3
I2
I1
I0
WE
DI
LUT
O
0
1
SR
CLK
CE
CIN

FPGA

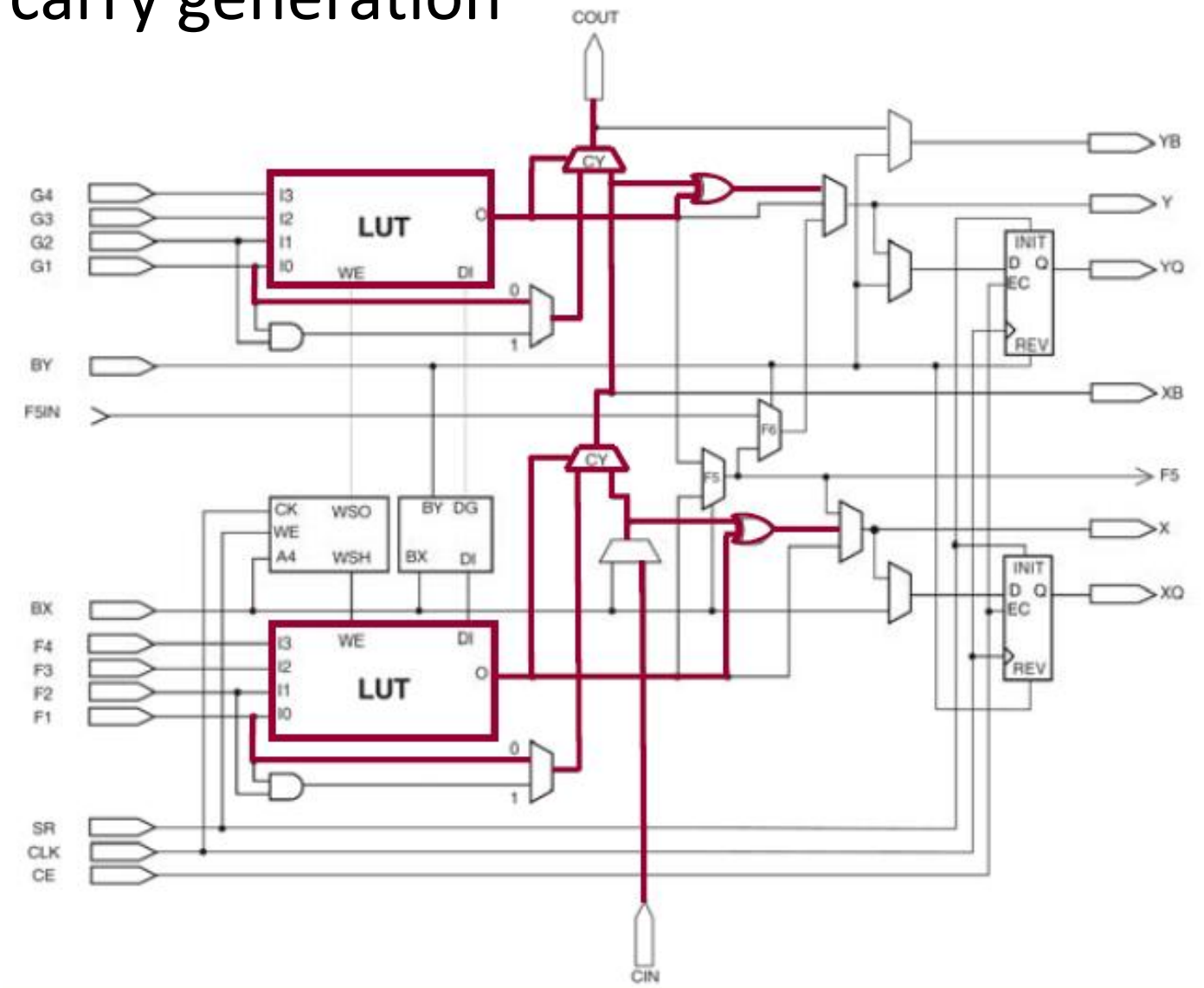
Fast carry generation



* [1]

FPGA

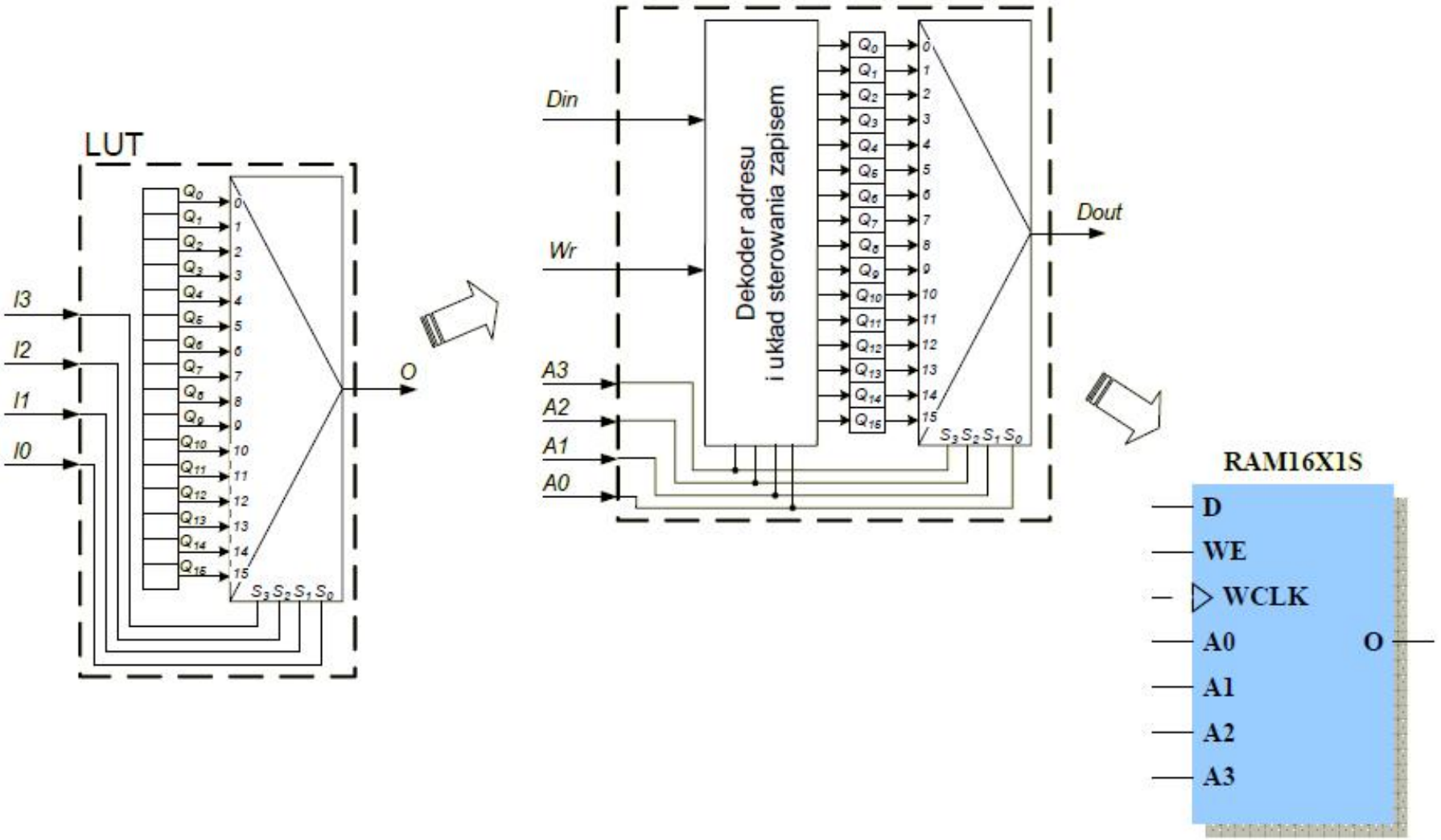
Fast carry generation



* [1]

FPGA

LUT RAM



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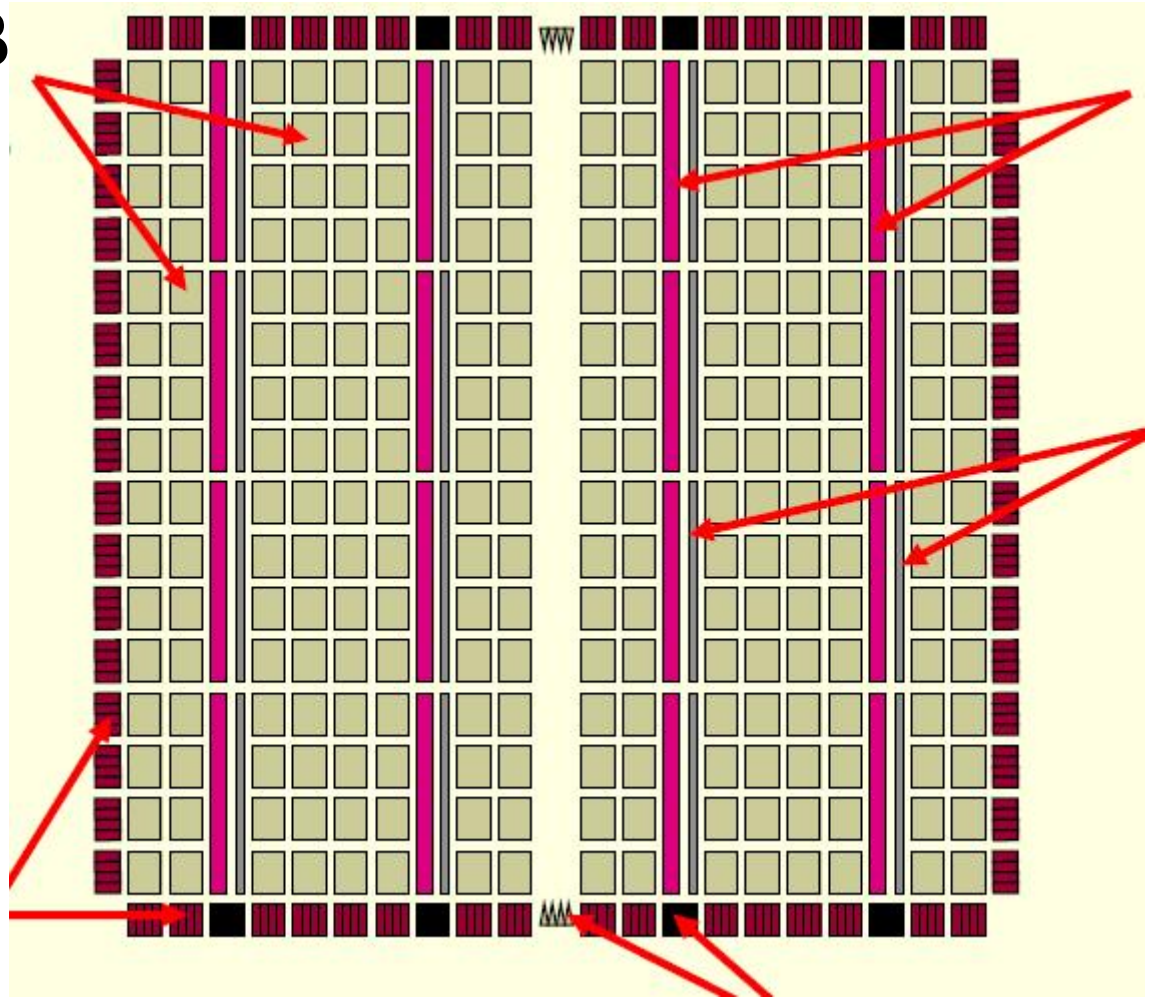
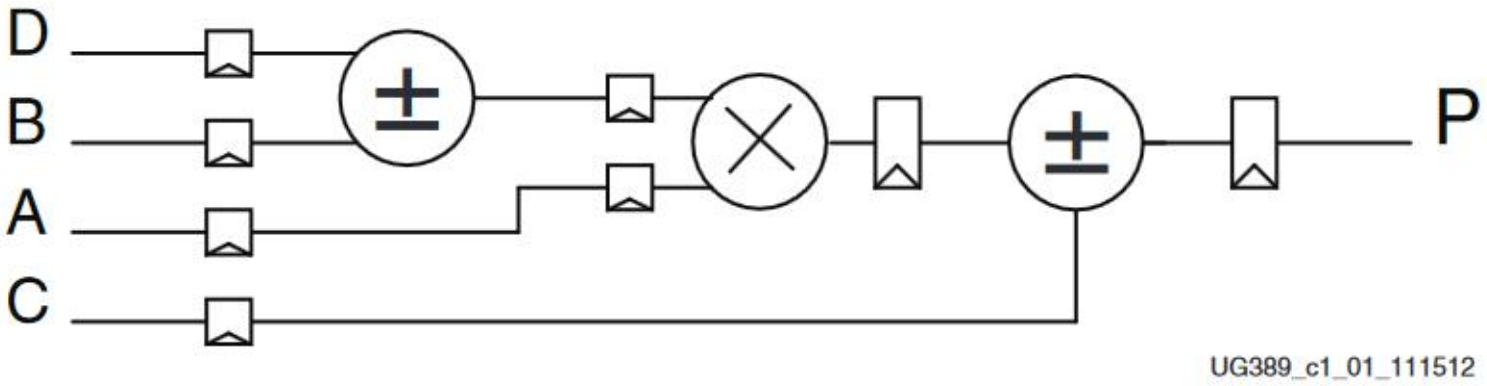
FPGA



* [1]

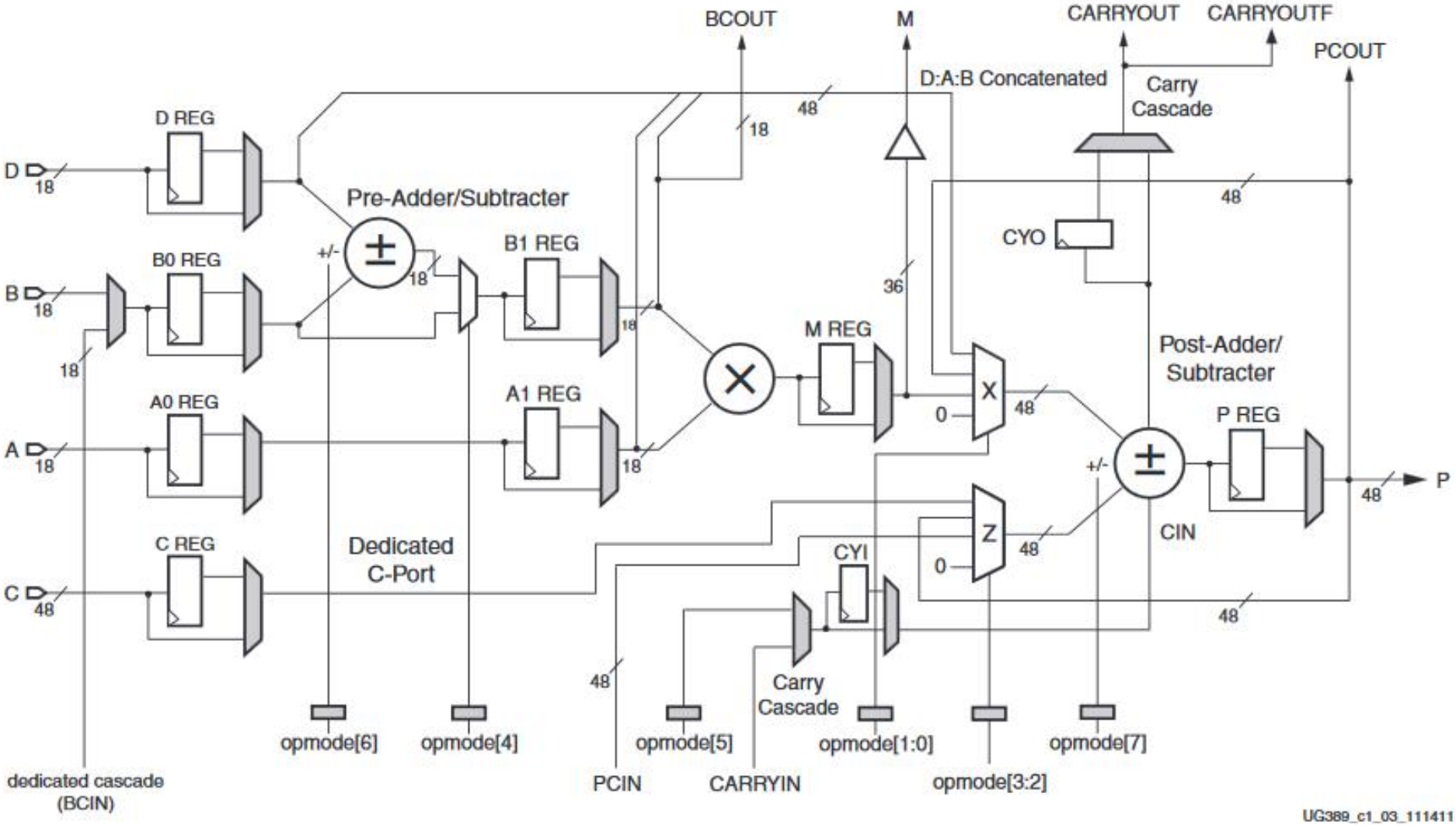
FPGA

- Adder/Multiplier (DSP48)



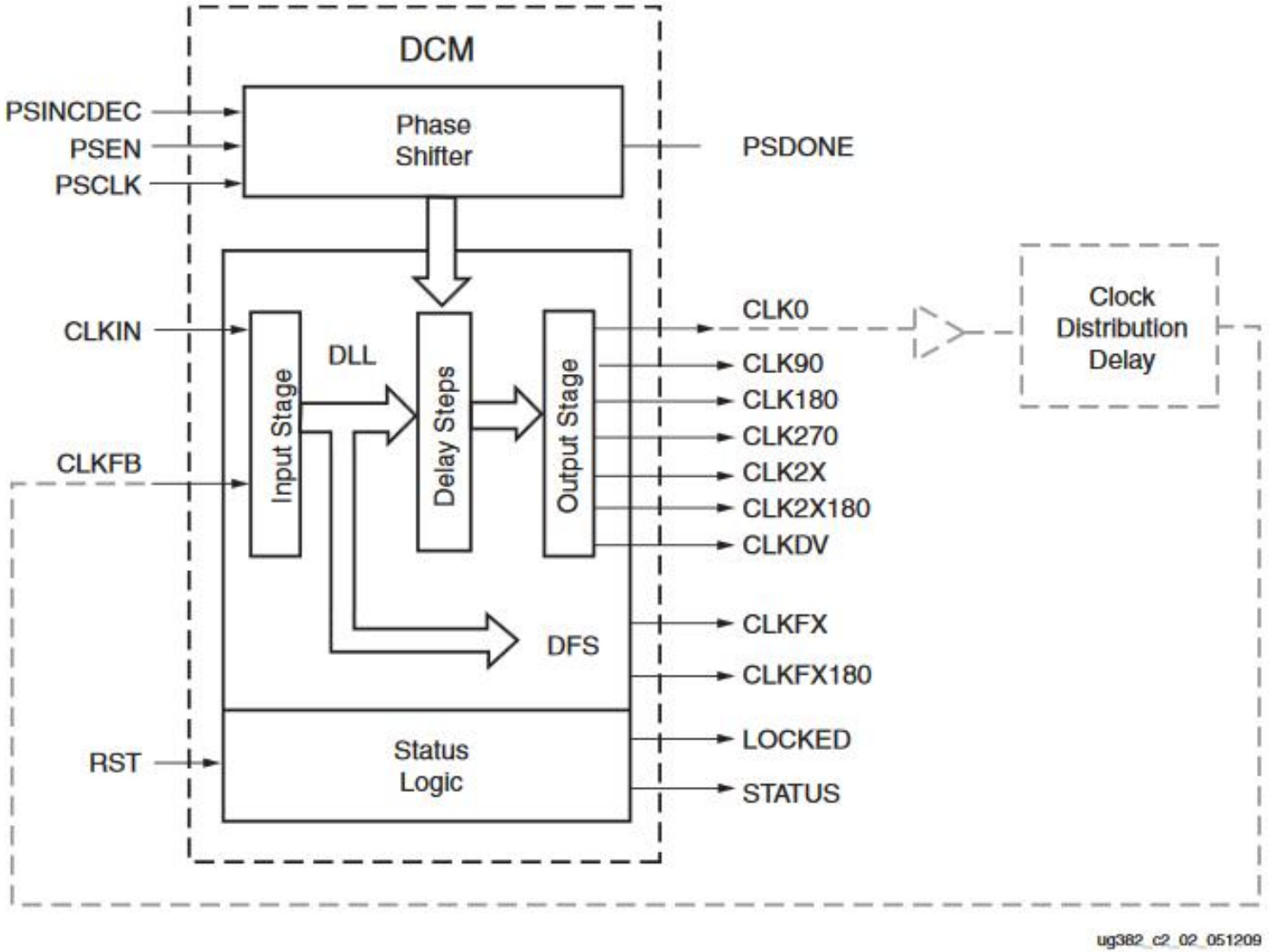
FPGA

- Adder/Multiplier (DSP48)



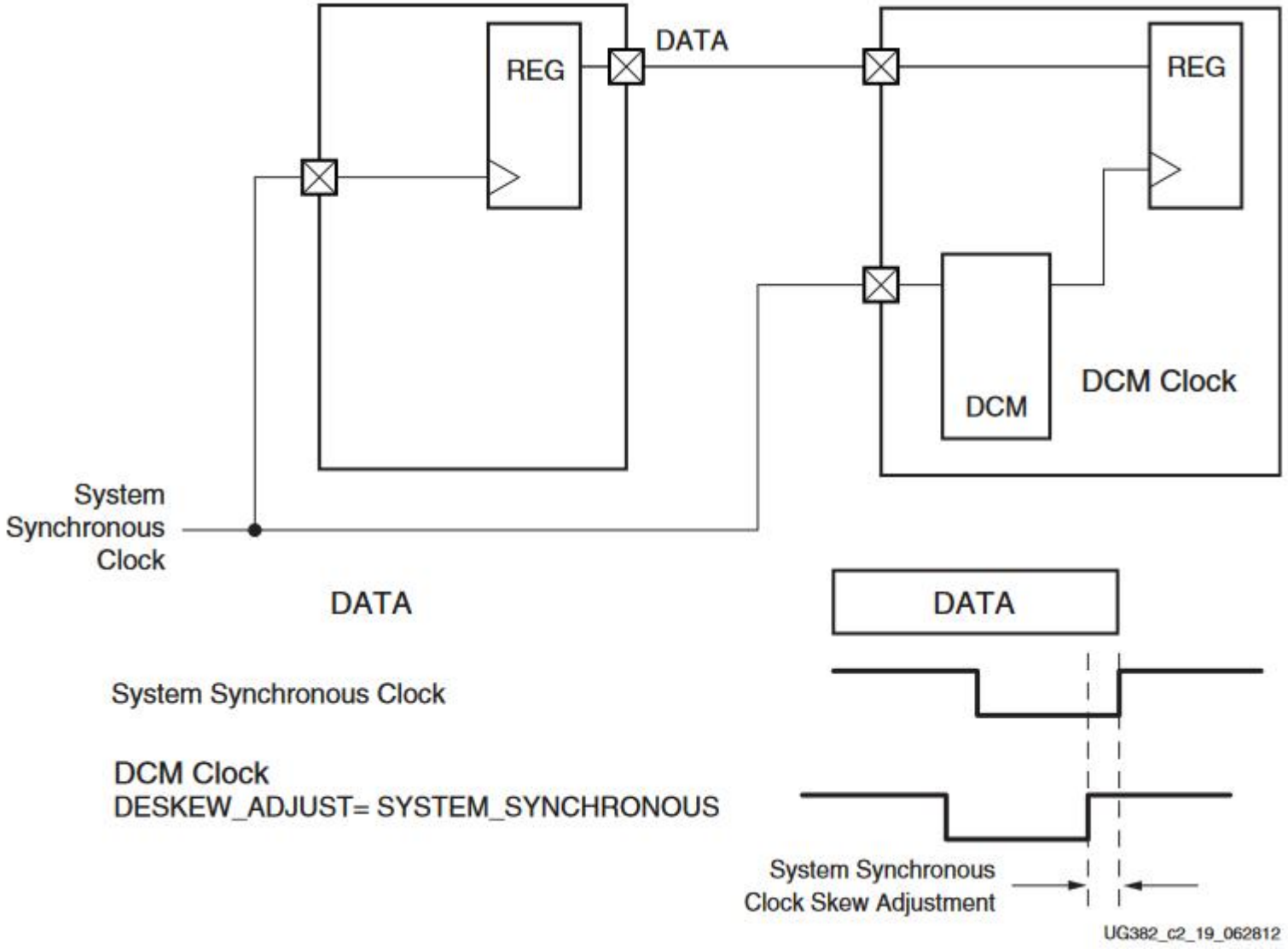
FPGA

- Digital Clock Manager/Phase Locked Loop

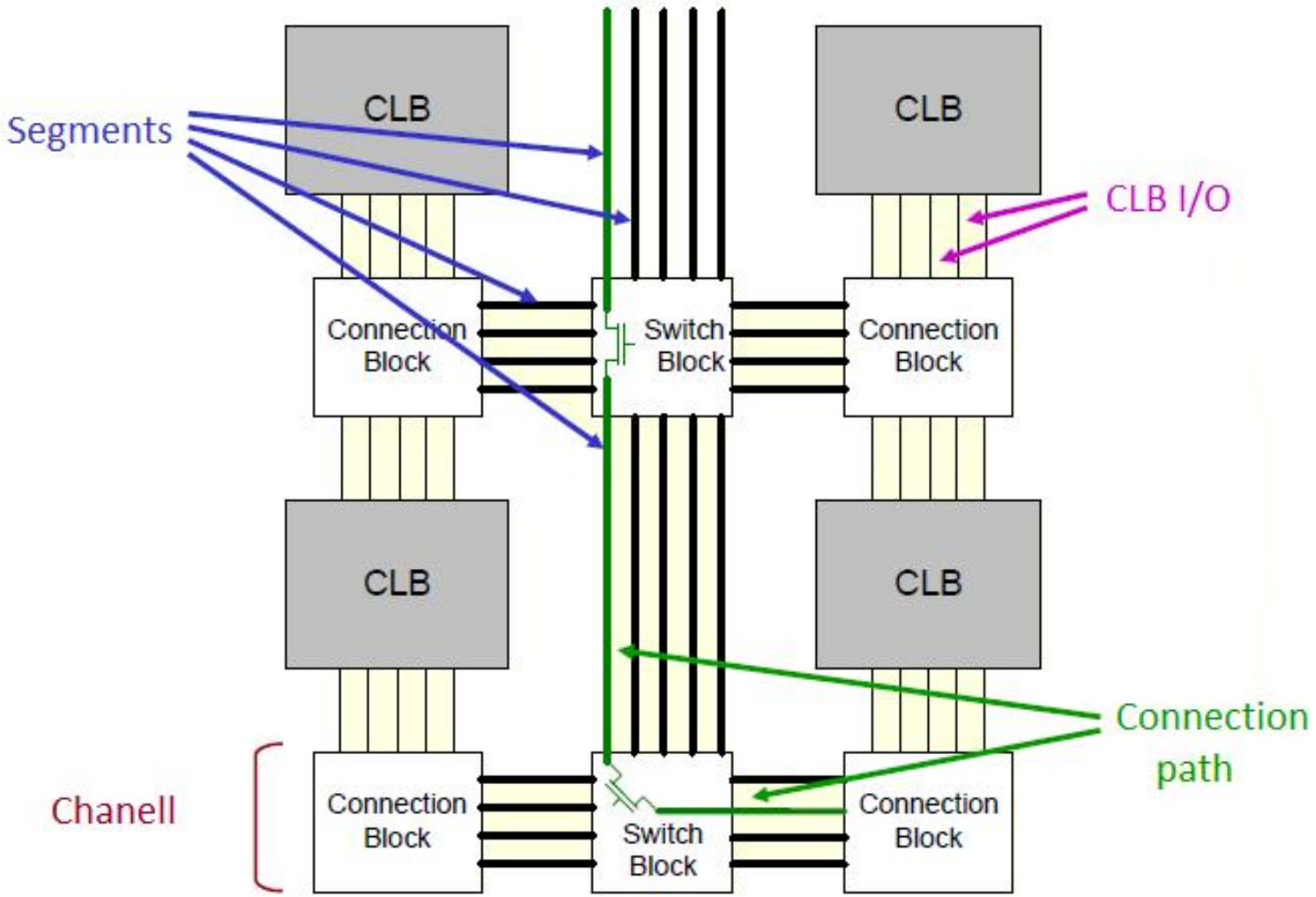


FPGA

- DCM –adjusting clock skew



FPGA – connection matrix



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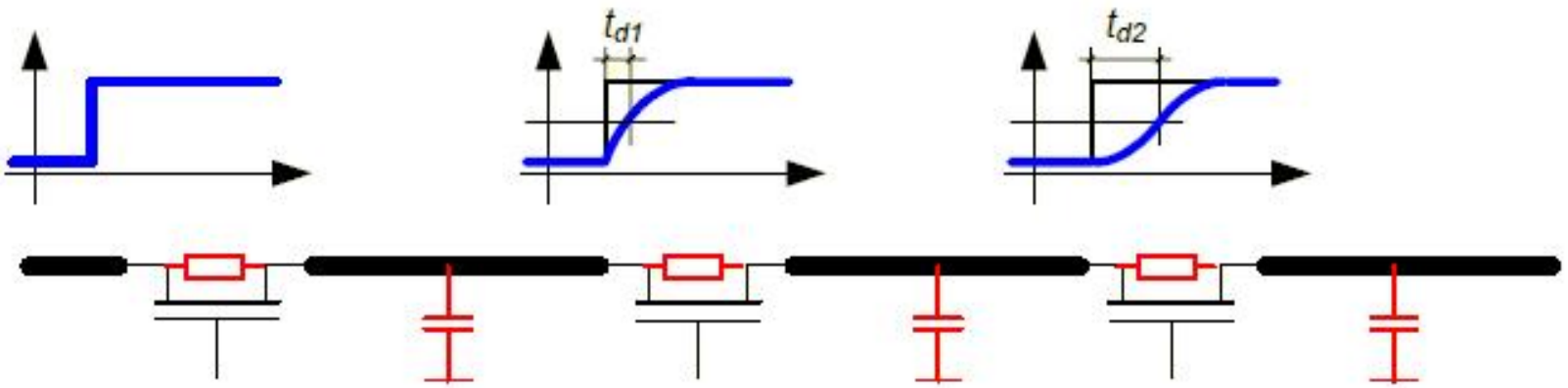

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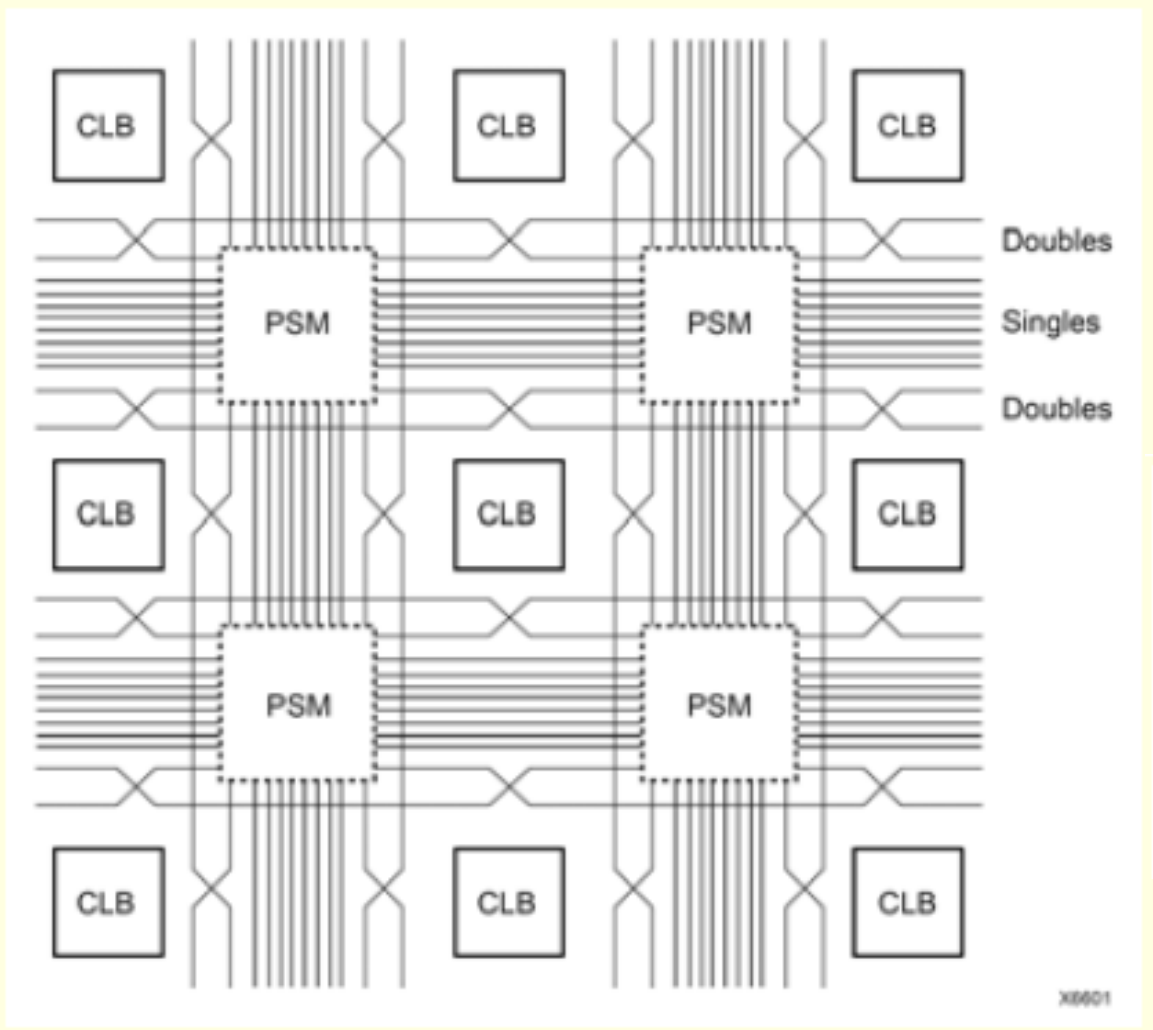
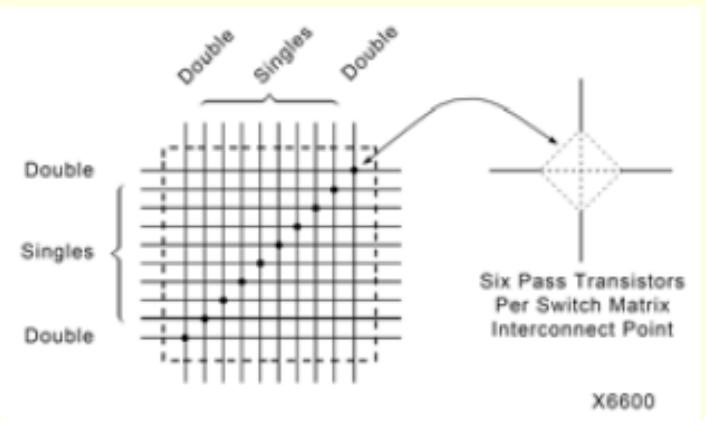
FPGA



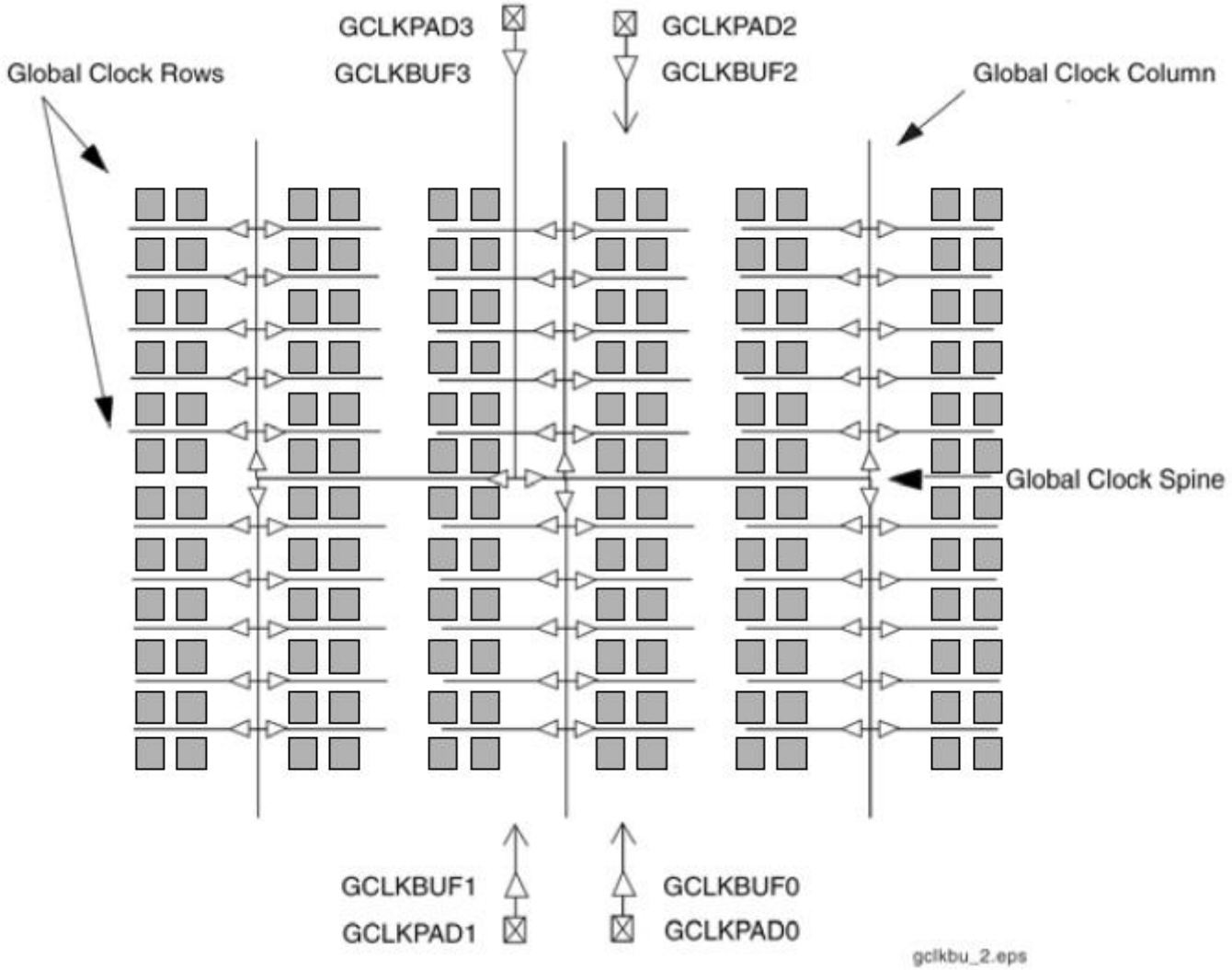
PSM- Programmable Switch Matrix



* [2]

FPGA

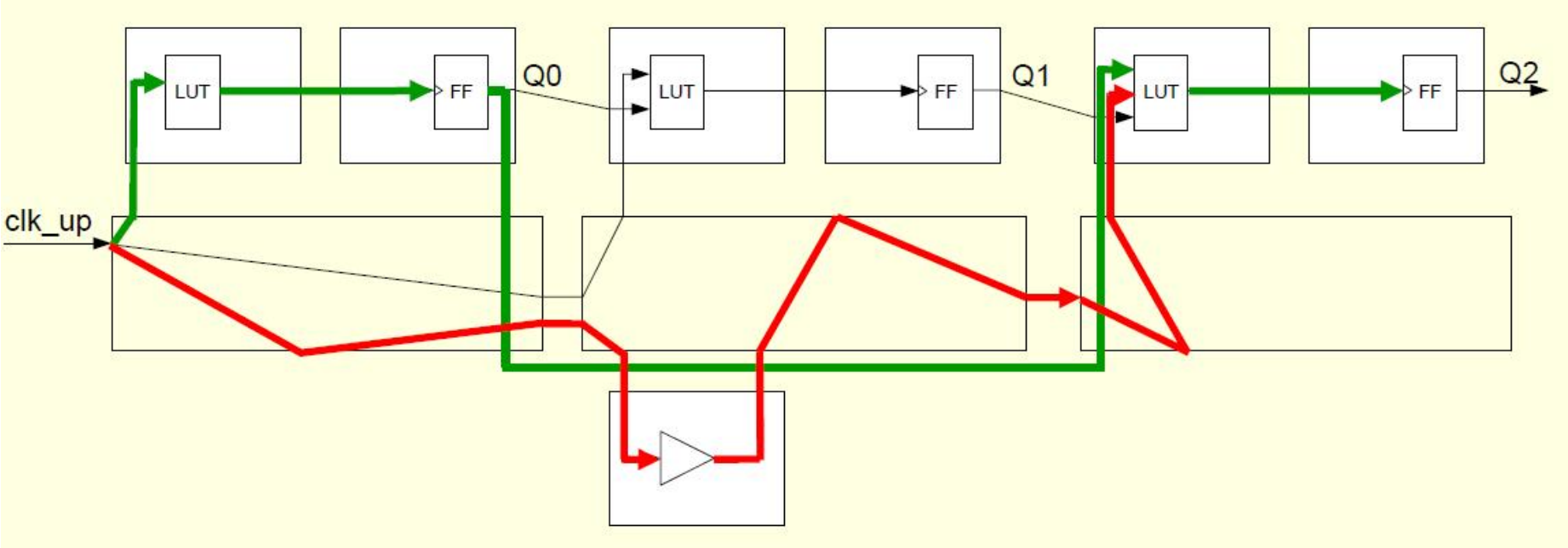
Global clocks signal distribution



* [2]

FPGA

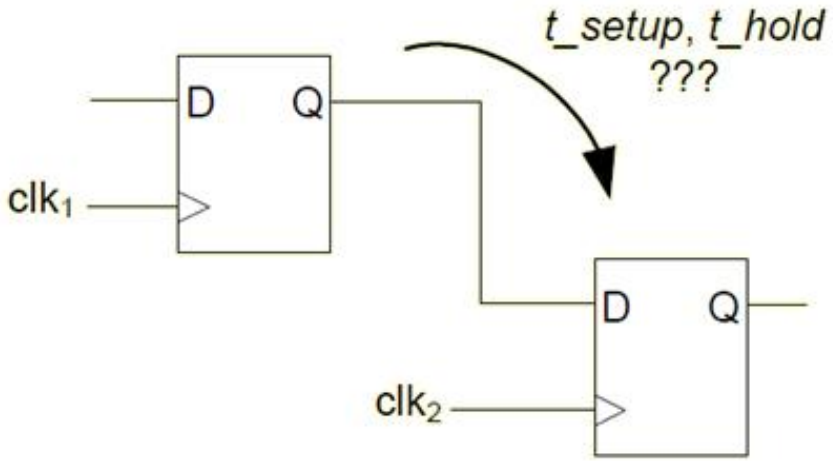
- Clock skew

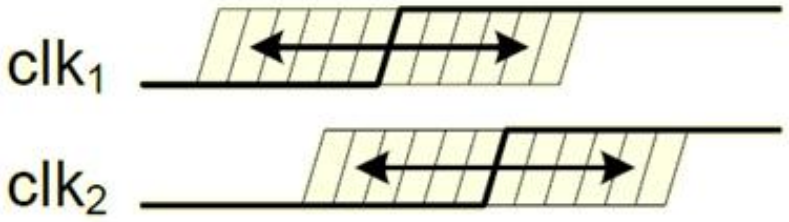


* [1]

FPGA

- Independent clock signals





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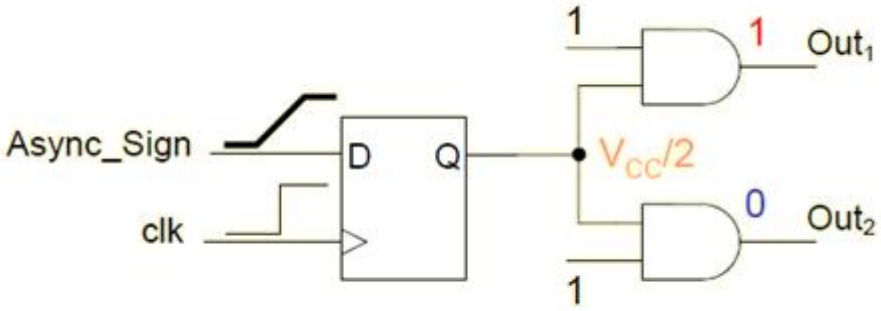
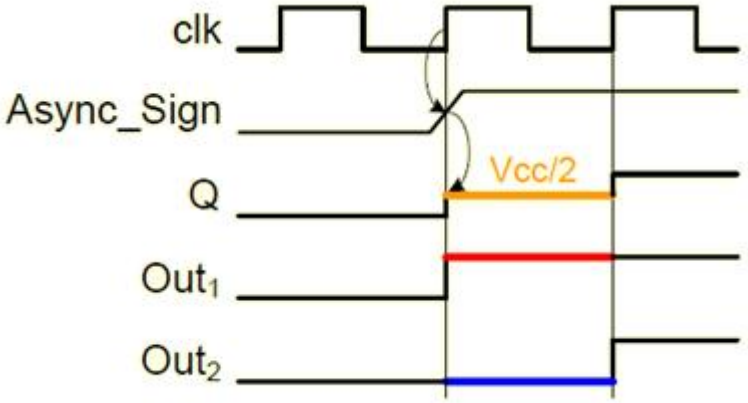
FPGA

- Metastability





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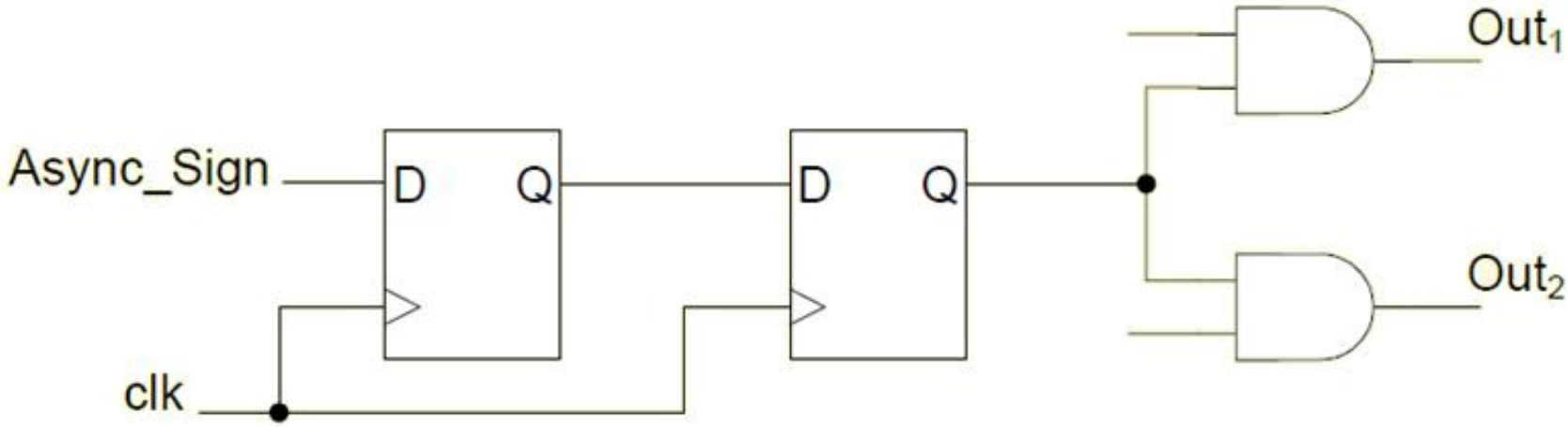
FPGA

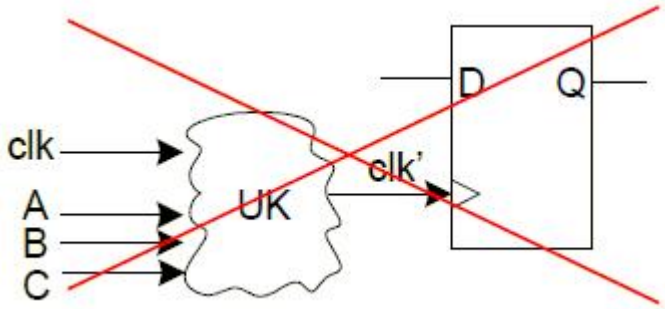
- Metastability

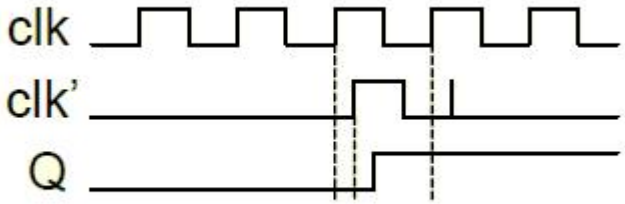


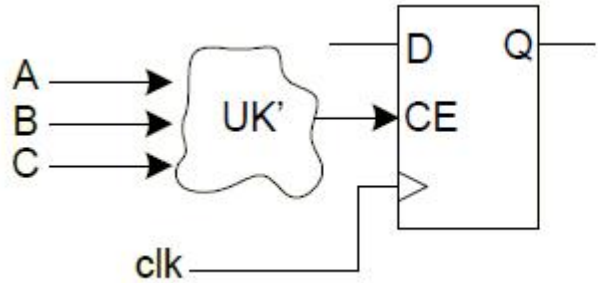
* [1]

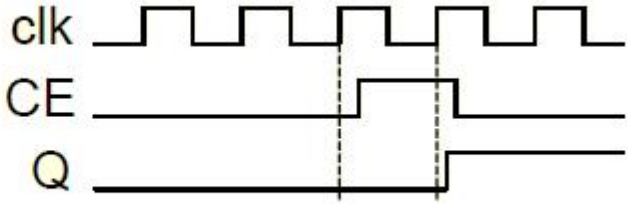
FPGA

- Clock enable signal





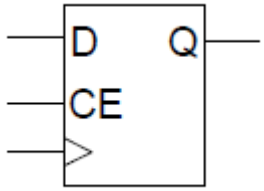


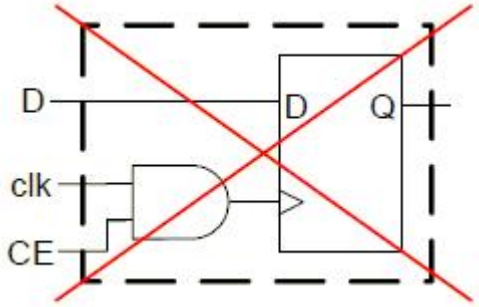


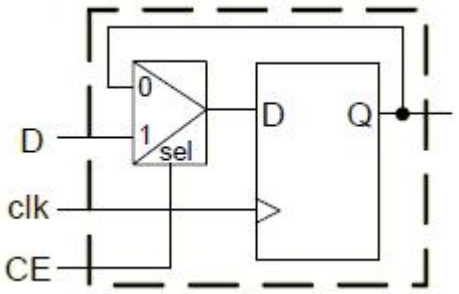
* [1]

FPGA

- Clock enable signal



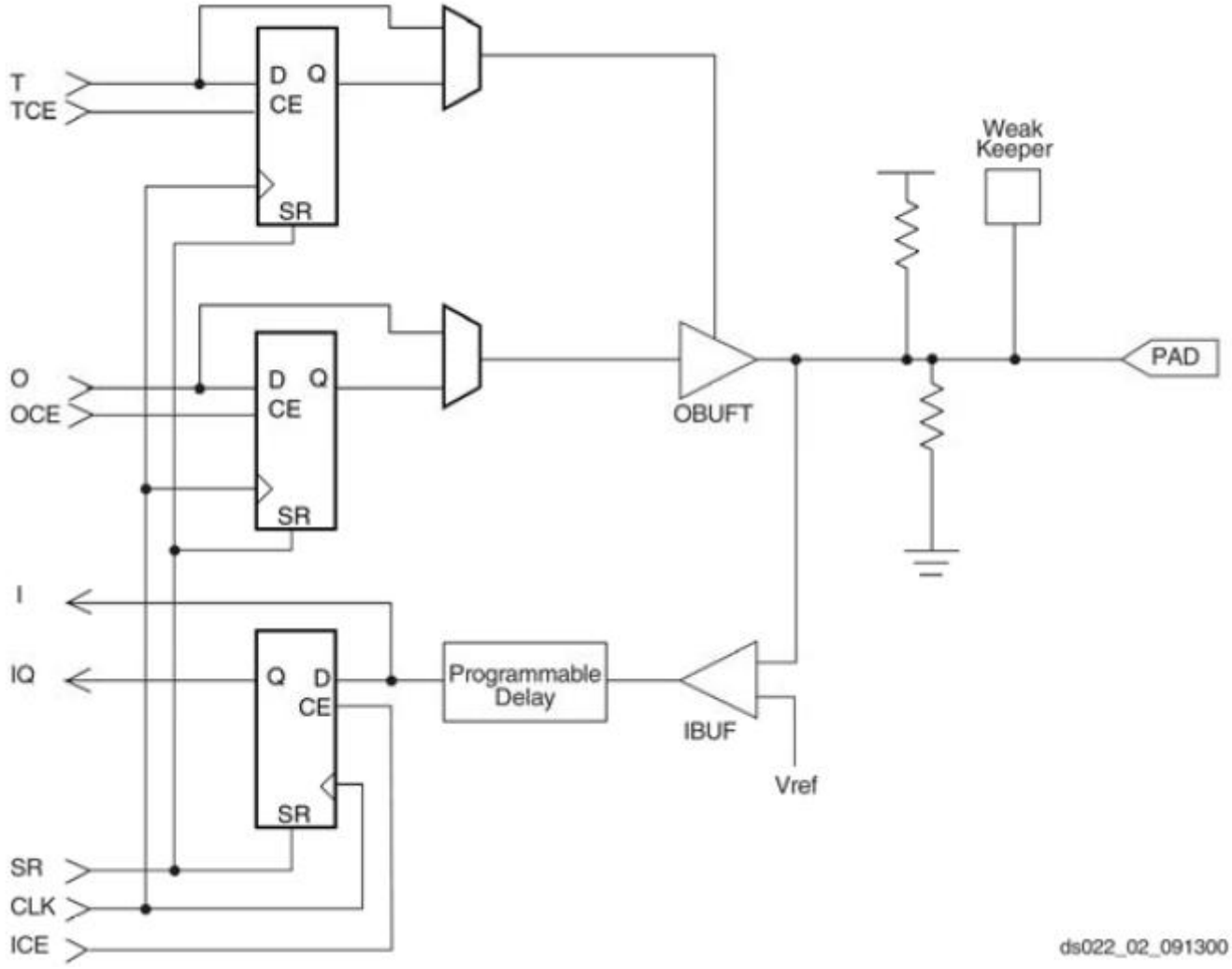




* [1]

FPGA

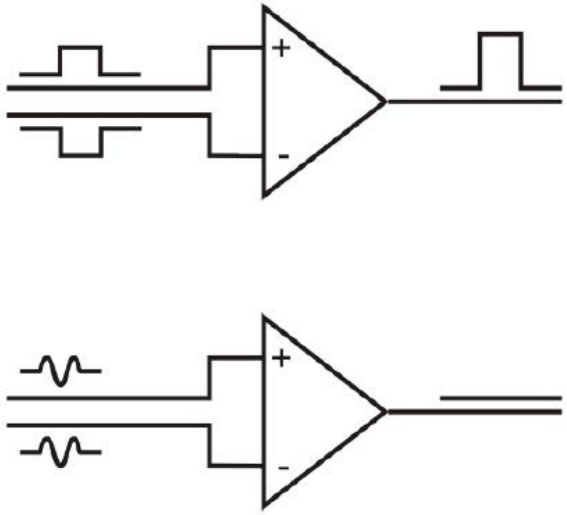
I/O Block



FPGA

I/O standards (Virtex-5):

- Nonsymmetric:
  - LVCMOS (3.3V, 2.5V, 1.8V, 1.5V, 1.2V)
  - LVTTL
  - HSTL (1.5V, 1.8V; Class I, II, III i IV)
  - HSTL (1.2V, Class I)
  - SSTL (2.5V, 1.8V; Class I i II)
  - GTL i GTLP
  - PCI (33 i 66 MHz), PCI-X
- Differential:
  - LVDS i Extended LVDS (2.5V)
  - HT
  - LVPECL
  - BLVDS
  - ULVDS
  - HSTL (1.2V i 1.8V, Class I i II)
  - SSTL (2.5V, 1.8V; Class I i II)
  - RSDS (2.5V)



FPGA

Sources:

[1] Józef Kulisz, *Programowalne Układy Cyfrowe*

[2] www.xilinx.com

* [1]